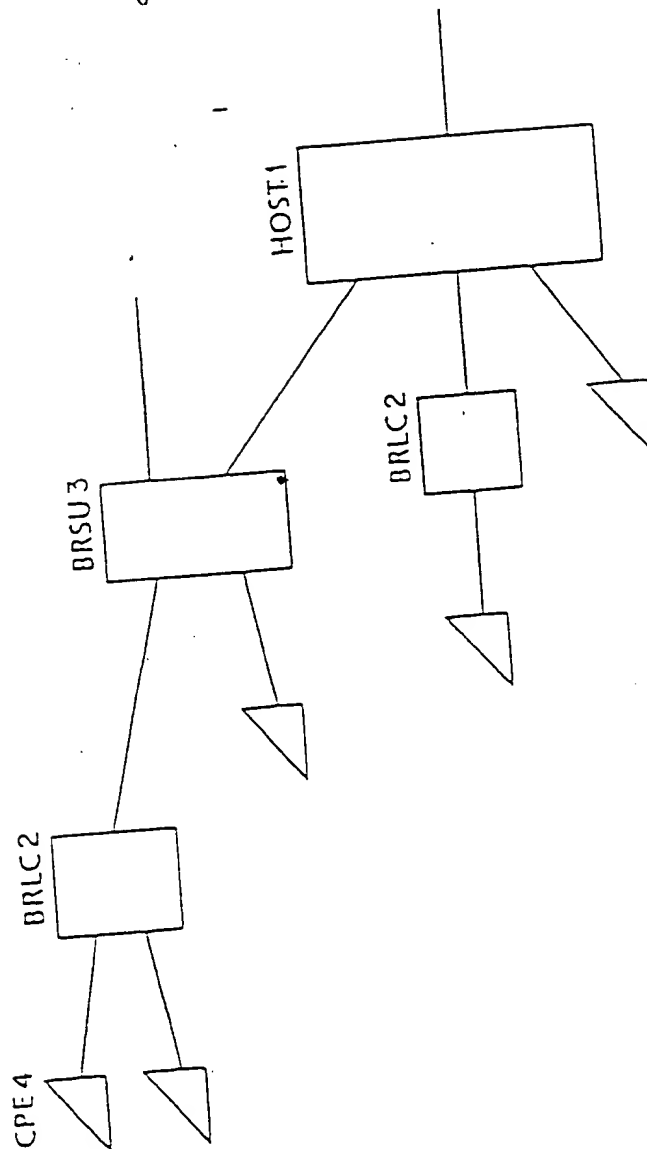


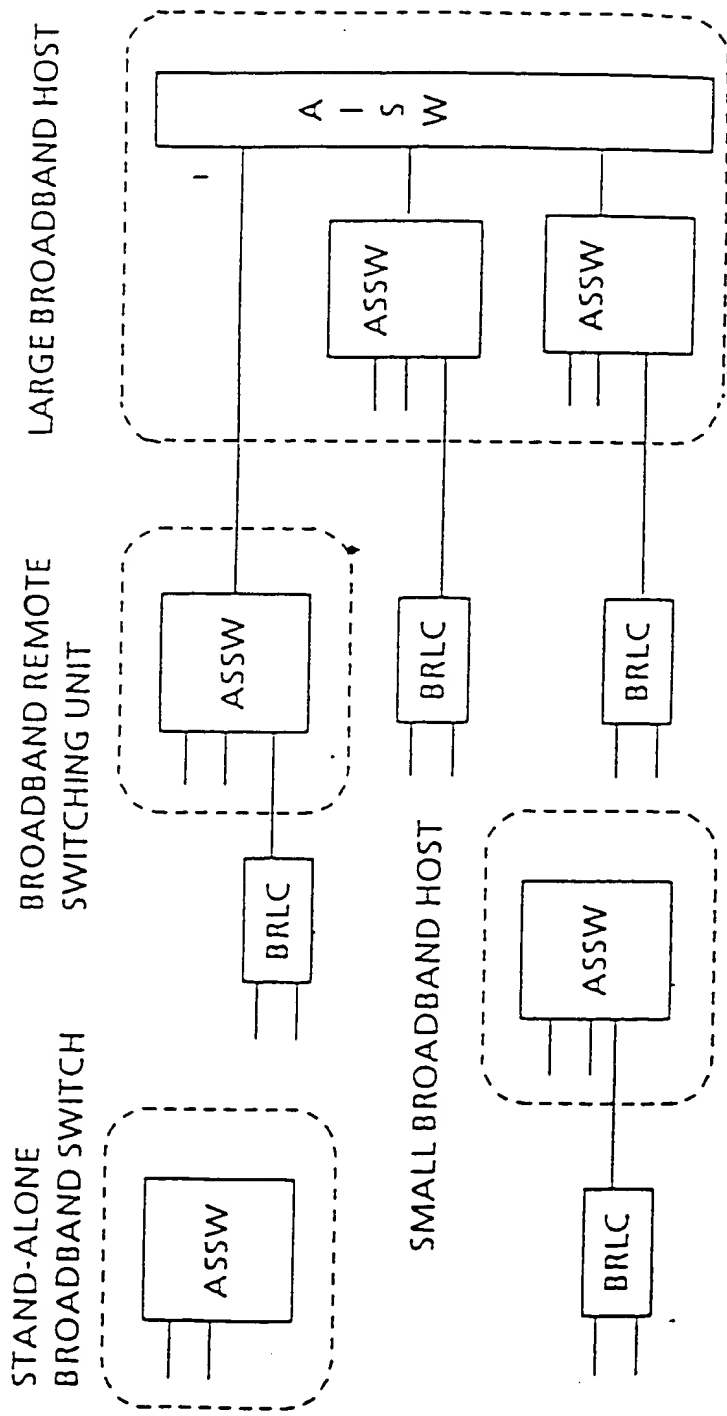
APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

54
-14
004



BRLC : Broadband Remote Line Concentrator
 BRSU : Broadband Remote Switching Unit
 CPE : Customer Premises Equipment
 HOST : Broadband Host Switch

FIG. 1

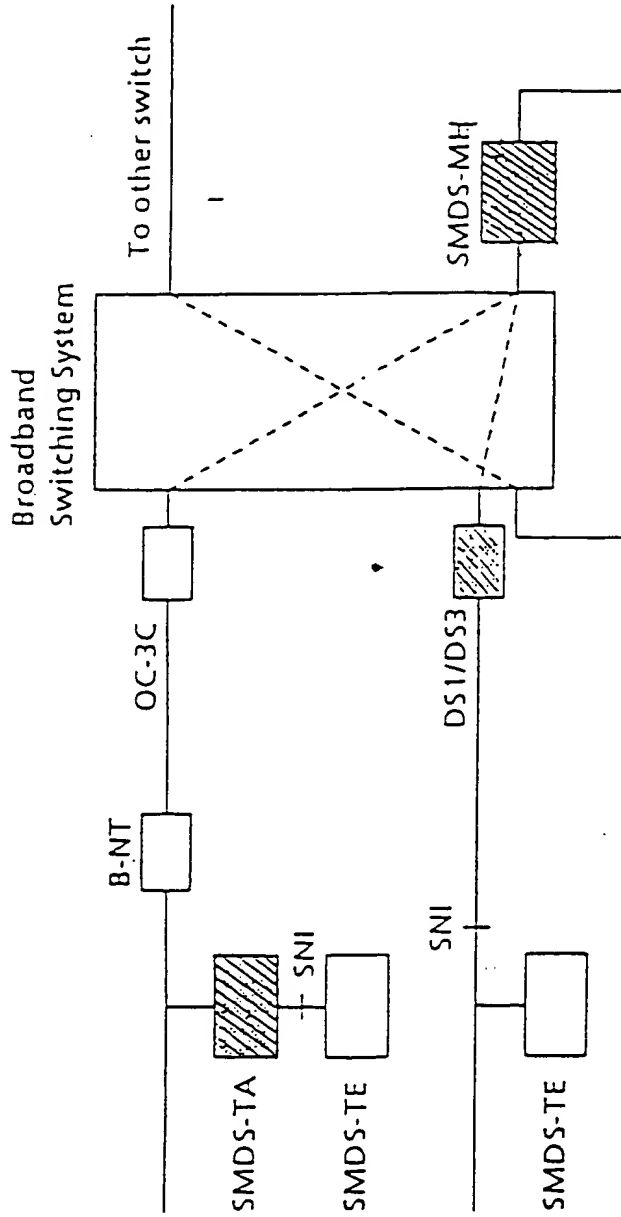


ASSW ATM Subscriber Switch
 AISW ATM Interconnection Switch
 BRLC Broadband Remote Line Concentrator

FIG. 2

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

66930-01-0000



B-NT : Broadband Network Termination
 SMDS-MH: SMDS Message Handler
 SMDS-TA : SMDS Terminal Adapter
 SMDS-TE : SMDS Terminal Equipment

FIG. 3

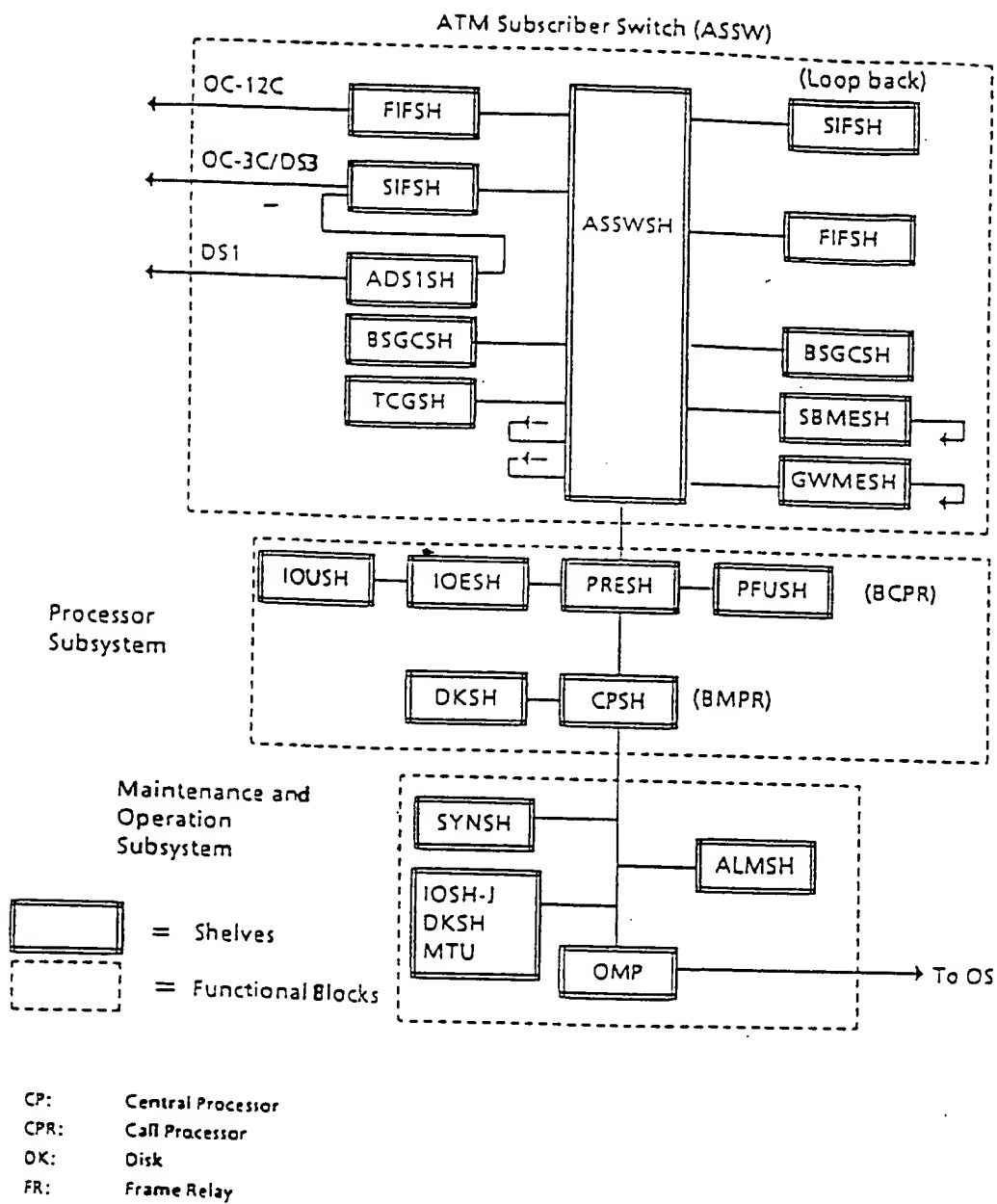


FIG. 4

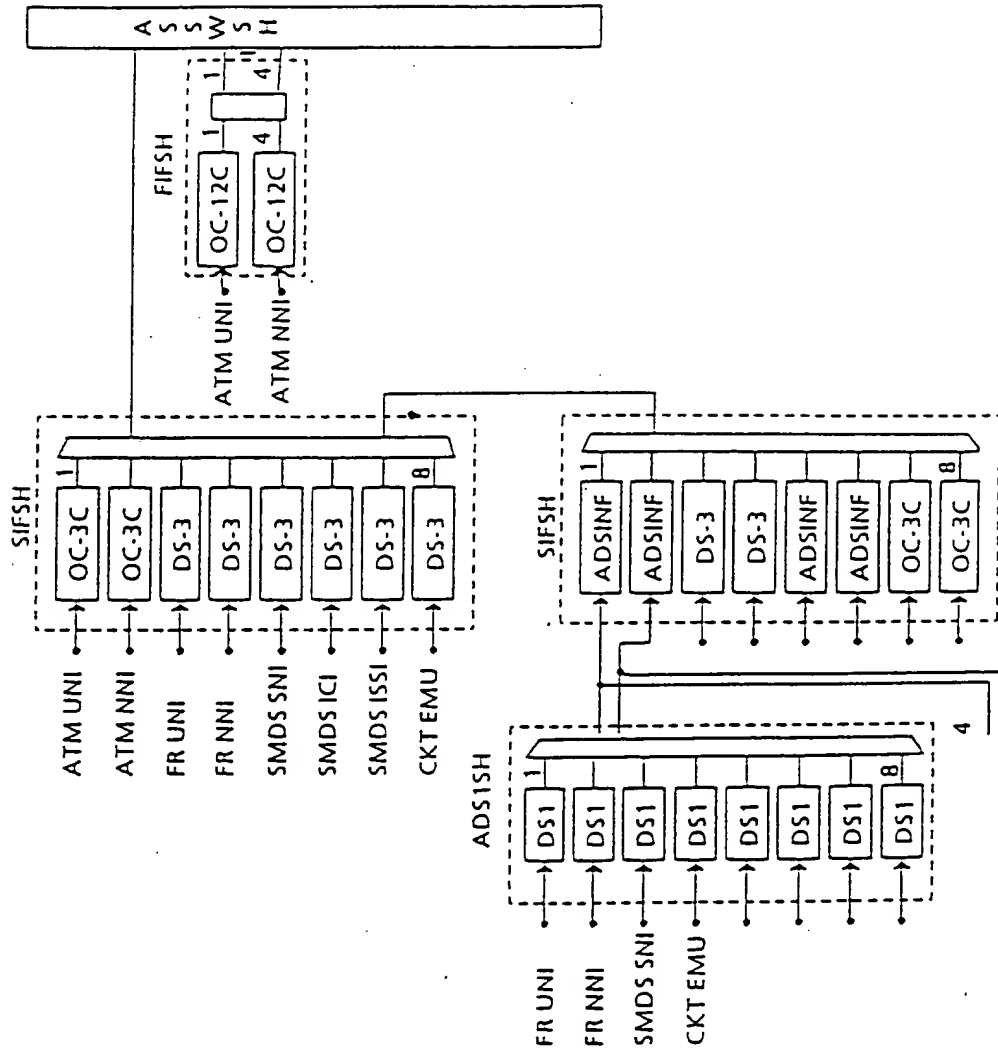


FIG. 5

APPROVED	O.G. #10.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

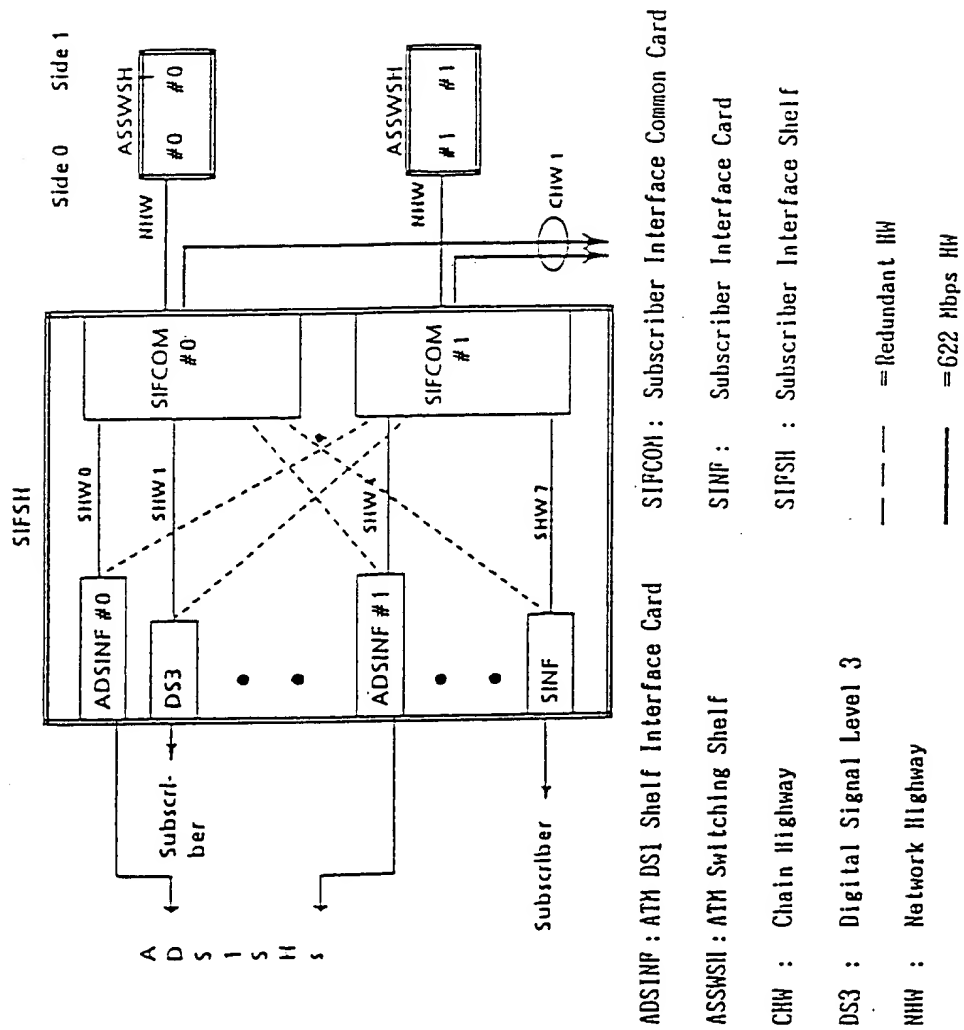
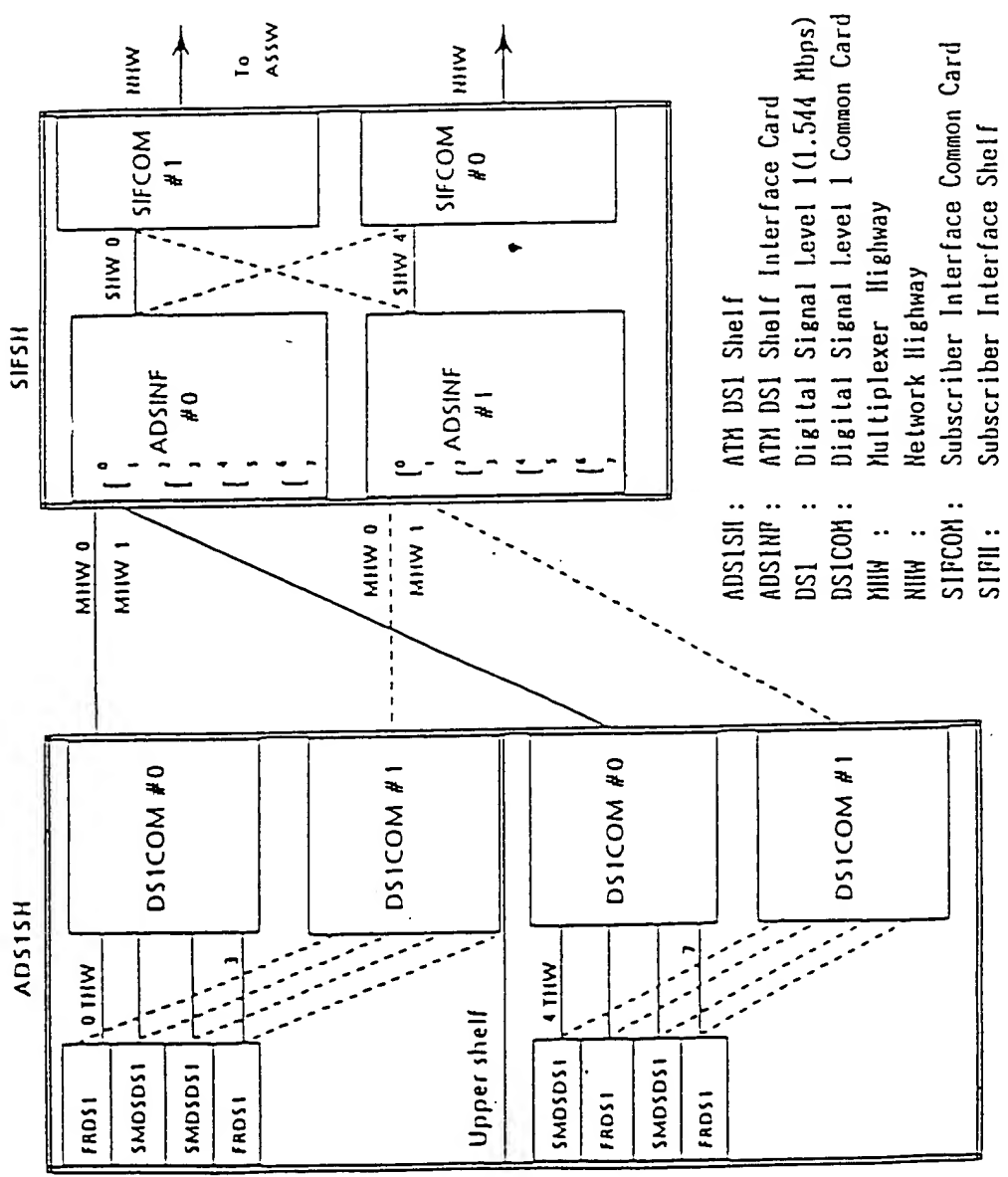


FIG. 6

66960-012200



_____ = 622 Mbps NIW

FIG. 7

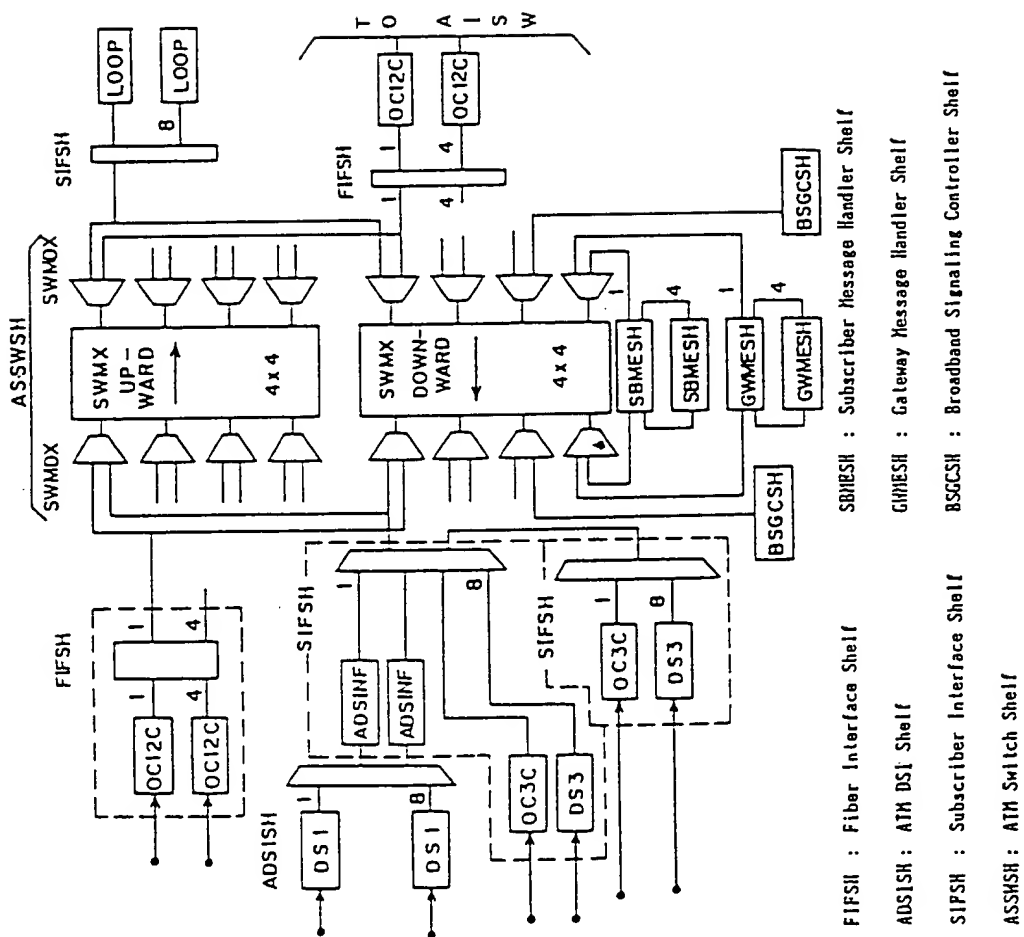


FIG. 8

66960-01-0000

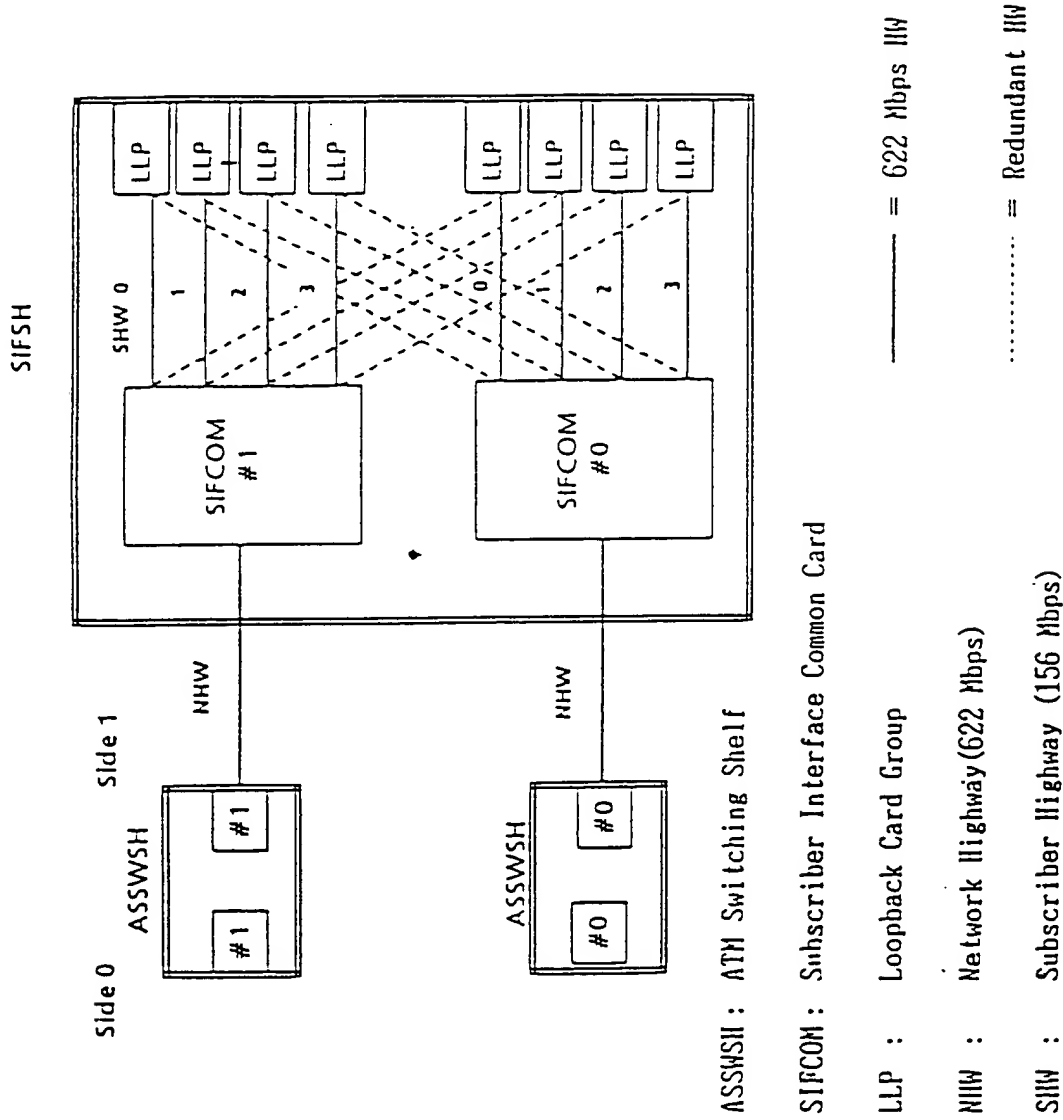


FIG. 9

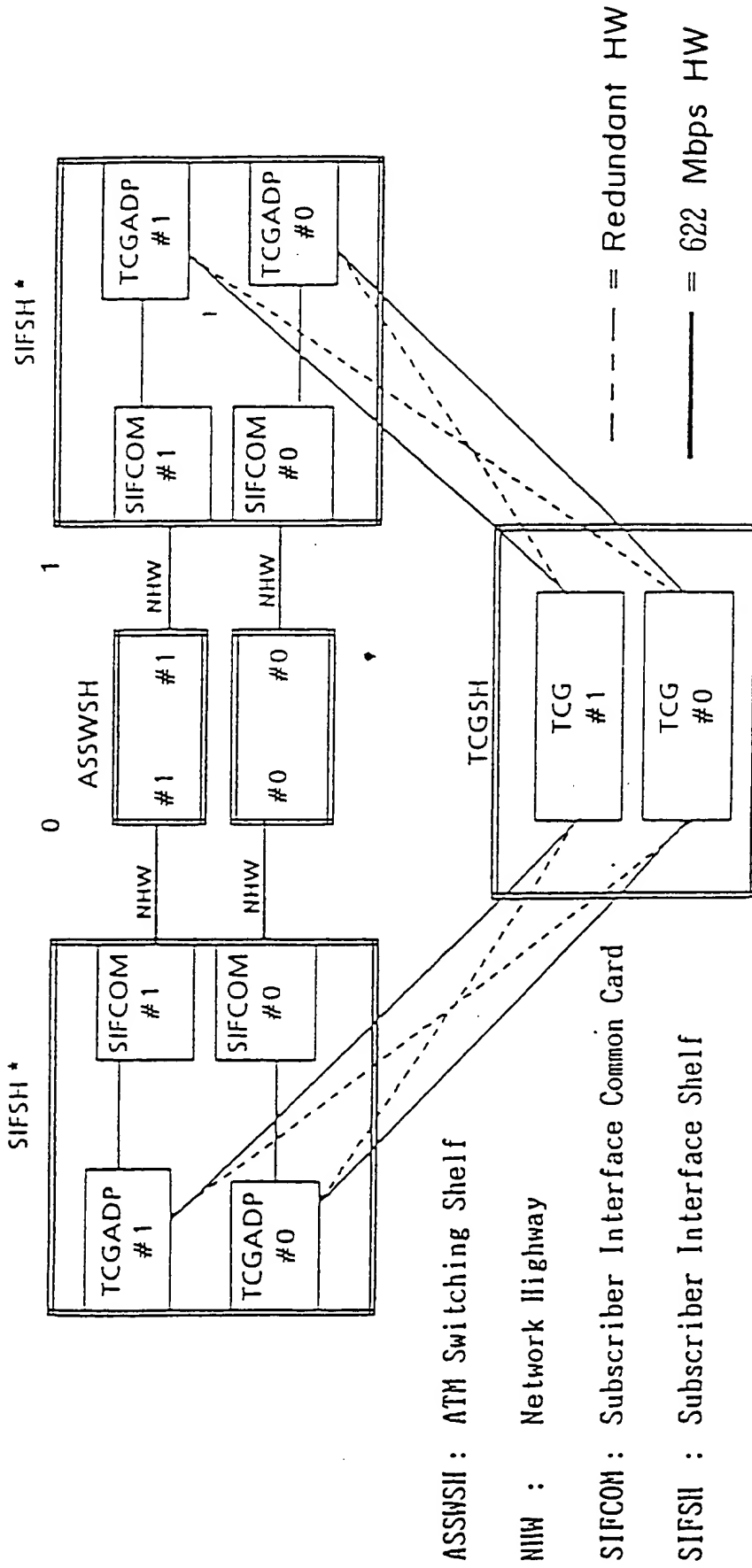


FIG. 10

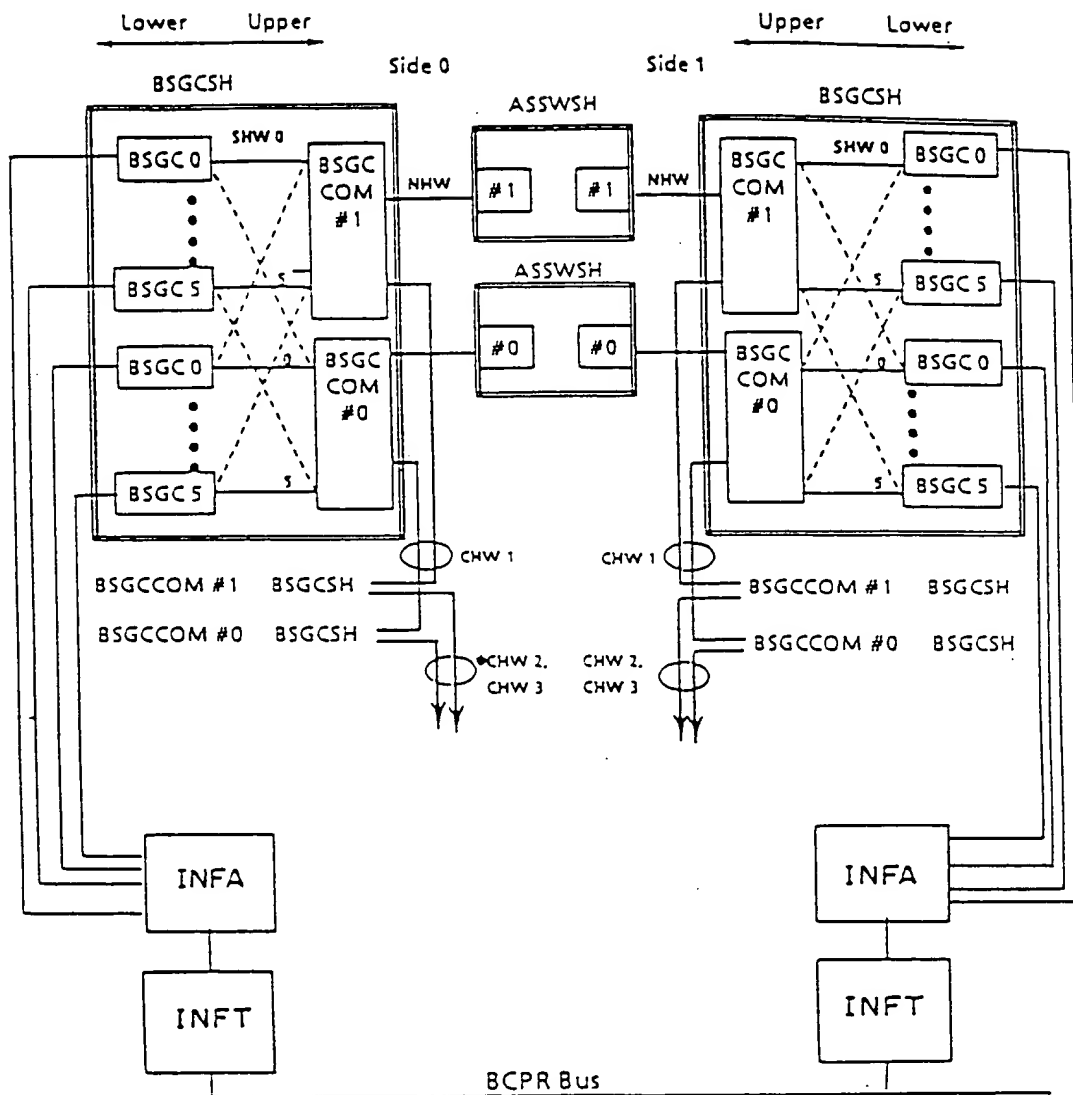


FIG. 11

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

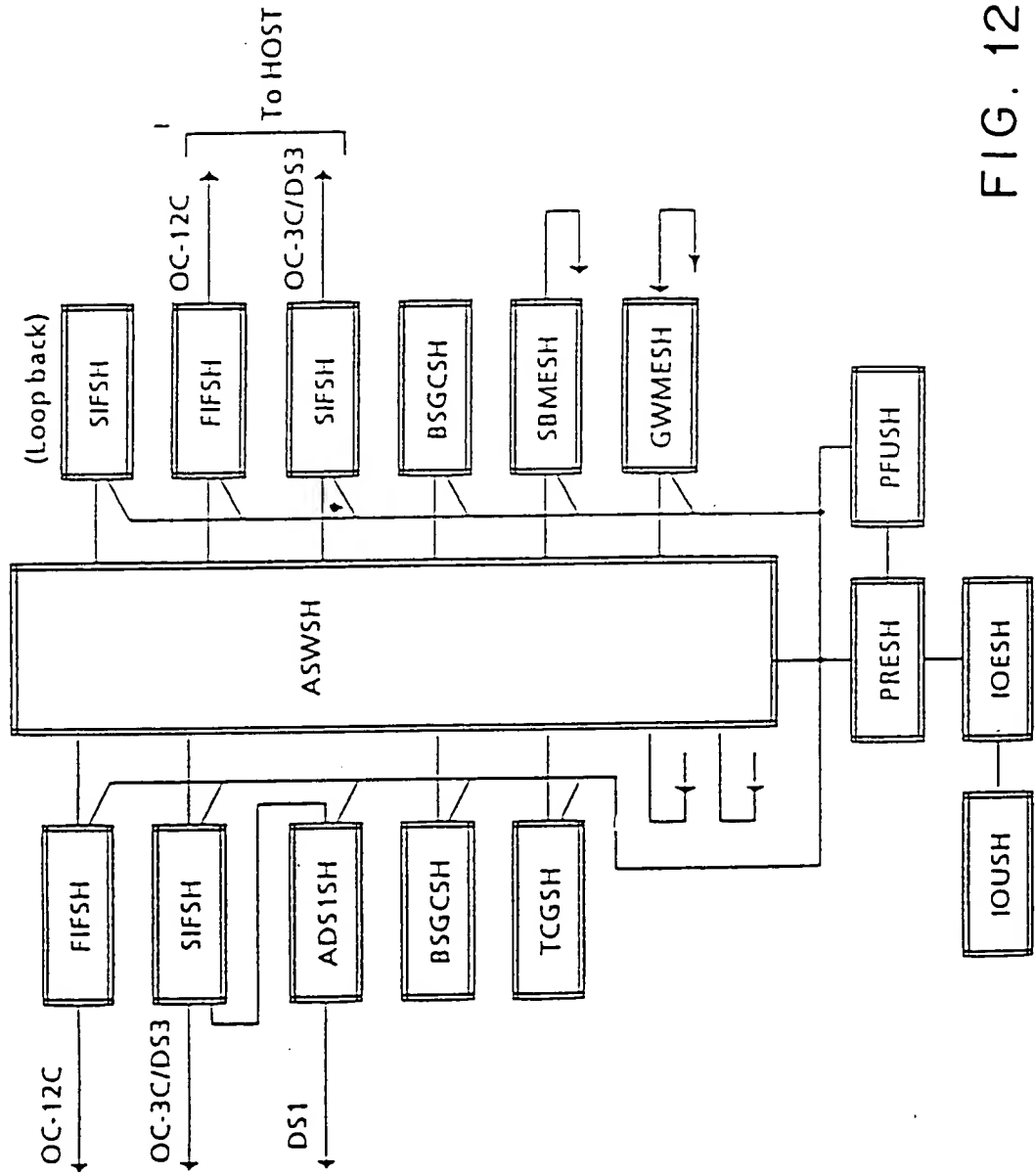
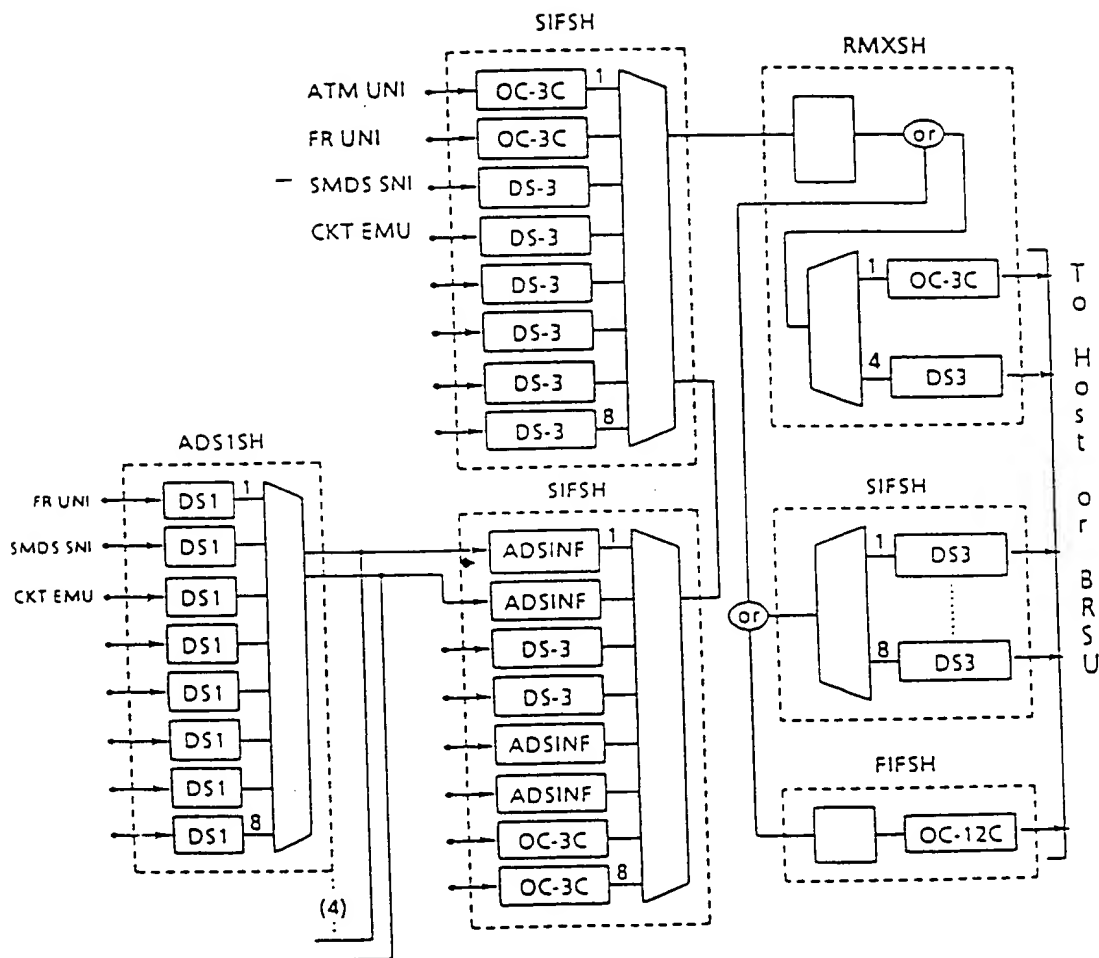


FIG. 12



SIFSH Subscriber Interface Shelf
 ADS1SH ATM DS1 Shelf
 FIFSH Fiber Interface Shelf
 RMXSH Remote Multiplex Shelf

FIG. 14

669260-PT2260

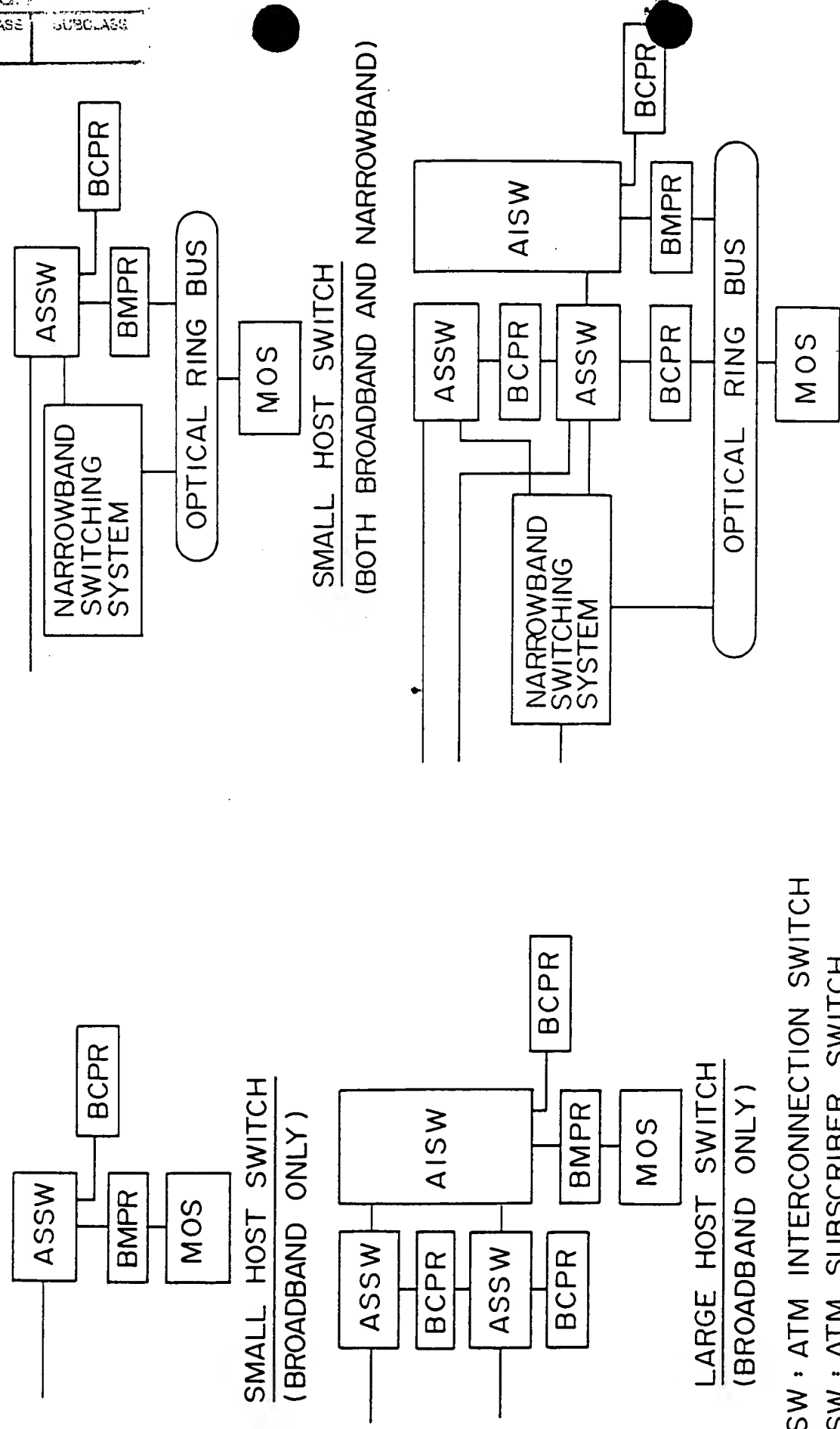
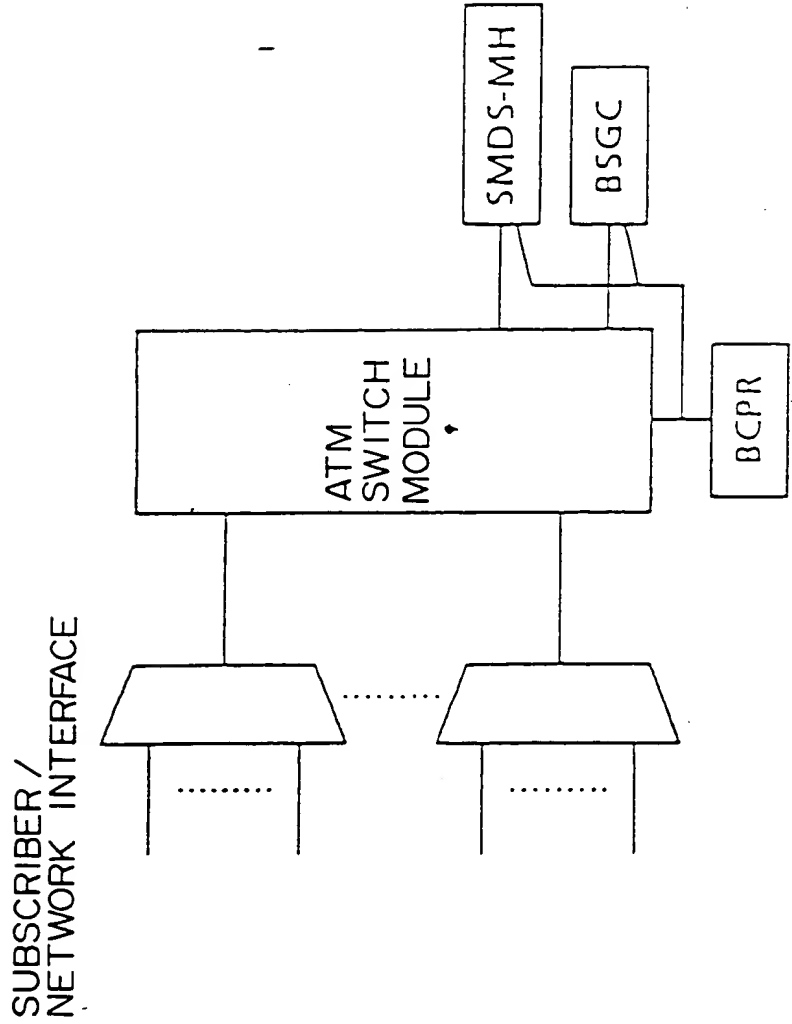


FIG. 15



- ASM : ATM SWITCH MODULE
- BCPR : BROADBAND CALL PROCESSOR
- BSGC : BROADBAND SIGNALING CONTROLLER
- SMDS-MH : SMDS MESSAGE HANDLER

FIG. 16

669320-22220

APPROVED	O.G. F12.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

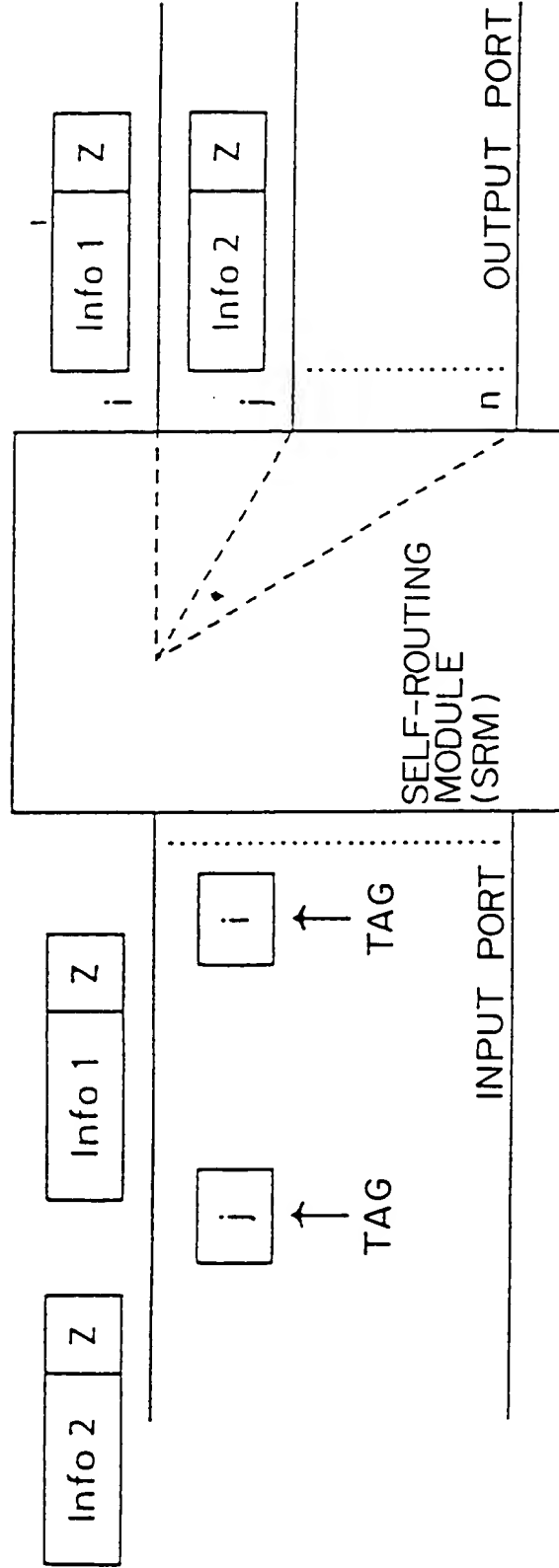


FIG. 17

66920-72260

APPROVED	O.C. FIG.
BY	02507 000000
DRAFTSMAN	

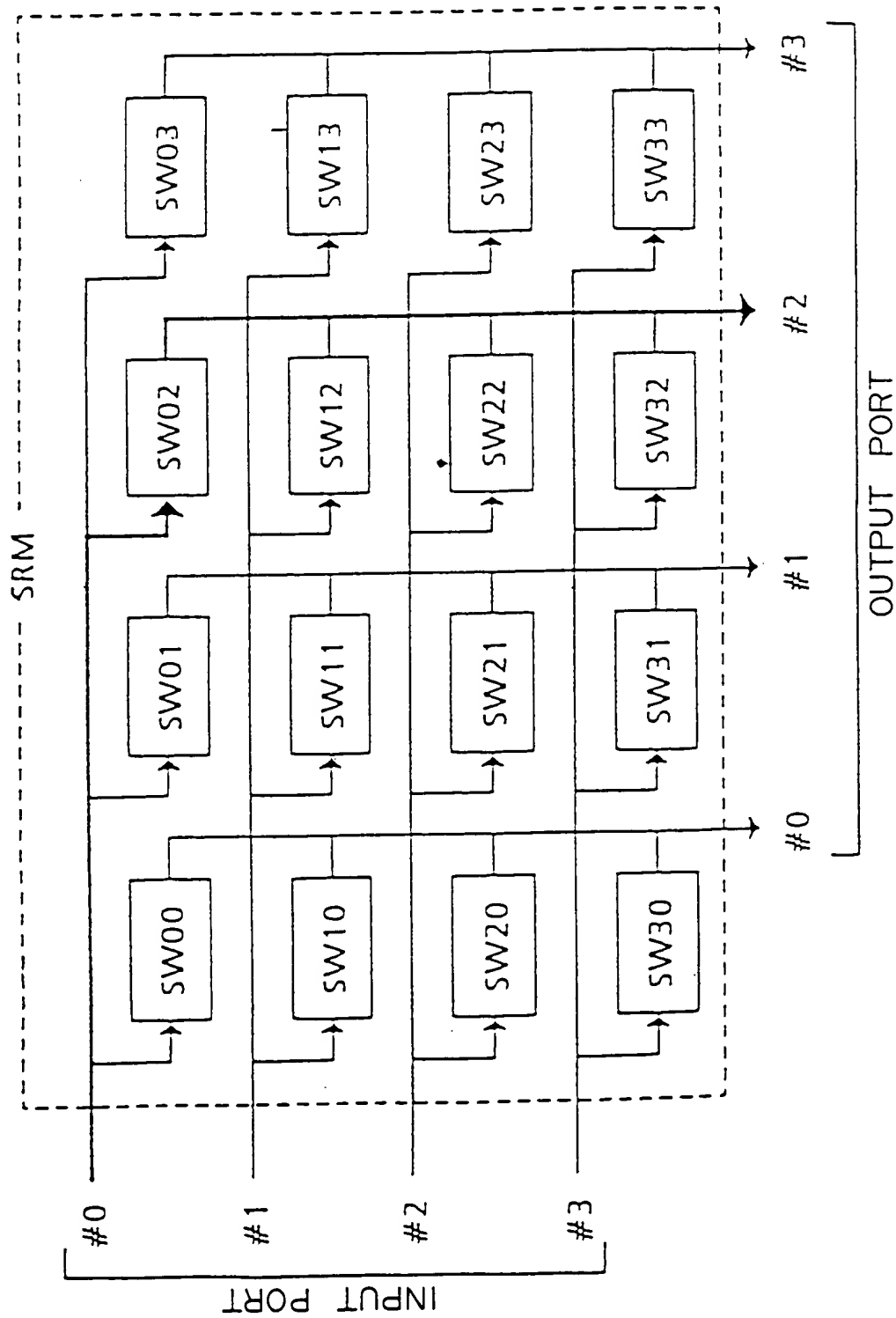


FIG. 18

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DATE		

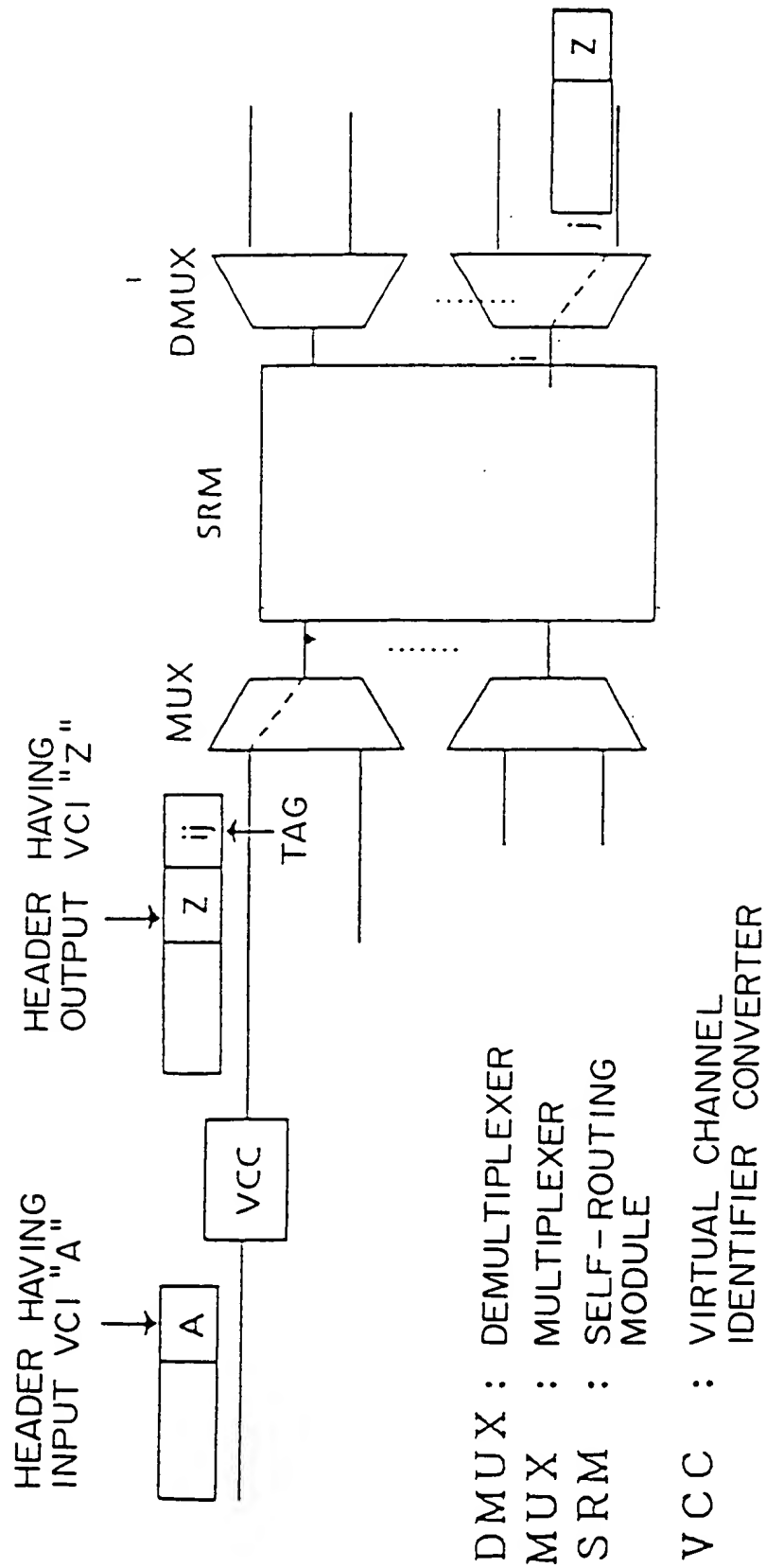


FIG. 19

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

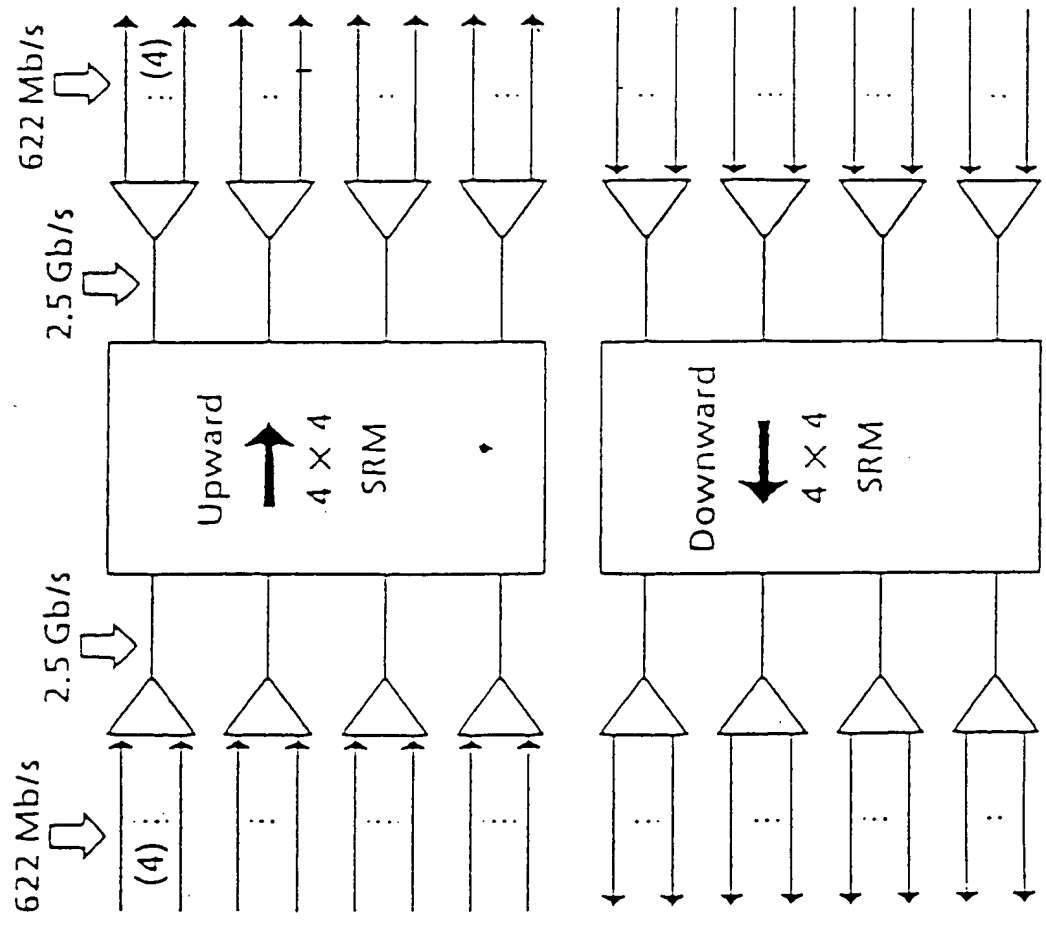


FIG. 20

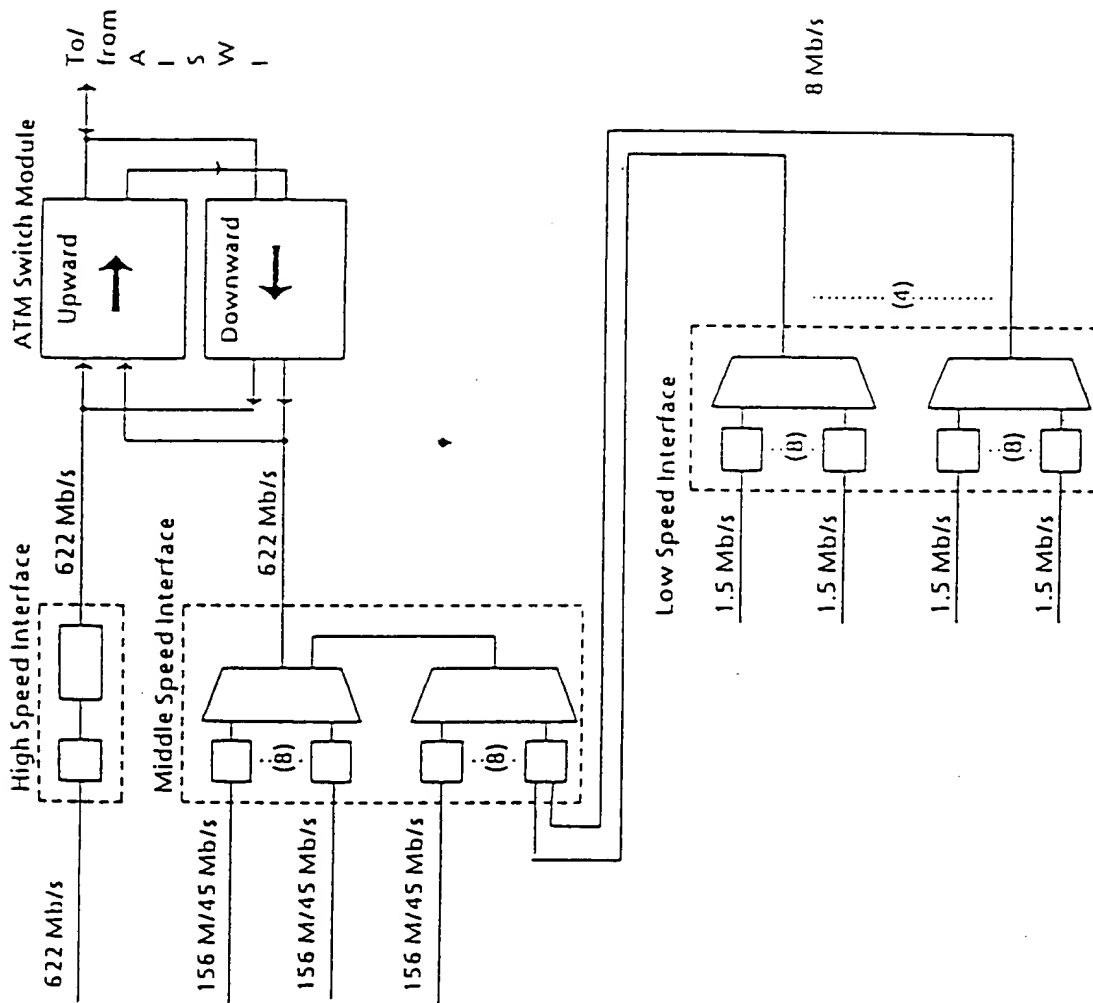
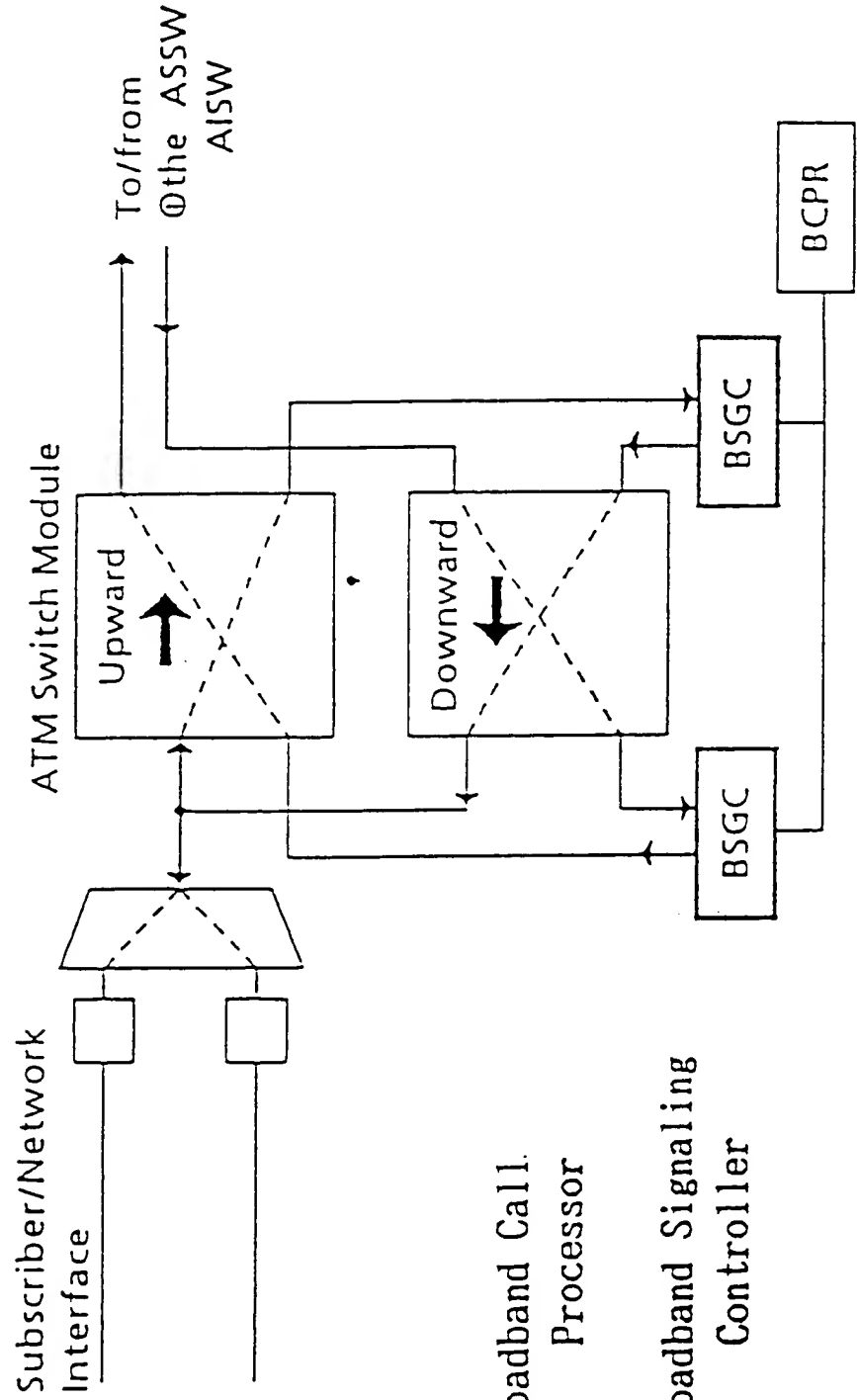


FIG. 21

66920-ET2260

APPROVED	O.G. P. 2.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



BCPR : Broadband Call Processor

BSGC : Broadband Signaling Controller

FIG. 22

APPROVED	O.G. FMS	
BY	CLASS	SUBCLASS
DRAFTSMAN		

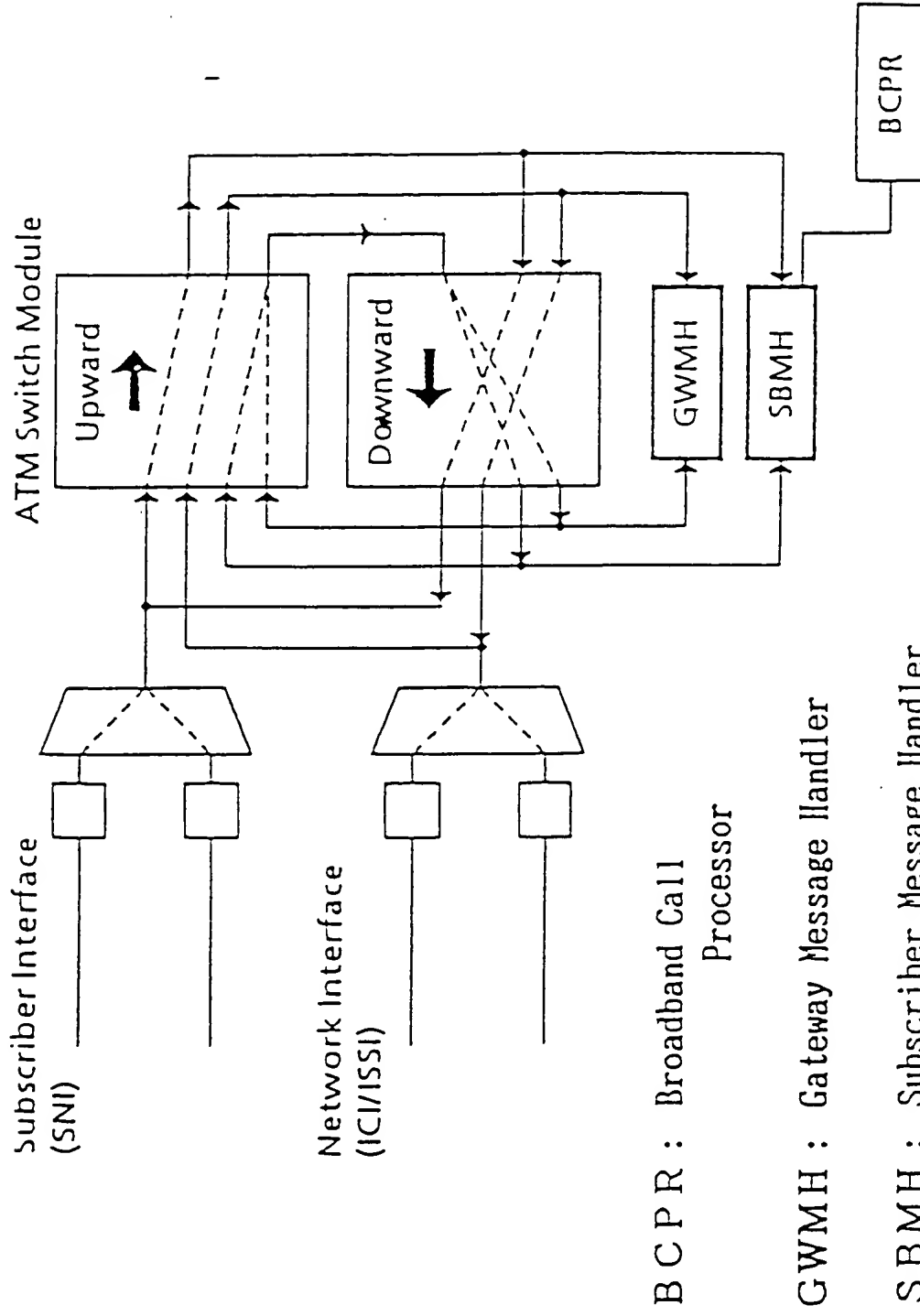
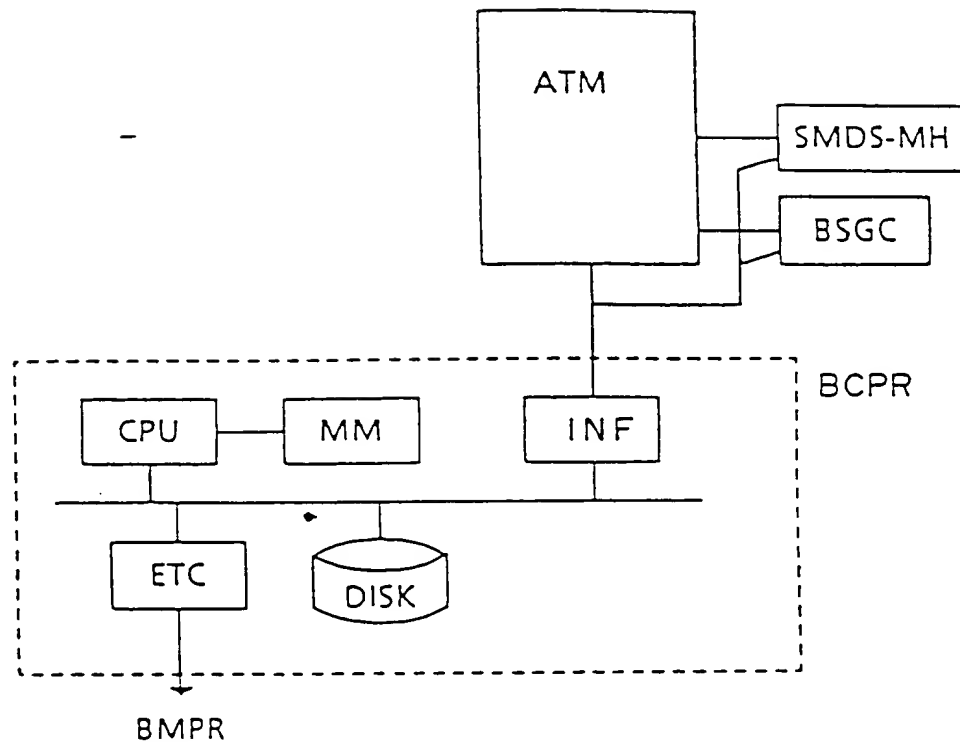


FIG. 23



BCPR : Broadband Call Processor

BMPR : Broadband Main Processor

BSGC : Broadband Signaling Controller

CPU : Central Processing Unit

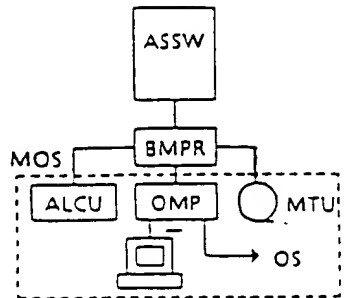
ETC : Ethernet Controller

MM : Main Memory

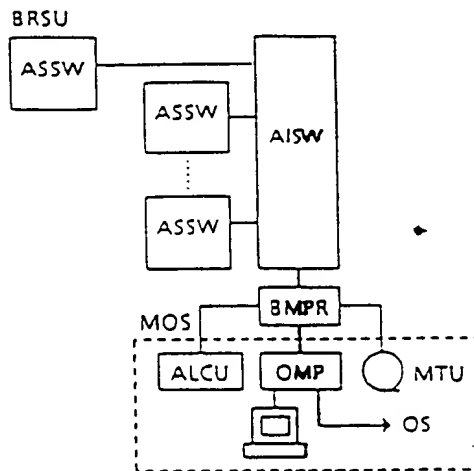
INF : Interface

SMDS-MH : SMDS Message Handler

FIG. 24



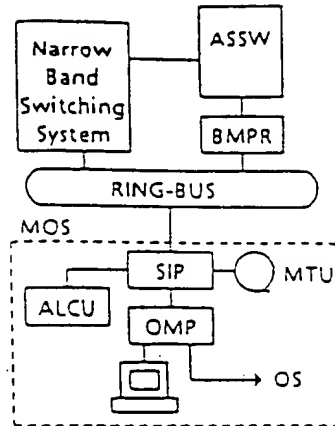
<Small Host: Broadband only>



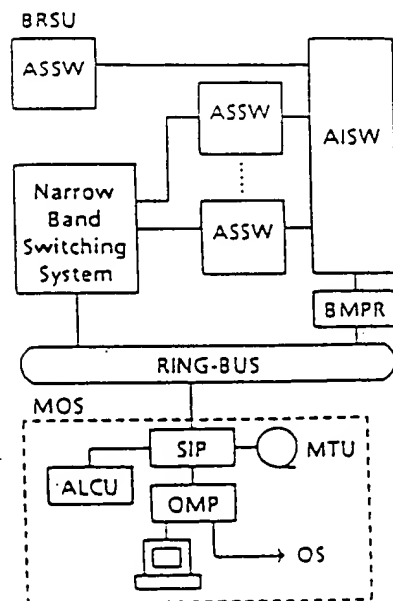
<Large Host: Broadband only>

Legend

ISW : ATM Interconnection Switch
 ALCU : Alarm Control Unit
 ASSW : ATM Subscriber Switch
 BMPR : Broadband Main Processor
 BRSU : Broadband Remote Switching Unit
 MTU : Magnetic Tape Unit
 MOS : Maintenance and Operation Subsystem
 SIP : System Integration Processor
 OMP : Operation and Maintenance Processor
 OS : Operations System



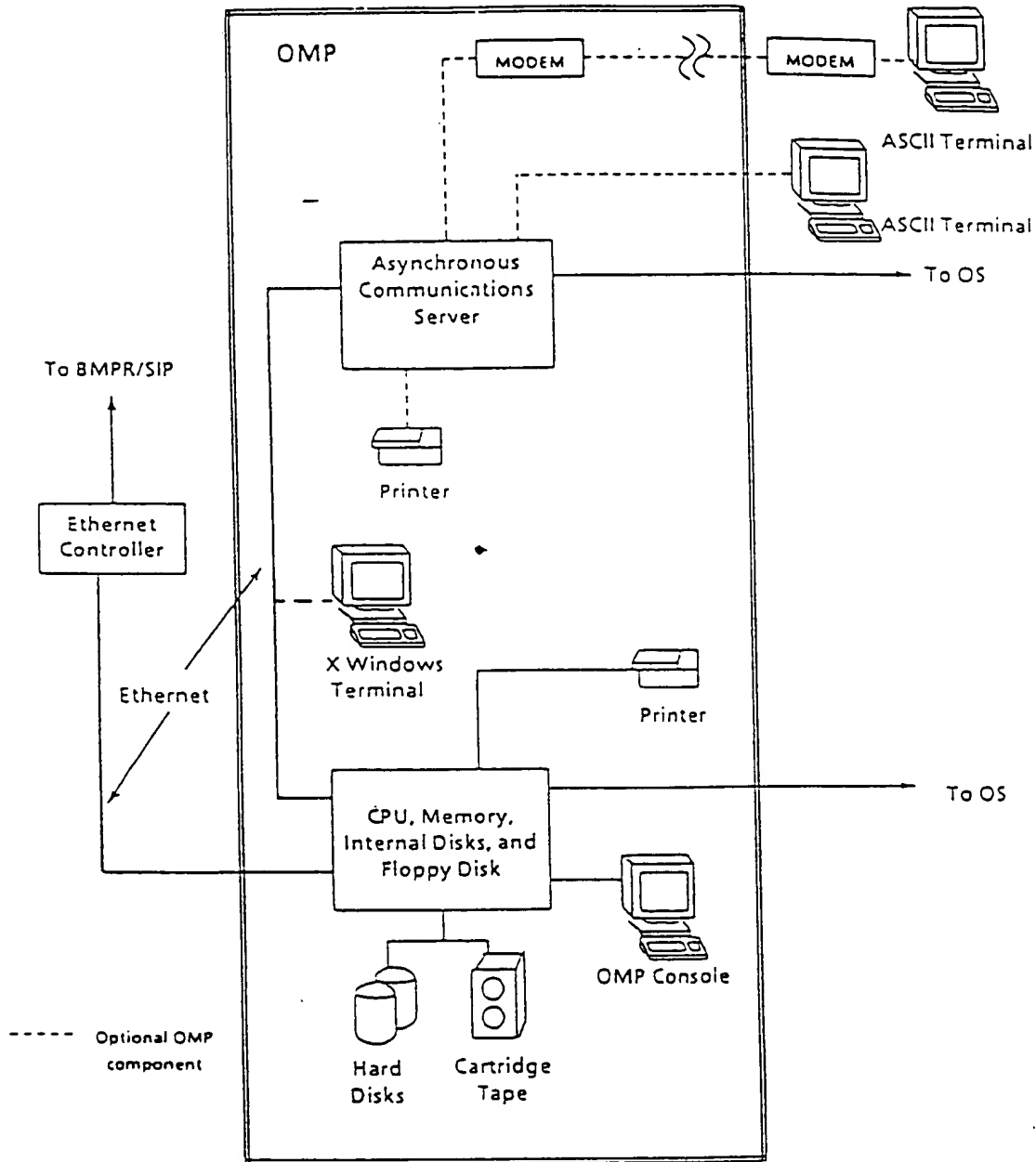
<Small Host with Narrow band>



<Large Host with Narrow band>

FIG. 25

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



BMPR : Broadband Main Processor

OS : Operations Support System

SIP : Systems Integration Processor

FIG. 26

66920-ET22200

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

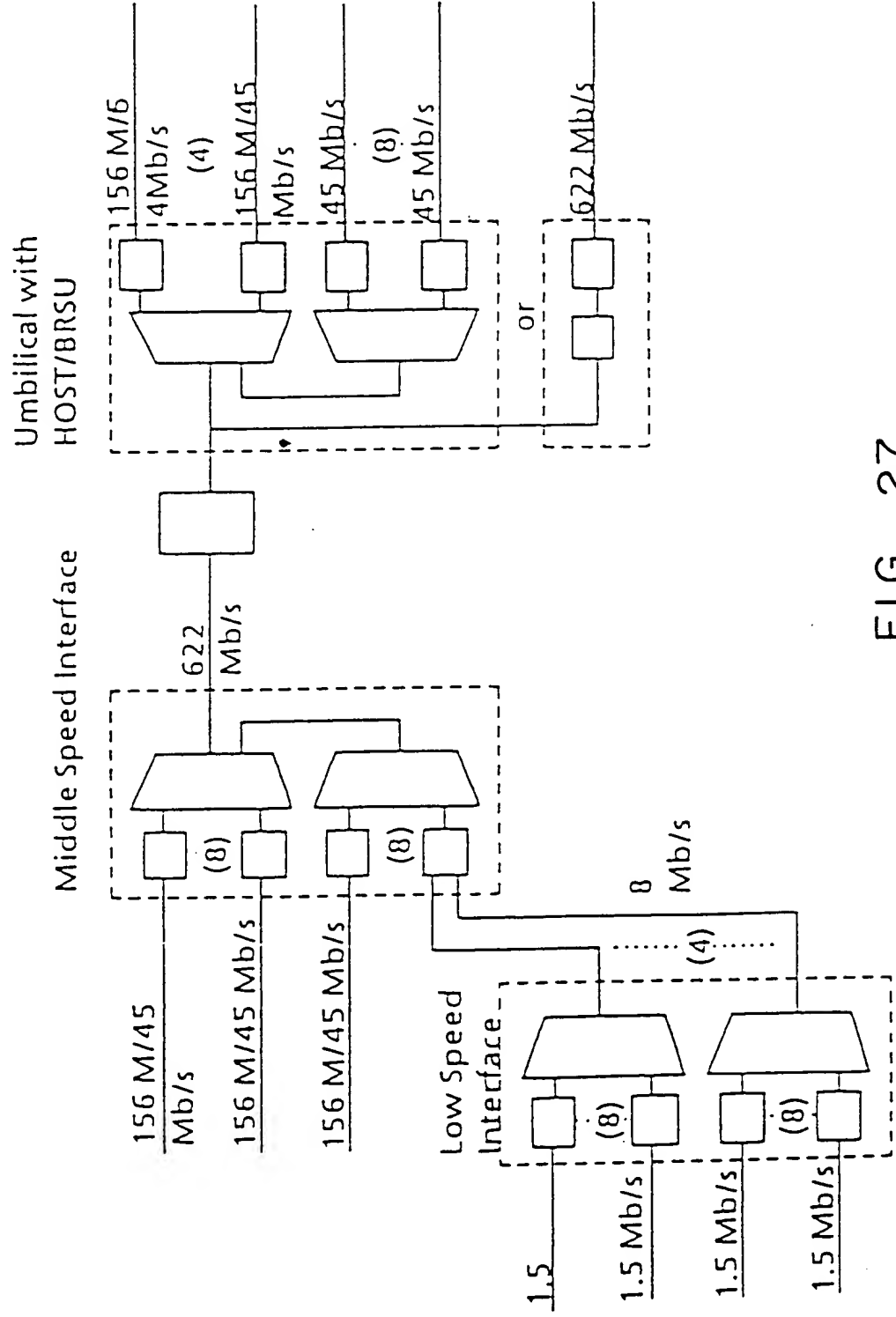
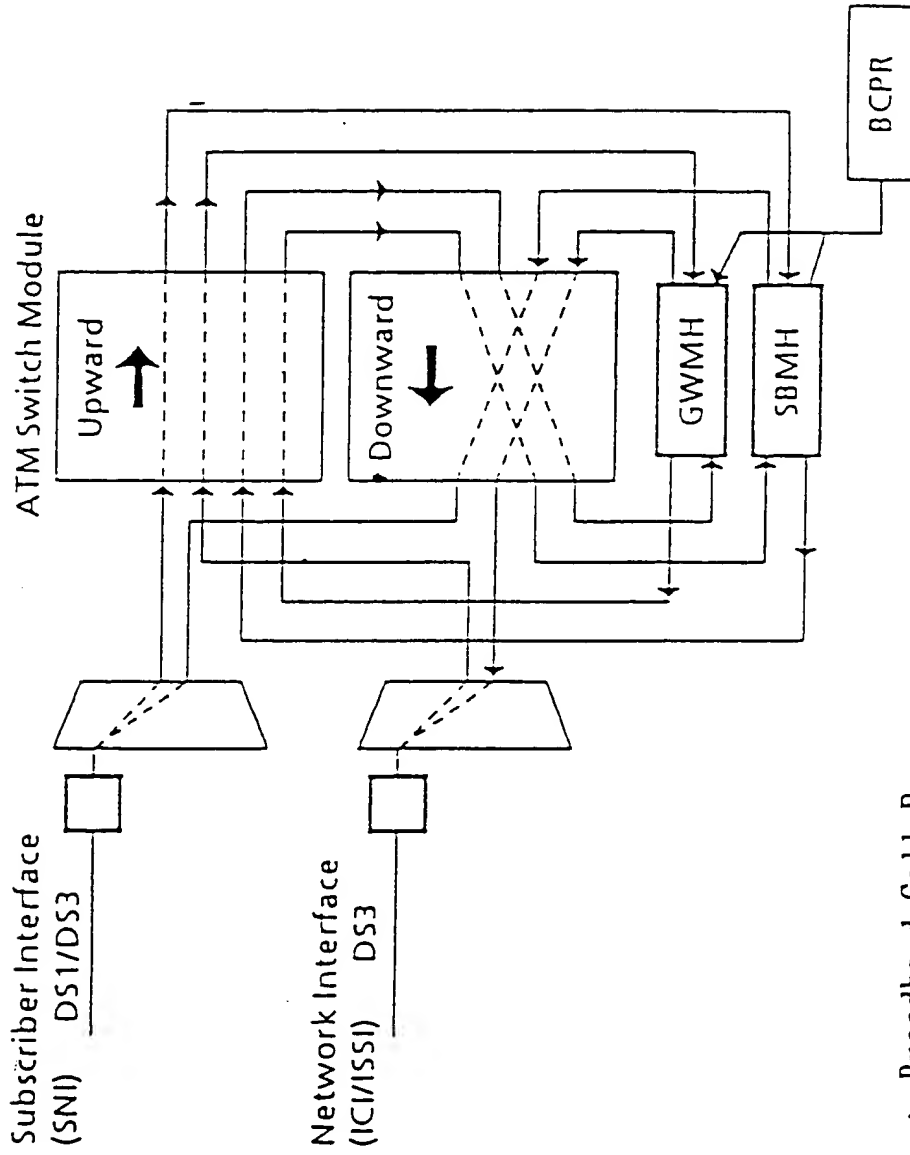


FIG. 27

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



BCPR : Broadband Call Processor
GWMH : Gateway Message Handler
SBMH : Subscriber Message Handler

FIG. 29

663220-ET34220

669226-2

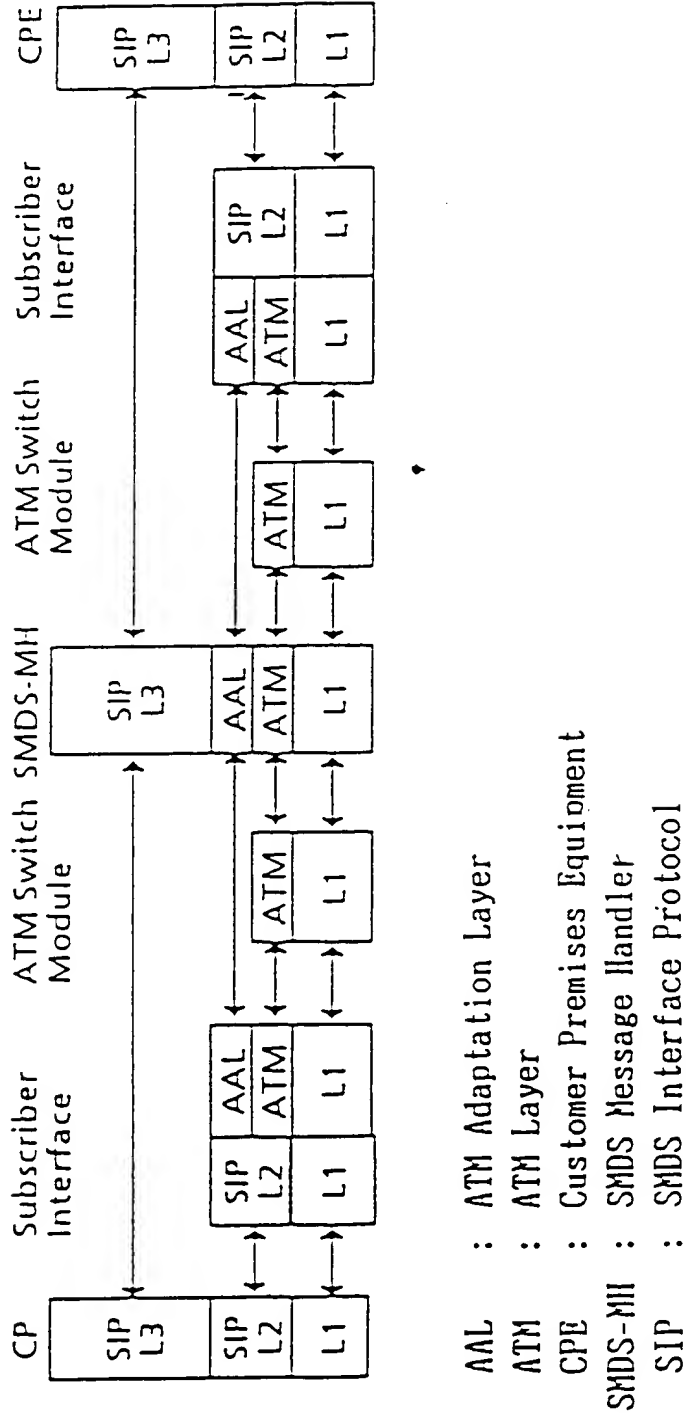
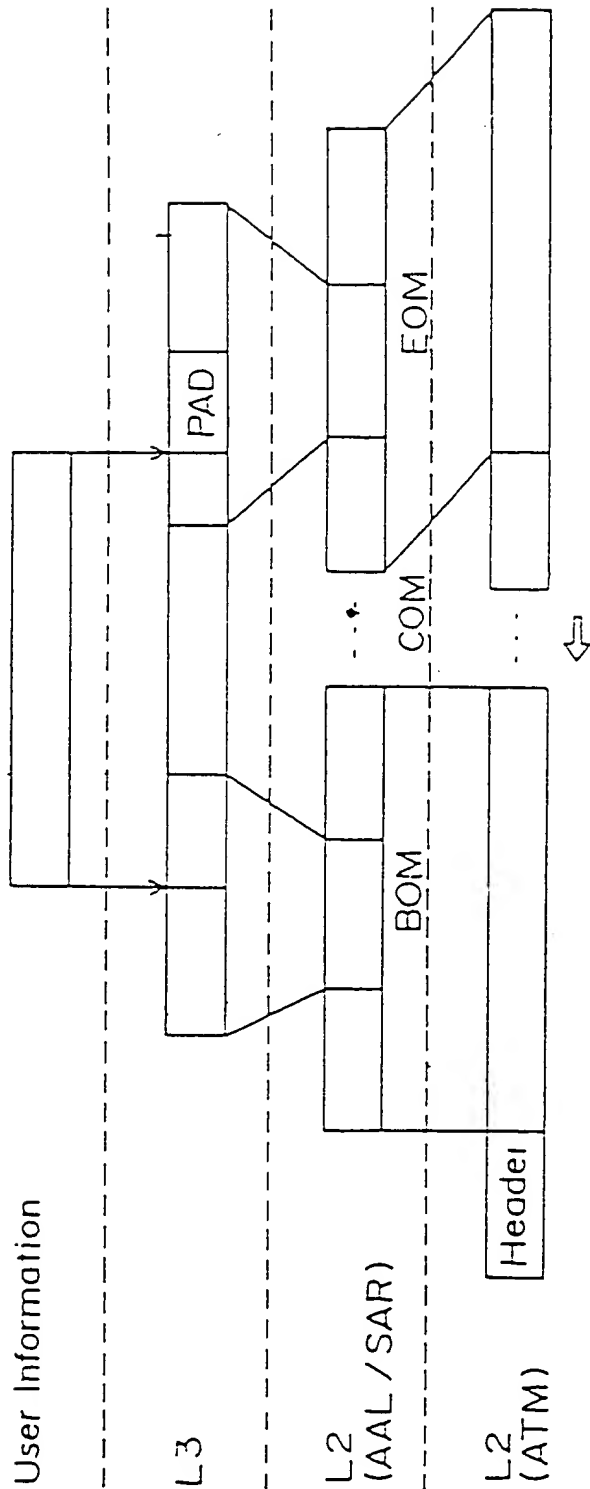


FIG. 30

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



BOM : Beginning of Message
 COM : Continuation of Message
 EOM : End of Message
 SAR : Segmentation and Re-assembly

FIG. 31

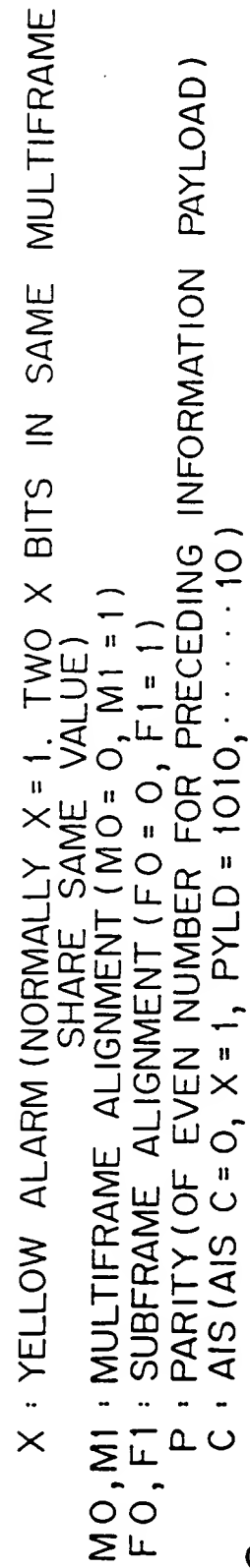
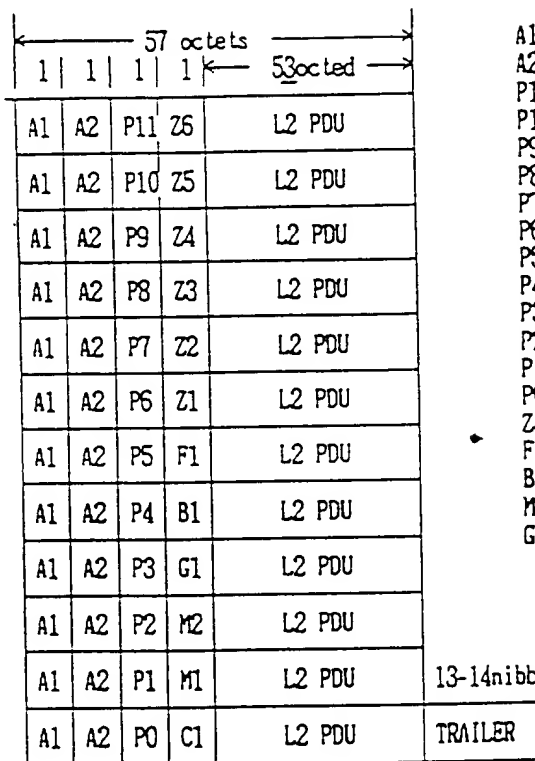


FIG. 36



A1 : Framing octet (11110110)
 A2 : Framing octet (00101000)
 P11 : Path Overhead Identifier octet (00101100)
 P10 : Path Overhead Identifier octet (00101001)
 P9 : Path Overhead Identifier octet (00100101)
 P8 : Path Overhead Identifier octet (00100000)
 P7 : Path Overhead Identifier octet (00011100)
 P6 : Path Overhead Identifier octet (00011001)
 P5 : Path Overhead Identifier octet (00010101)
 P4 : Path Overhead Identifier octet (00010000)
 P3 : Path Overhead Identifier octet (00001101)
 P2 : Path Overhead Identifier octet (00001000)
 P1 : Path Overhead Identifier octet (00000100)
 P0 : Path Overhead Identifier octet (00000001)
 Z4-0 : Growth octet (default 00000000)
 F1 : PLCP Path User Channel (default 00000000)
 B1 : Bit Interleaved Parity-8 (even parity)
 M2-1 : SIP Level 1 Control Information
 G1 : PLCP Path Status

FEBE	YEL.SIG.	LSS
------	----------	-----

FEBE : Far End Block Error
 YEL.SIG : Yellow Signal (normal 0)
 LSS : Link Status Signal

LSS	Link Status	Incoming SIG/LSS
000	connected	connected
000	connected	rx link up
110	rx link up	rx link dn
110	rx link up	PLCP Out-Of-Frame
011	rx link dn	PLCP Loss-Of-Frame

C1 : Cycle/Stuff Counter
 TRAILER : Trailer Nibble (1100)

C1 Code	Frame in Cycle	Trailer Length
11111111	1	13 nibbles
00000000	2	14 nibbles
01100110	3 (no stuff)	13 nibbles
10011001	4 (stuff)	14 nibbles

FIG. 37

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

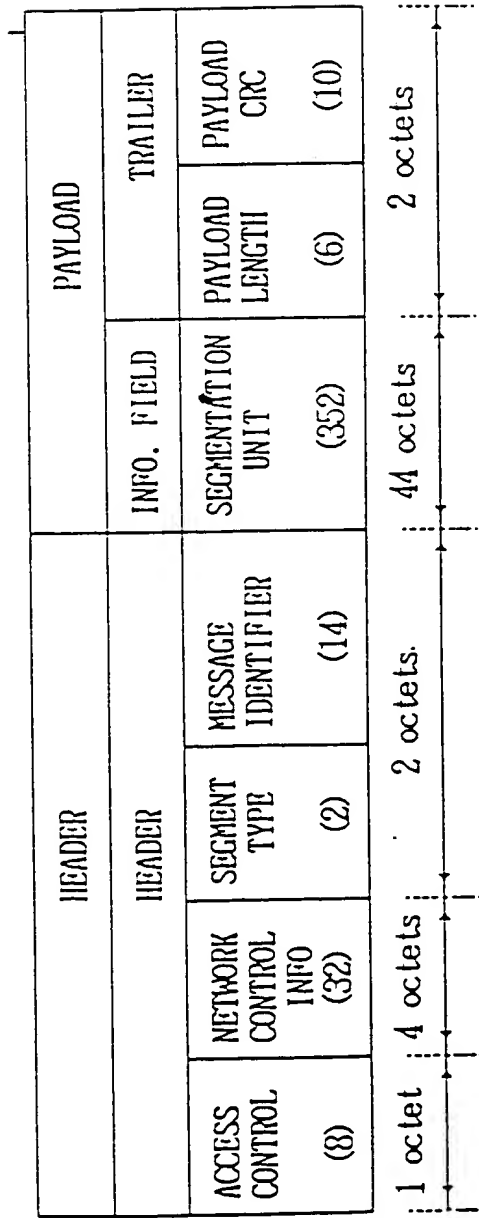


FIG. 38

66930-012260

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

DIR.	SNI	NNI																
UP	<table><tr><td>BUSY</td><td>X</td><td>X</td><td>X</td><td>X</td><td>REQ2</td><td>REQ1</td><td>REQ0</td></tr></table> <p>BUSY : CONTAIN INFORMATION =1, EMPTY =0 REQ2 : PRIORITY LEVEL 2 REQ1 : PRIORITY LEVEL 1 REQ0 : PRIORITY LEVEL 0 REQUEST FOR SEND = 0, NO REQUEST =1 X : NOT PROCESSED BY THE NETWORK</p>	BUSY	X	X	X	X	REQ2	REQ1	REQ0	<table><tr><td>BUSY</td><td>DC</td><td>DC</td><td>DC</td><td>DC</td><td>DC</td><td>DC</td><td>DC</td></tr></table> <p>BUSY : VALID CELL = 1, INVALID CELL =0 DC : DON'T CARE</p>	BUSY	DC	DC	DC	DC	DC	DC	DC
BUSY	X	X	X	X	REQ2	REQ1	REQ0											
BUSY	DC	DC	DC	DC	DC	DC	DC											
DOWN	<table><tr><td>BUSY</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> <p>BUSY : CONTAIN INFORMATION =1, EMPTY =0</p>	BUSY	0	0	0	0	0	0	0	<table><tr><td>BUSY</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> <p>BUSY : VALID CELL = 1, INVALID CELL= 0</p>	BUSY	0	0	0	0	0	0	0
BUSY	0	0	0	0	0	0	0											
BUSY	0	0	0	0	0	0	0											

FIG. 39

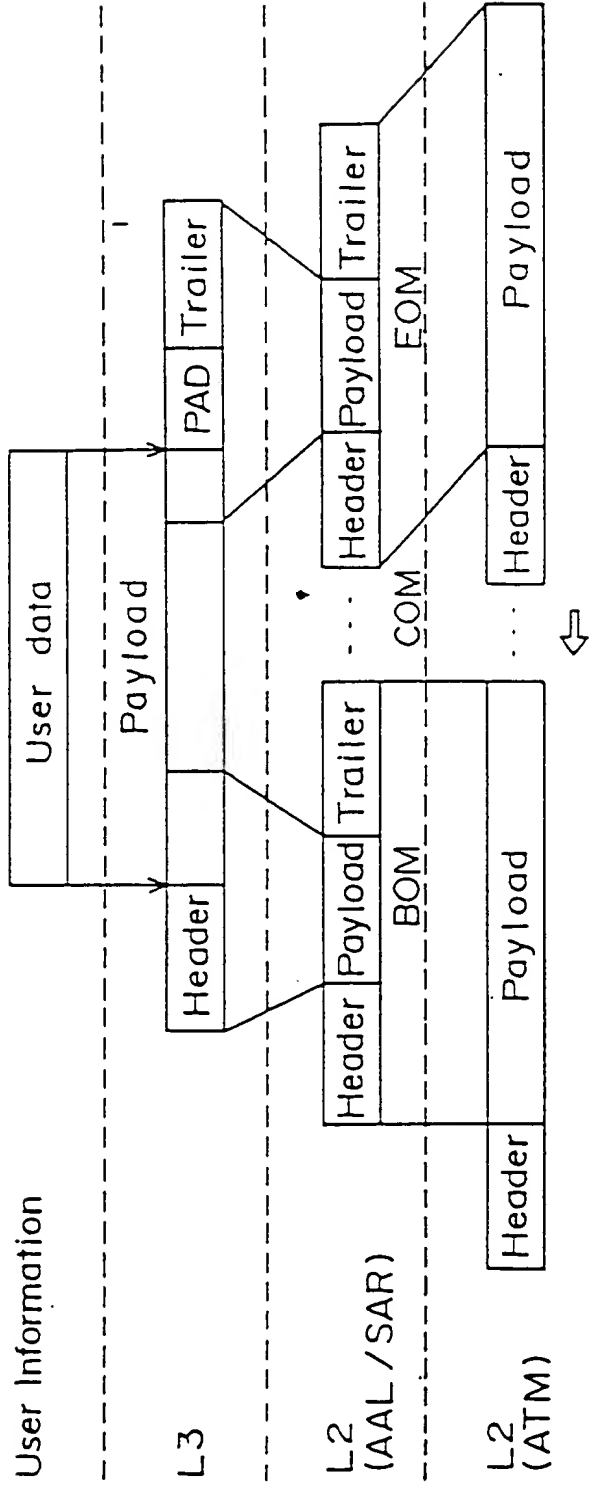
APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

	VCI	PT	SP	IICS
IF L2 PDU CONTAINS INFORMATION DATA	11111111 11111111 1111 1111	00	00	00100010
IF L2 PDU CONTAINS NO INFORMATION DATA	00000000 00000000 0000 0000	00	00	00000000

FIG. 40

00920 ET 2260

APPROVED	O.G. FIG	
BY	CLASS	SUBCLASS
DRAFTSMAN		



BOM : Beginning of Message
COM : Continuation of Message
EOM : End of Message
SAR : Segmentation and Re-assembly

FIG. 42

66960" E F 2260

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

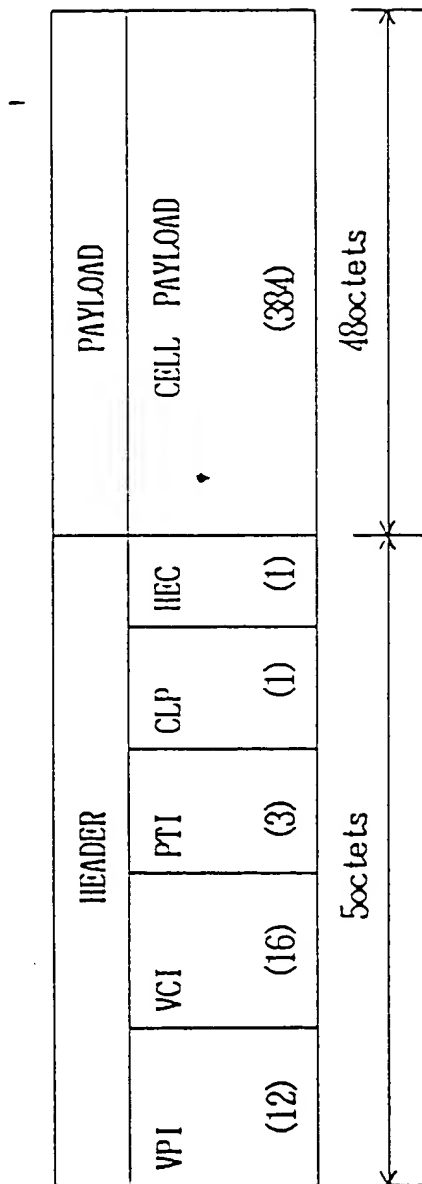


FIG. 43

6693ED*E7E22ED

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FUNCTION	VPI	VCI	PT	CLP
UNASSIGNED CELL	00000000 0000	0000 00000000 0000	XXX	0
ASSIGNED CELL	YYYYYYYY YYYY	YYYY YYYYYYYY YYYY	YYY	Y

X : NOT FIXED
Y : OPTIONAL

FIG. 44

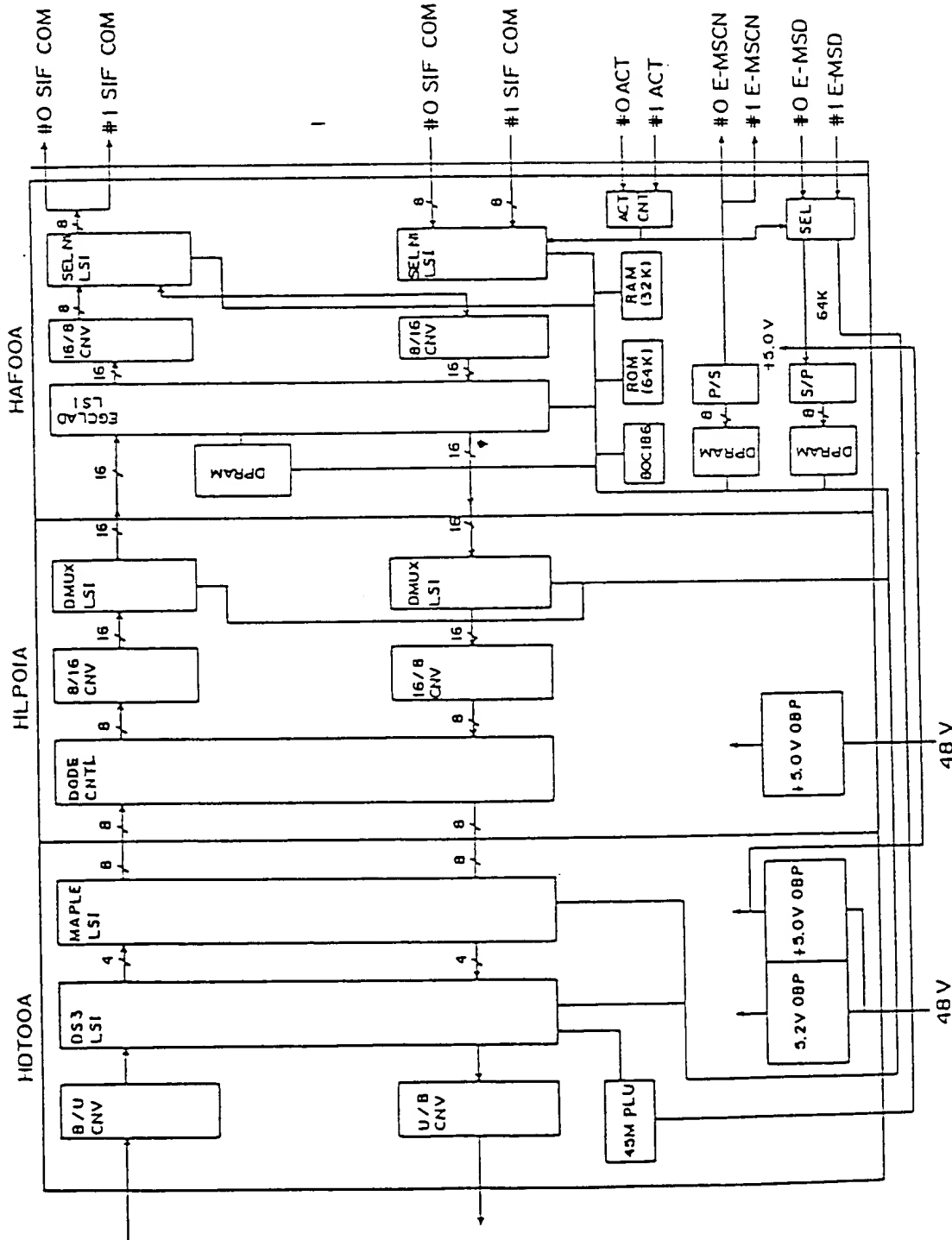


FIG. 45

66920-01-2260

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

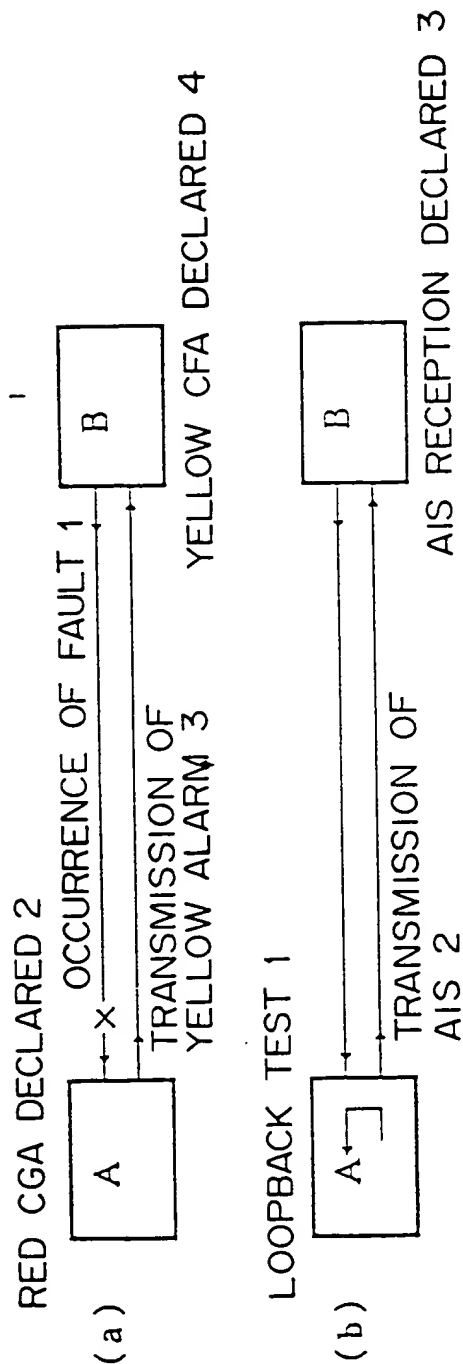


FIG. 46

APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FAULTY DETECTION	FAULT TO BE MASKED					
	LOS	AIS	OOF	YEL	POOF	PYEL
LOS	-	X	X	X	X	X
AIS		-	X	X	X	X
OOF			-	X	X	X
YEL	-			-		
POOF					-	X
PYEL						-

"X" INDICATES FAULT TO BE MASKED

POOF : PLCP OOF

PYEL : PLCP YELLOW SIGNAL

F I G. 4 7

669263-616/2260

66360-672200

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

	DETECTION CONDITION	RECOVERY CONDITION	REACTION
LOS OF SIGNAL	175±75 SEQUENCE OF 0 (NO PULSE)	AVERAGE PULSE DENSITY OF 33%	RED CGA DECLARED TRANSMISSION OF YELLOW ALARM
OUT-OF-FRAME (DS3)	THREE OR MORE ERRORS IN FRAME BITS OF 16 OR LESS IN SERIES	Framing bit pattern AND MATCHING OF CRC	RED CGA DECLARED TRANSMISSION OF YELLOW ALARM
AIS	C=0, X=1, INF0. PYLD=1010, ...10	VALUES OTHER THAN LEFT DATA	AIS DECLARED TRANSMISSION OF YELLOW ALARM
YELLOW ALARM (DS3)	X=0	X=1	YELLOW SIGNAL RECEPTION DECLARED

FIG. 48

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

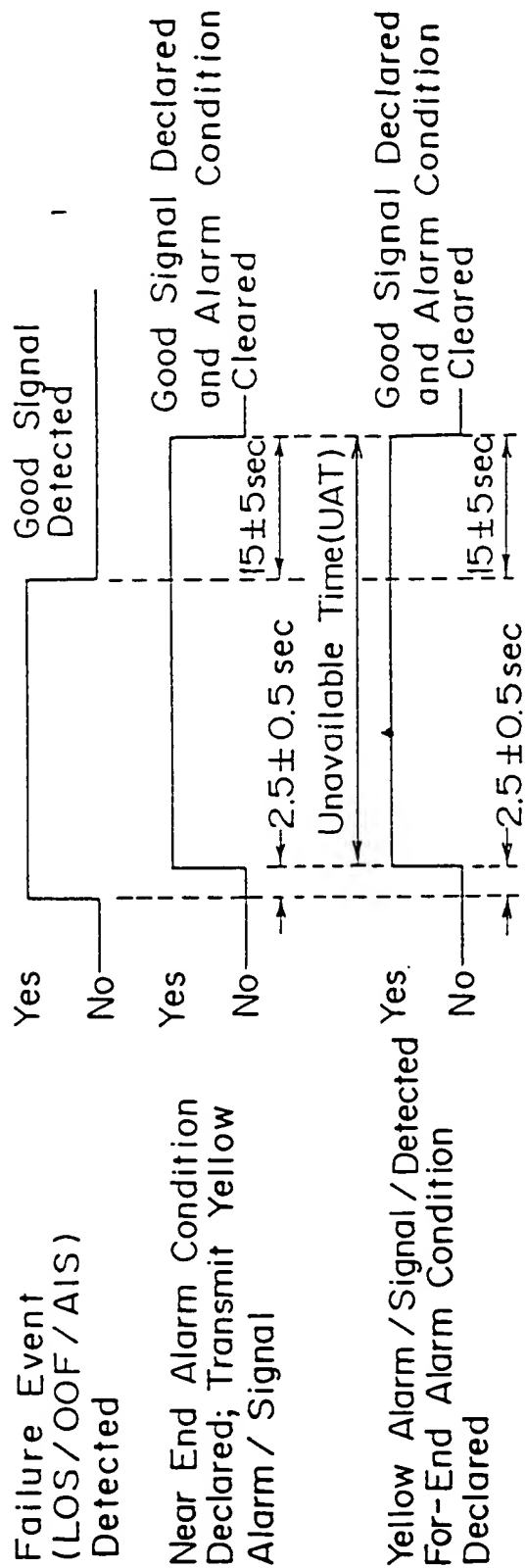


FIG. 49

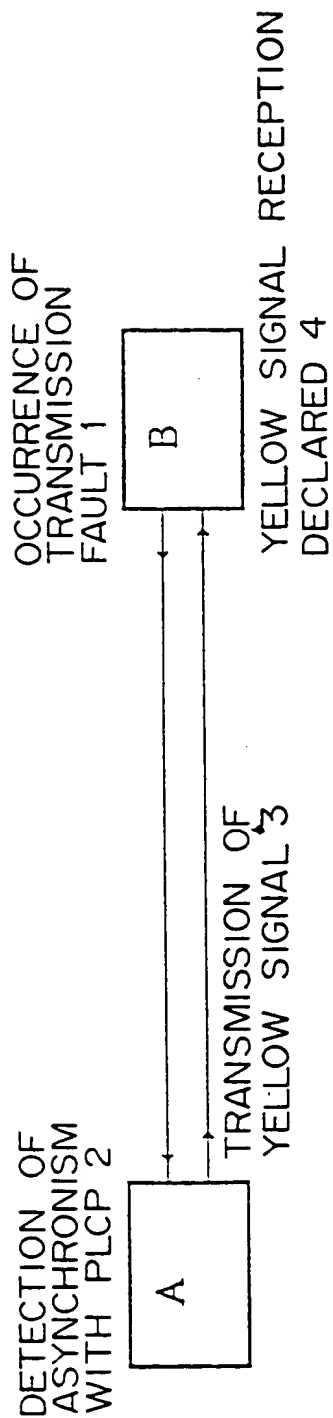


FIG. 50

665260-672260

APPROVED BY DRAFTSMAN	O.G. FIG.
CLASS	SUBCLASS

	DETECTION CONDITION	RECOVERY CONDITION	REACTION
OUT-OF-FRAME (DS3 PLCP)	A1 AND A2 DETECT REEOR OR PATH OVERHEAD IDENTIFIER DETECTS REKORS TWICE CONTINUOUSLY	MATCHING A1 AND A2, MATCHING PATH OVERHEAD IDENTIFIER	TRANSMISSION OF YELLOW SIGNAL
YELLOW SIGNAL (DS3 PLCP)	DETECTION OF "1" IN FIFTH G1 BIT.	DETECTION OF "0" IN FIFTH G1 BIT.	YELLOW SIGNAL RECEPTION DECLARED

FIG. 51

66920-ET2200

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

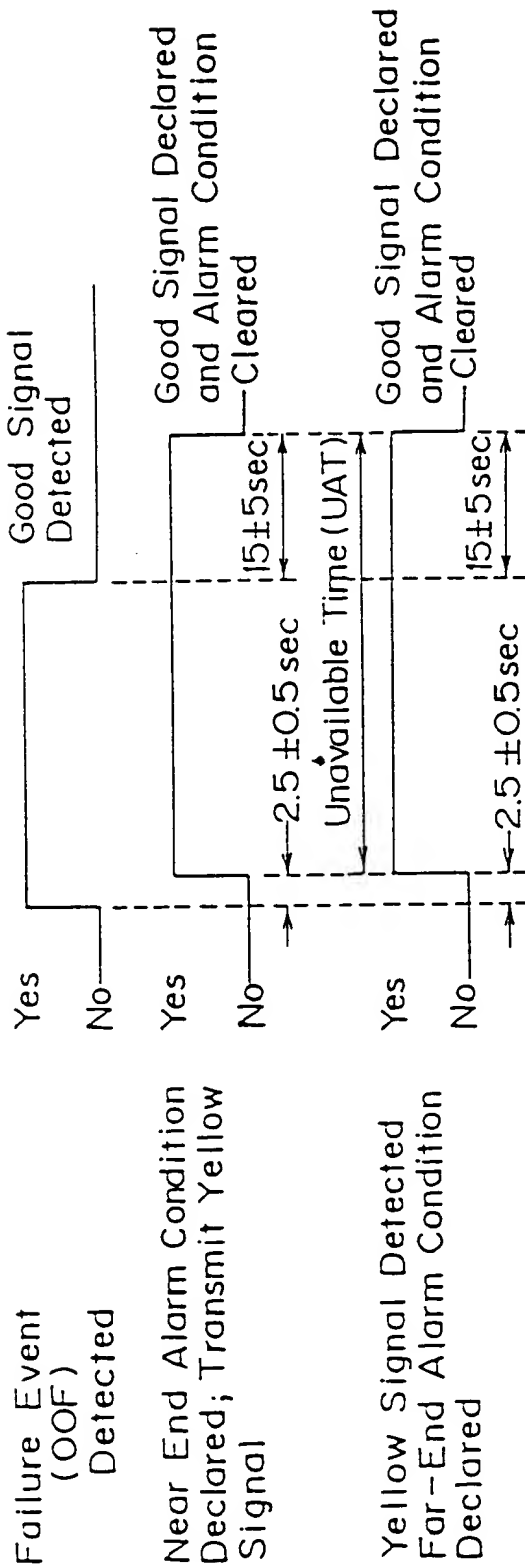


FIG. 52

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

Parameters	Normal counter Advance	Counter Advance During Failure Events and Conditions			
		LOS	OOF	AIS	UAT
LCV	Each BPV	No	Yes	Yes	No
LES	If at least 1 LCV during sec.	Yes	Yes	Yes	No
LSES	If 45 or more LCVs during sec.	Yes	Yes	Yes	No
CV	Each P-bit error	No	No	Yes	No
ES	If at least 1 P-bit error during sec.	No	Yes	Yes	No
SES	If 44 or more P-bit error during sec.	No	Yes	Yes	No
SEFS	If at least one SEF event during sec.	No	Yes	Yes	No
AISS	If at least one incoming AIS during sec.	No	No	No	Yes
UAS	Start at onset of a failure condition	No	No	No	Yes

FIG. 53

00000-ET2200

APPROVED	C.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

Parameters	Normal counter Advance	Counter Advance During Failure Events and Conditions	
		OOE	UAT
CV(BIP-8)	Each BIP-8	No	No
ES(BIP-8)	If at least 1 BIP-8 during sec.	Yes	No
SES(BIP-8)	If 5 or more BIP-8 error during sec.	Yes	No
SEFS(BIP-8)	If at least one SEFS during sec.	Yes	No
UAS(BIP-8)	Status at onset of a failure condition	No	Yes

FIG. 54

66320-ET-2200

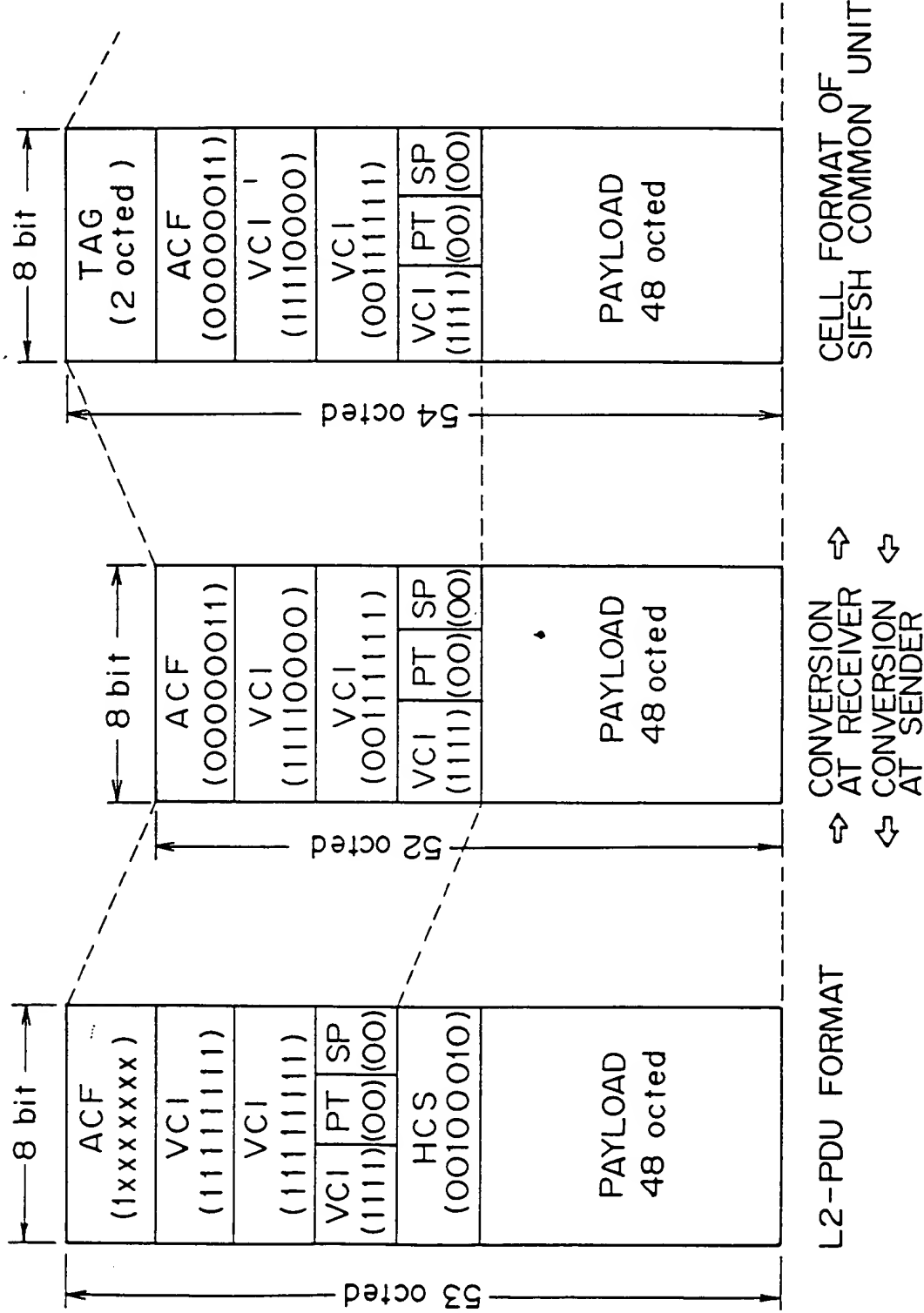
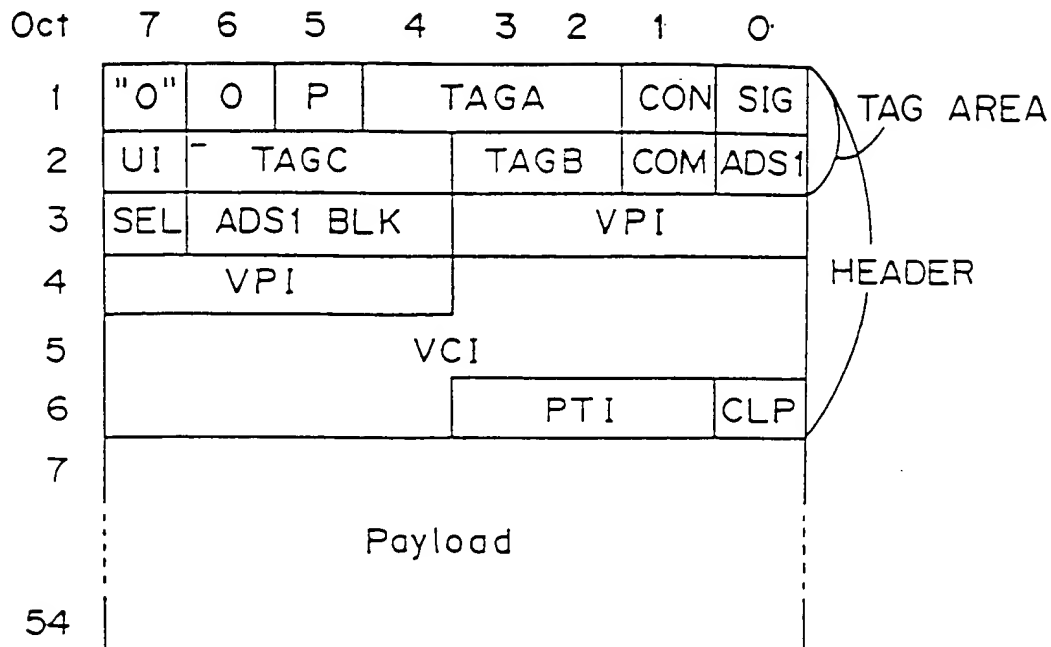


FIG. 55 IN CASE OF CONVERSION AT SENDER EFFECTIVE
ACF CELL IS "10000000"

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



O : ONE-TO-ONE COMMUNICATIONS MODE
(NO COPY MODE)

O : INTERNAL TEST CELL INDICATOR
(0: USER CELL, 1: INTERNAL CELL)

P : QUALITY INDICATOR

CON : PRIORITY CLASS INDICATOR AT CONGESTION

TAG A : 2.4 G 4 x 4 SELECTED

TAG B : 2.4 G ⇨ 600 M SELECTED

TAG C : 600 M ⇨ 156 M SELECTED

UL : DAISY-CHAIN HIGH ORDER / LOW ORDER

COM : SELECTING COMMON UNIT ACCOMMODATING
600 MHW

SIG : INTRA-STATION CELL IDENTIFICATION

ADS1 BLK : MUX ⇨ DTC SELECTED ("000" FOR DS3 - SMDS)

ADS1 SEL : ADS1 CARD SELECTED ("0" FOR DS3 - SMDS)

FIG. 56

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

66320-ET220

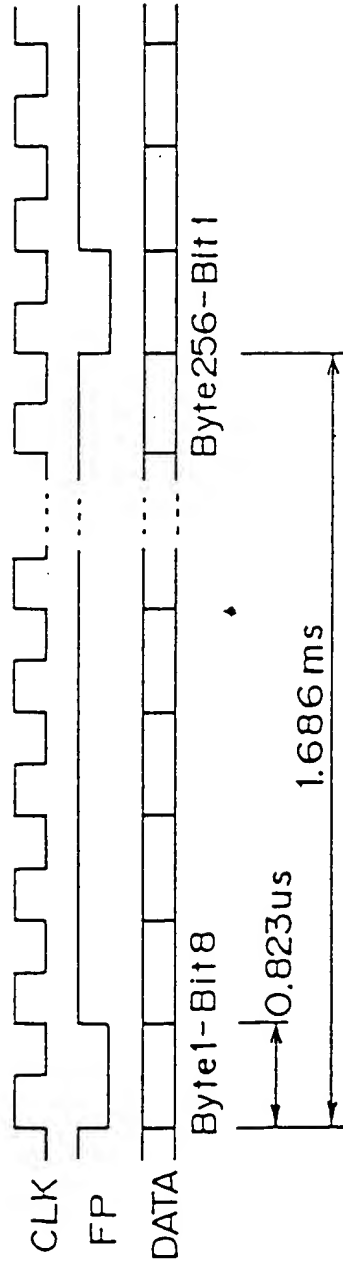


FIG. 57

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

BIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
000	PLT1	PLT0						DTEN
001								
002								
003		SDFRST	μ PRST					
004	-							
005		LOOP-2	LOOP-3	AISSND			O-LOOP	V-LOOP
006								
007	PF-CK	PF-CF	PF-PTY		PF-WDT		PTYRST	DS3DEC
008								
009								
010								
011								
012								
013								
014								
015								
016								
017								
018								
019								
020								
021								
246								
256								

UNUSED AREA

FIG. 58

669220-0122200

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

ROW No	DATA	ABBR	MEANING	POLARITY	TYPE
000	0	DTEN	DATA ENABLE (SET IN SIFSH COMMON)	Neg	S/R
000	6	PLT0	STUCK MONITOR PILOT BIT (FIXED EARTH)	Neg	S/R
000	7	PLT1	STUCK MONITOR PILOT BIT (FIXED AT +5)	Neg	S/R
003	5	μ PRST	μ -PROCESSOR RESET (FOR MAINTENANCE)	Neg	S/R
003	6	SDFRST	FAULT RESET	Neg	S/R
005	0	V-LOOP	SPECIFYING VPI/VCI CELL LOOPBACK	Pos	S/R
005	1	O-LOOP	SPECIFYING "0"-BIT CELL LOOPBACK	Pos	S/R
005	4	AISSND	SPECIFYING TRANSMISSION OF AIS PATTERN IN DS3 LINE	Pos	S/R
005	5	LOOP-3	SPECIFYING LINE LOOPBACK	Pos	S/R
005	6	LOOP-2	SPECIFYING INTERNAL LOOPBACK (DS3 SMDS ALL LOOP)	Pos	S/R
007	0	DS3DEC	SPECIFYING DIAGNOSYS OF DS3-HARDWARE	Pos	S/R
007	1	PTYRST	PARITY ERROR RESET	Pos	S/R
007	4	PF-WDT	SPECIFYING PSEUDO-FAULT OF WATCH DOG TIMER	Pos	S/R
007	5	PF-PTY	SPECIFYING PSEUDO-FAULT OF PARITY ERROR	Pos	S/R
007	6	PF-CF	SPECIFYING PSEUDO-FAULT OF CELL FRAME PULSE DISCONNECTION CHECKER	Pos Pos	S/R S/R
007	7	PF-CK	SPECIFYING PSEUDO-FAULT OF CELL DISCONNECTION CHECKER	Pos	S/R

POLARITY : Neg : 0/1 = SIGNIFICANT/INSIGNIFICANT
 : Pos : 0/1 = INSIGNIFICANT/SIGNIFICANT
 : DOUBLE VALUES : SIGNIFICANT AT CHANGE POINT

FIG. 59

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

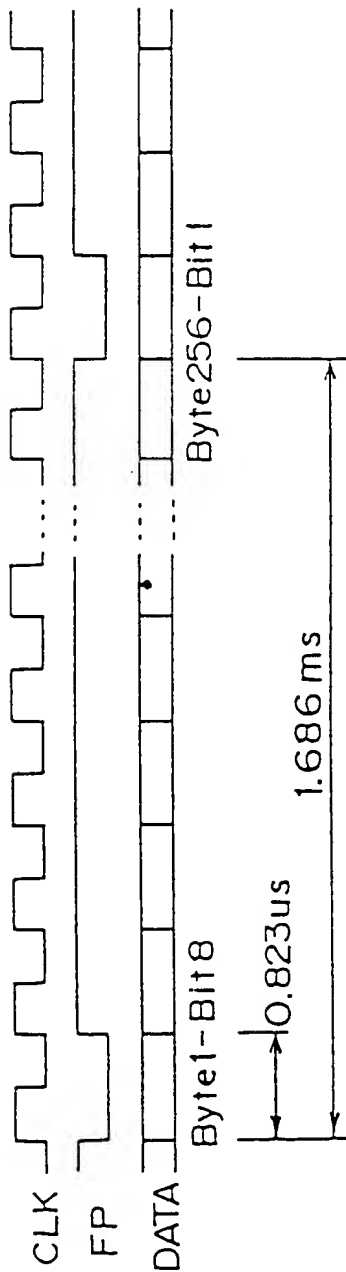


FIG. 60

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

BIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
000	PLT1	PLT0	PWC8 GROUP ID					
001	0	0	1	0	0	0	0	1
002	SYNCF0	PLTF0	SYNCF1	PLTF1	PE0	PE1		
003	-	SDFRST	PRST					
004								
005		LOOP-2	LOOP-3	AISSND			O-LOOP	V-LOOP
006								
007	PF-CK	PF-CF	PF-PTY		PF-WDT		PTYRST	DS3DEC
008								
009								
010								
011								
012								
013								
014								
015	EC-AC1	EC-ACO	EC-TID	EC-TQH	EC-TSM			
016	FERR-1	FERR-2	LIALM	TCAALM	CLOSAL			TIMALM
017			MPE			TSTEND	TSTIND	INS
018	DH19M0	DH19M1	DHCFO	DHCF1	DHDPT0	DHDPT1		
019	UHDPT	UH19M	EGPTY					
020			L1FLG	TCAFLG	CLFLG			
021								
031		DEC NG PHASE No.				DEC NG TST No.		
246								
	UNUSED AREA							
255								

FIG. 61

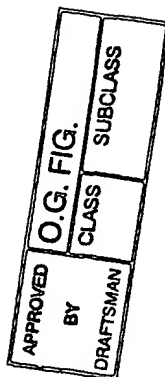
[illegible]

FIG. 62

ROW No	DATA	ABBREVIATION	MEANINGS	POLARITY	TYPE	RESET
015	6	EC-AC0	ECHO-BACK OF OTHER LINE MSD(ACT#0)	Neg	—	—
015	7	EC-AC1	ECHO-BACK OF OTHER LINE MSD(ACT#1)	Neg	—	—
016	0	TIMALMD	OTHER LINE TIMER INFORMATION NG OR CONDITION	Pos	NOT HELD	SDFRST
016	3	CLOSAL	15M → 45M CONVERSION BUFFER CELL DISCARD START OR CONDITION	Pos	NOT HELD	—
016	4	TCAALM	DS3/PLCP TCA OR CONDITION	Pos	NOT HELD	—
016	5	LIALM	DS3/PLCP ALARM OR CONDITION	Pos	NOT HELD	—
016	6	FEER-2	SD3-SMDS INF HARDWARE FAULT OR CONDITION	Pos	HELD	SDFRST
016	7	FEER-1	INTRA-STATION COMMUNICATION DISABLE DS3-SMDS INF HARDWARE FAULT	Pos	HELD	SDFRST
017	0	INS	DS3-SMDS INF MICROPROCESSOR INITIALIZATION TERMINATE	Pos	HELD	—
017	1	TSTIND	DS3-SMDS DIAGNOSTICS RESULT INDICATOR	Pos	HELD	SDFRST
017	2	TSTEND	DS3-SMDS DIAGNOSTICS COMPLETION INDICATOR	Pos	HELD	SDFRST
017	5	MPE	DS3-SMDS INF MICROPROCESSOR FAULT	Pos	HELD	μ PRST
018	2	DHDPT1	#1 SYSTEM DOWNWARD PRIMARY SIGNAL DATA PARITY ERROR	Pos	HELD	FRST1
018	3	DHDPT0	#0 SYSTEM DOWNWARD PRIMARY SIGNAL DATA PARITY ERROR	Pos	HELD	FRST0
018	4	DHCF1	#1 SYSTEM CELL FRAME FAULT	Pos	HELD	FRST1
018	5	DHCF0	#0 SYSTEM CELL FRAME FAULT	Pos	HELD	FRST0
018	6	DM19M1	#1 SYSTEM DOWN 19M CLOCK FAULT	Pos	HELD	FRST1
018	7	DM19M0	#0 SYSTEM DOWN 19M CLOCK FAULT	Pos	HELD	FRST0
019	5	EGPTY	EGCLAD PARITY ERROR	Pos	HELD	SDFRST
019	6	UH19M	UP 19M CLOCK FAULT	Pos	HELD	SDFRST
019	7	UHDPT	UPWARD PRIMARY SIGNAL DATA PARITY ERROR	Pos	HELD	SDFRST
020	3	CLFLG	15M → 45M CONVERSION BUFFER CELL DISCARD START CHANGE FLAG	ALTERNATION	NOT HELD	—
020	4	TCAFLG	DS3/PLCP TCA CHANGE FLAG	ALTERNATION	NOT HELD	—
020	5	LIFLG	DS3/PLCP ALARM CHANGE FLAG	ALTERNATION	NOT HELD	—
031	0-3	DEC NG TST No.	DS3-SMDS INF DIAGNOSTICS NG TST No. INDICATOR	Pos	HELD	—
031	4-7	DEC NG Ph No.	DS3-SMDS INF DIAGNOSTICS NG PH No. INDICATOR	Pos	HELD	—

POLARITY: NEG: 0/1=SIGNIFICANT/INSIGNIFICANT; POS: 0/1
=INSIGNIFICANT/SIGNIFICANT; ALTERNATION: SIGNIFICANT WHEN CHANGE IS MADE

FIG. 63



66666-6722660

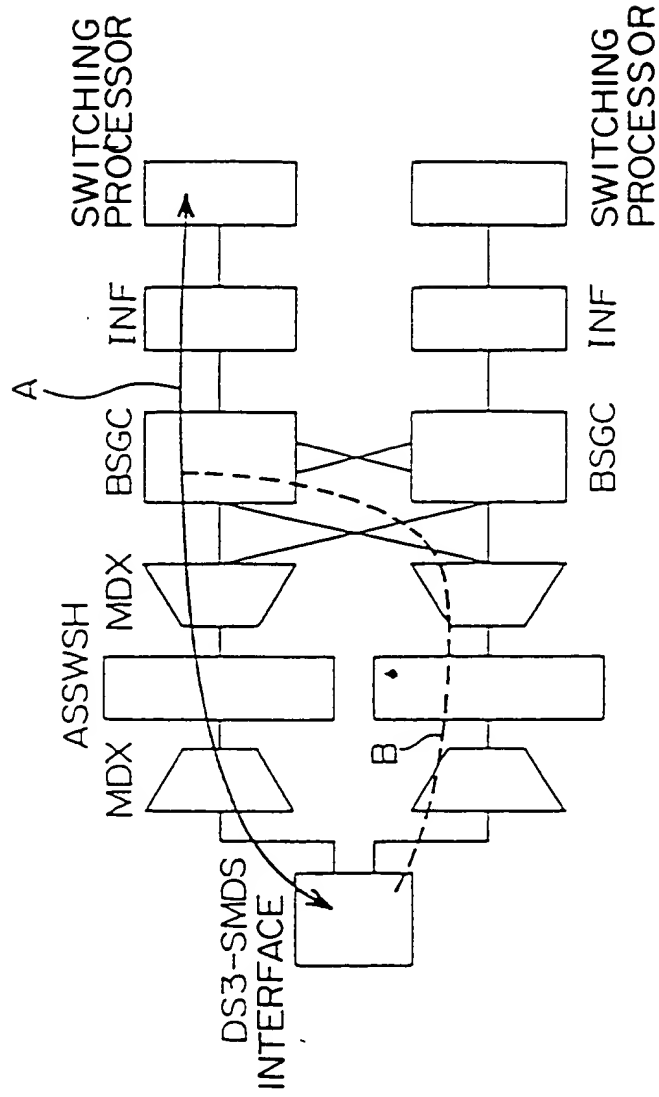


FIG. 64

669260-6732260

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

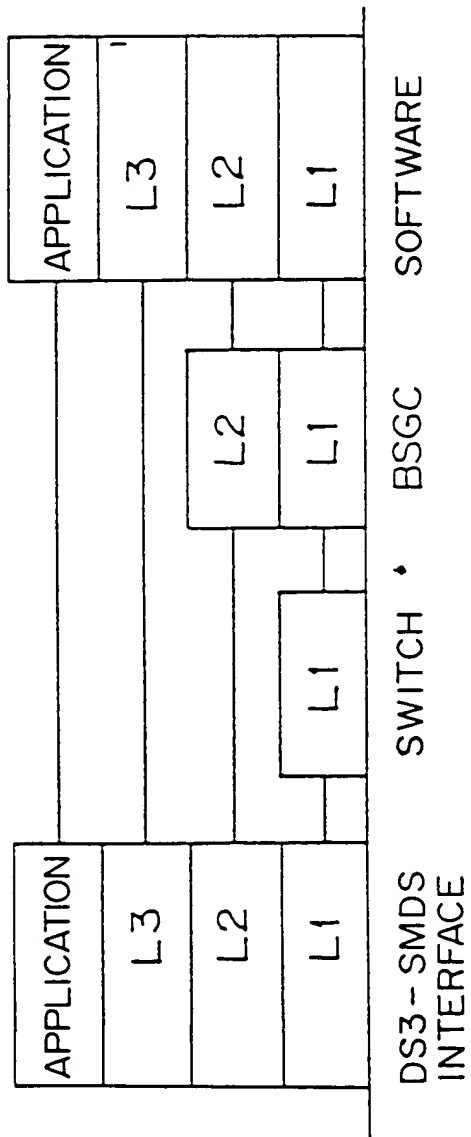
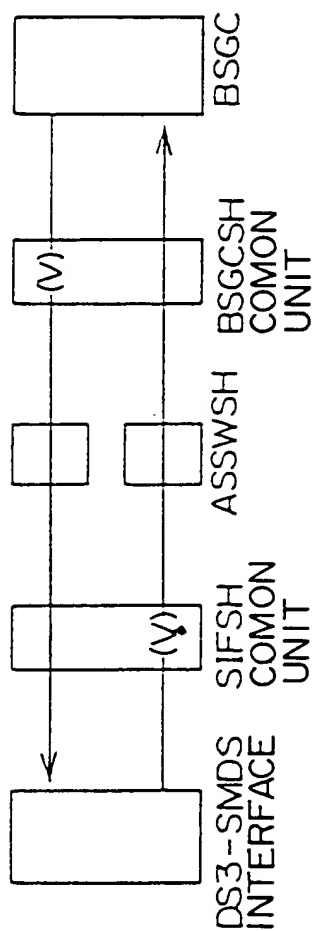


FIG. 65

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

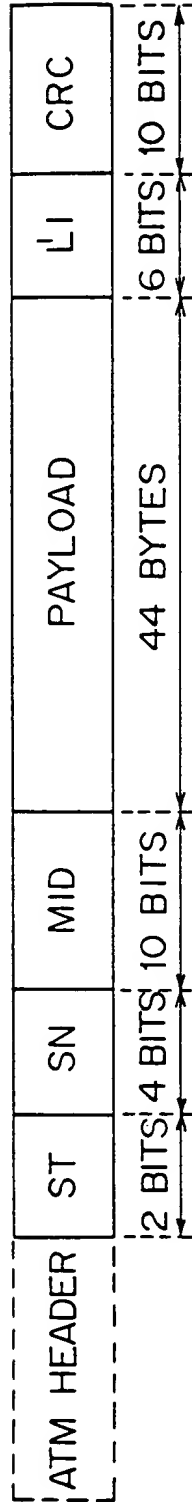
00000-012200



(V) : INDICATES POSITION OF VCC

FIG. 66

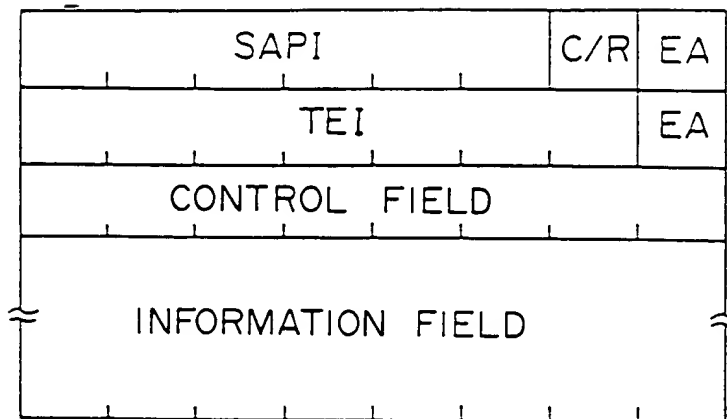
APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



ST : SEGMENT TYPE (BOM, EOM, SSM, etc)
 SN : SEQUENCE NUMBER
 LI : PAYLOAD BYTE LENGTH INDICATOR
 CRC : CRC (CRC-10 OF ST, SN, MID, AND PAYLOAD)
 MID : d.c. FOR INTRA-STATION COMMUNICATIONS CELL

FIG. 67

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		



SAPI : ALL '0'

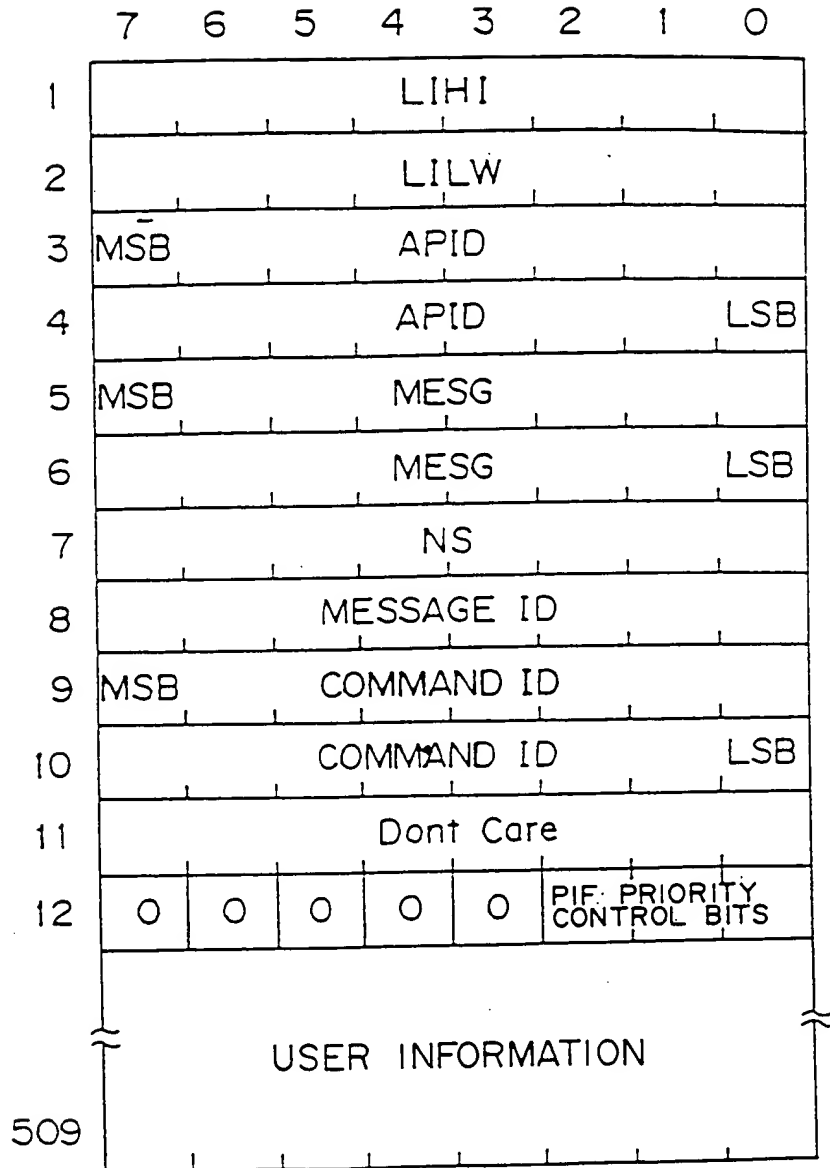
C/R : '1'

EA : EXTENSION ADDRESS (= 0)

TEI : ALL 0 IN SINP → BSGC DIRECTION
PRIORITY LEVEL IS DEFINED FOR 3
LOWER BITS.

CONTROL FIELD : ID IS ASSIGNED TO SABM, UA, RR, AND DISC.

FIG. 68

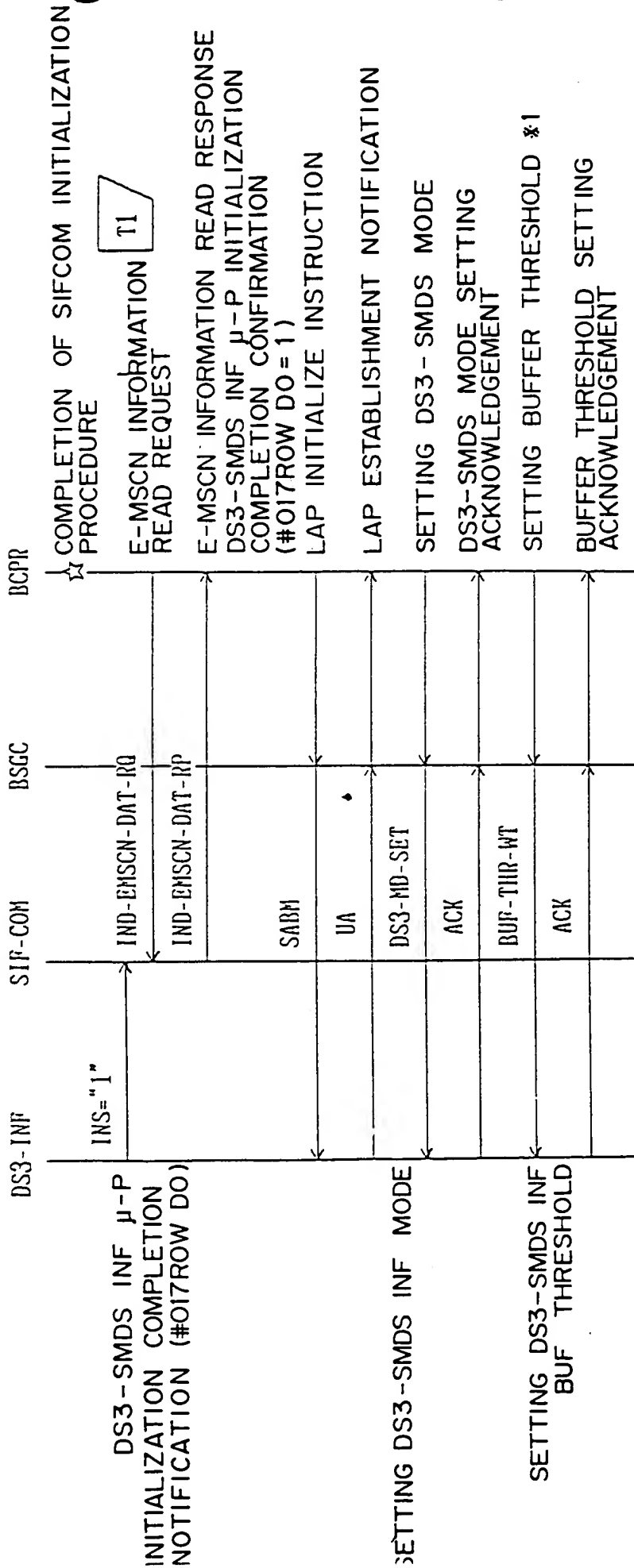


LIHI: INDICATES HIGHER HITS OF OCTETS \leq LILW
 LILW: INDICATES LOWER HITS OF OCTETS \leq LILW
 APID: INDICATES APPLICATION TO BE COMMUNICATED
 MESH: IDENTIFIES MESSAGE IN APPLICATION
 NS: BCPR \rightarrow DEVICE SIGNAL
 COMMAND ID: SOFTWARE SEQUENCE NUMBER

FIG. 69

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

(1) DS3-SMDS INTERFACE INITIALIZATION



T1: TIMEOUT AFTER 500 (MSEC) x 30 TIMES

*1: SET WHEN NECESSARY

FIG. 70

669220-0000

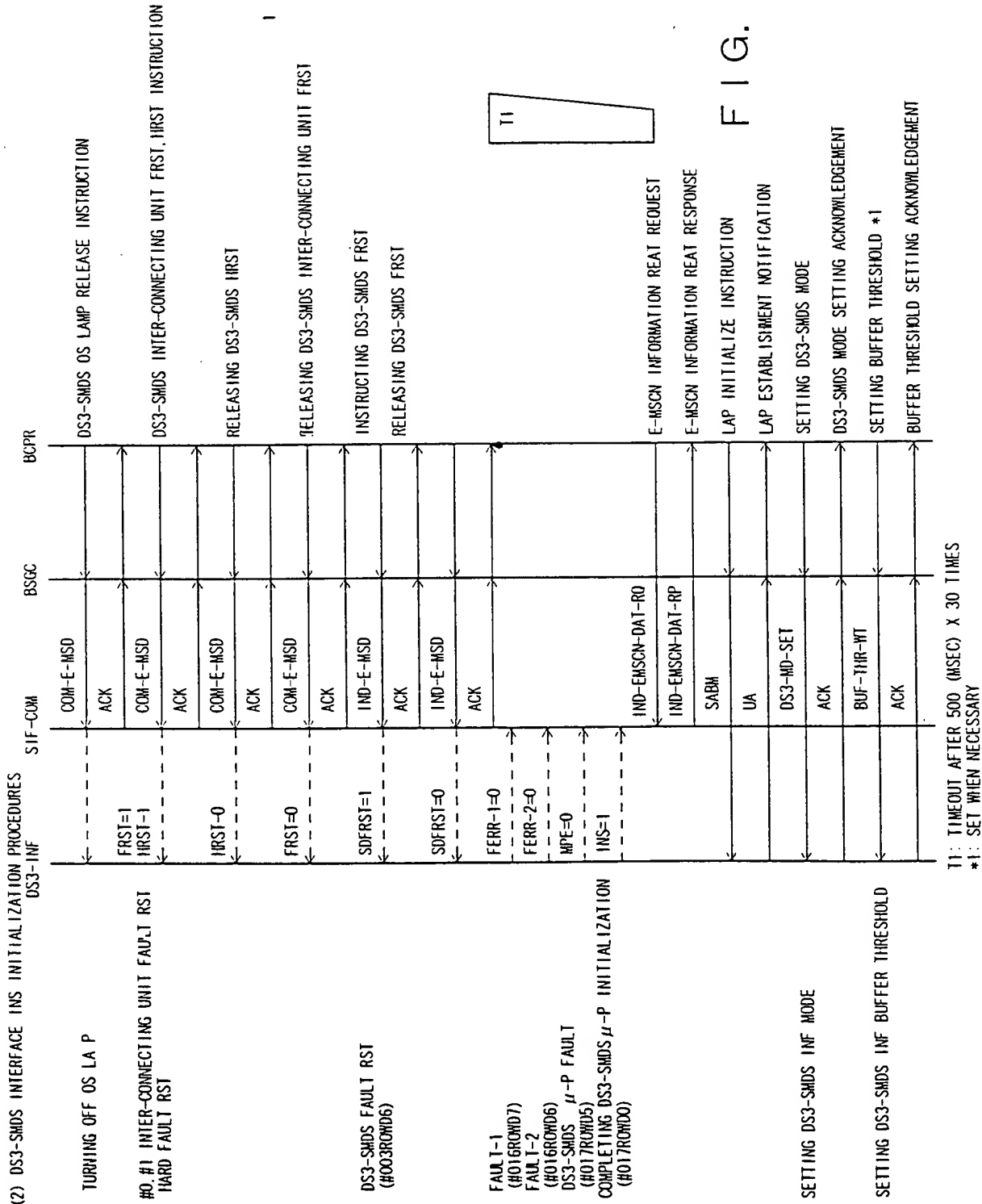


FIG. 71

(3) DS3-SMDS INTERFACE OUS PROCEDURE (MAINTENANCE BLOCK)

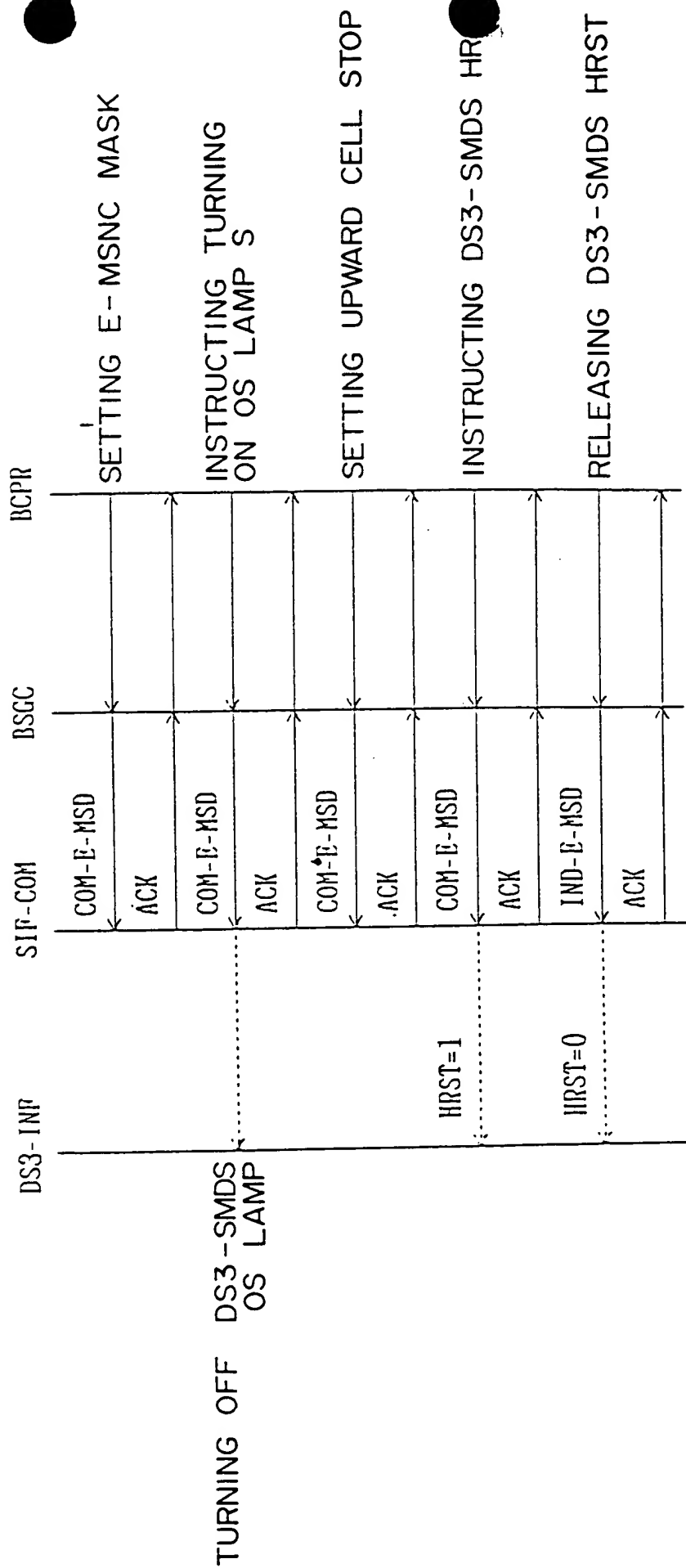


FIG. 72

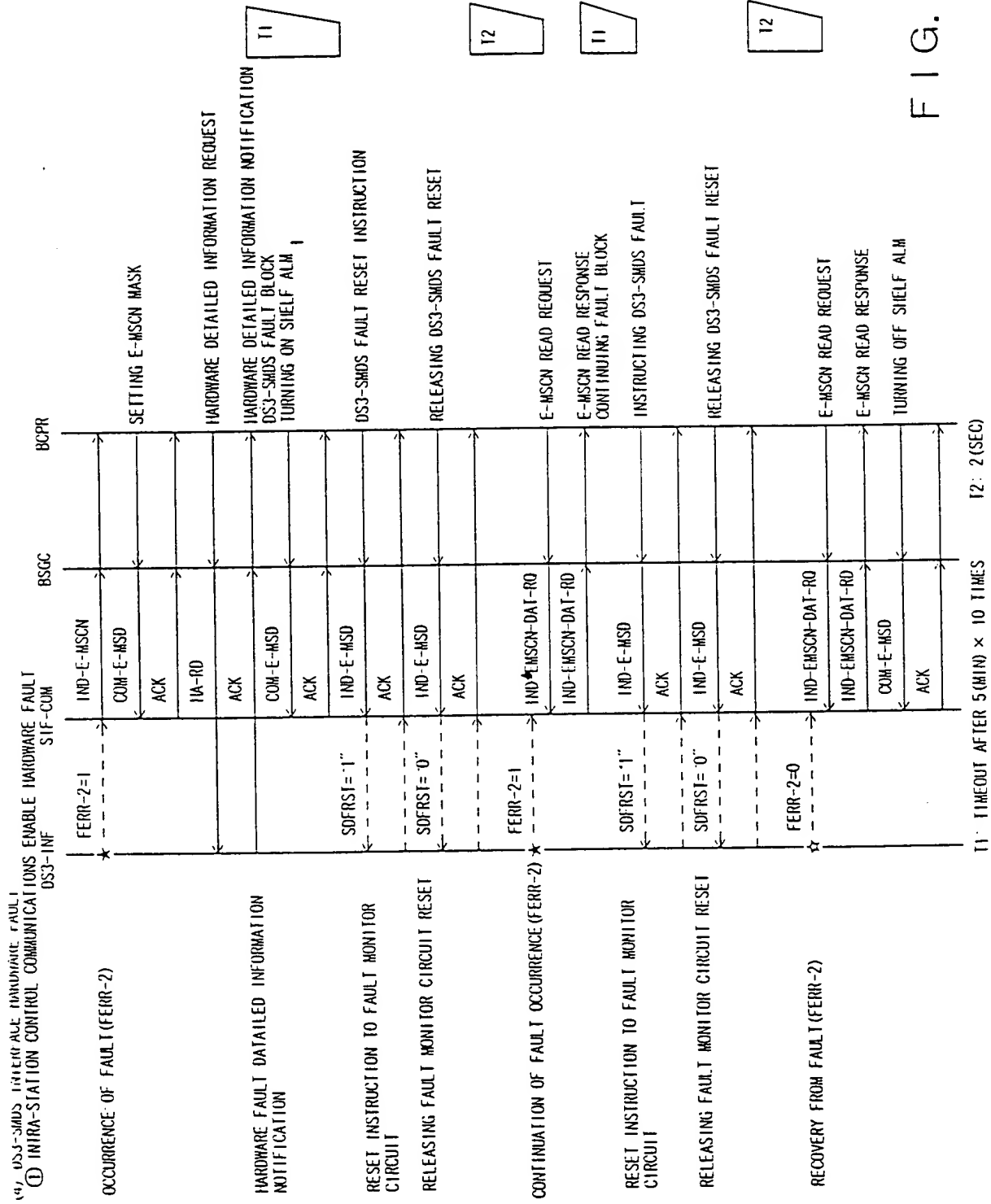


FIG. 73

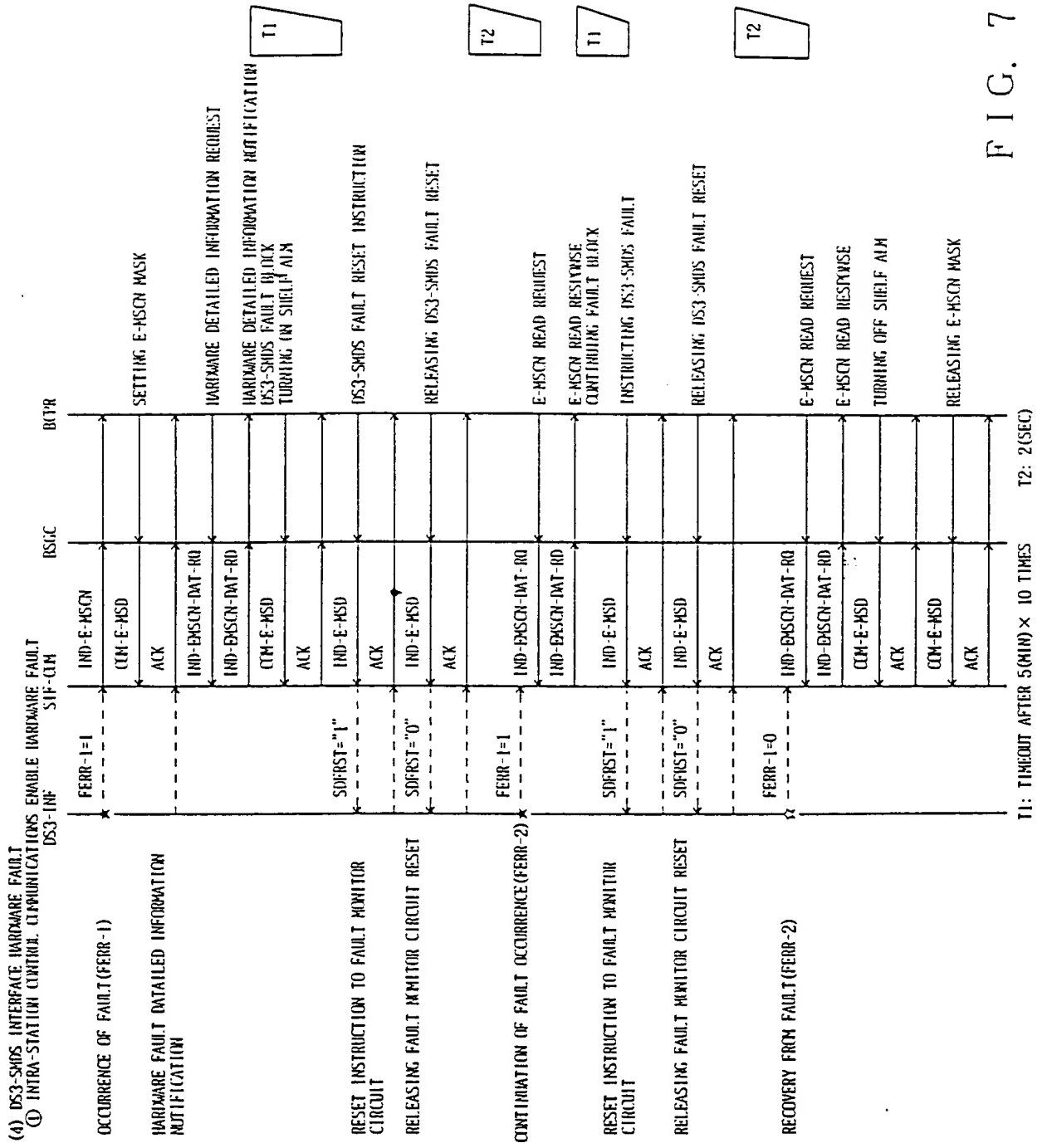


FIG. 74

(4) DS3-SMDS INTERFACE HARDWARE FAULT
 ③ μ PROCESSOR FAULT

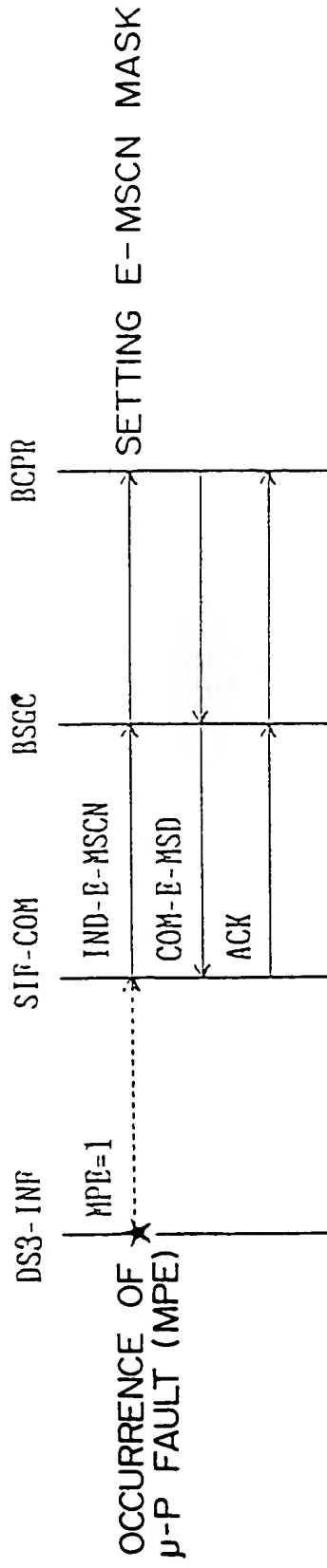


FIG. 75

(4) DS3-SMDS INTERFACE HARDWARE FAULT

④ SIFSH COMMON UNIT - DS3 SMDS IN INTER-CONNECTING UNIT FAULT (ACT SYSTEM)

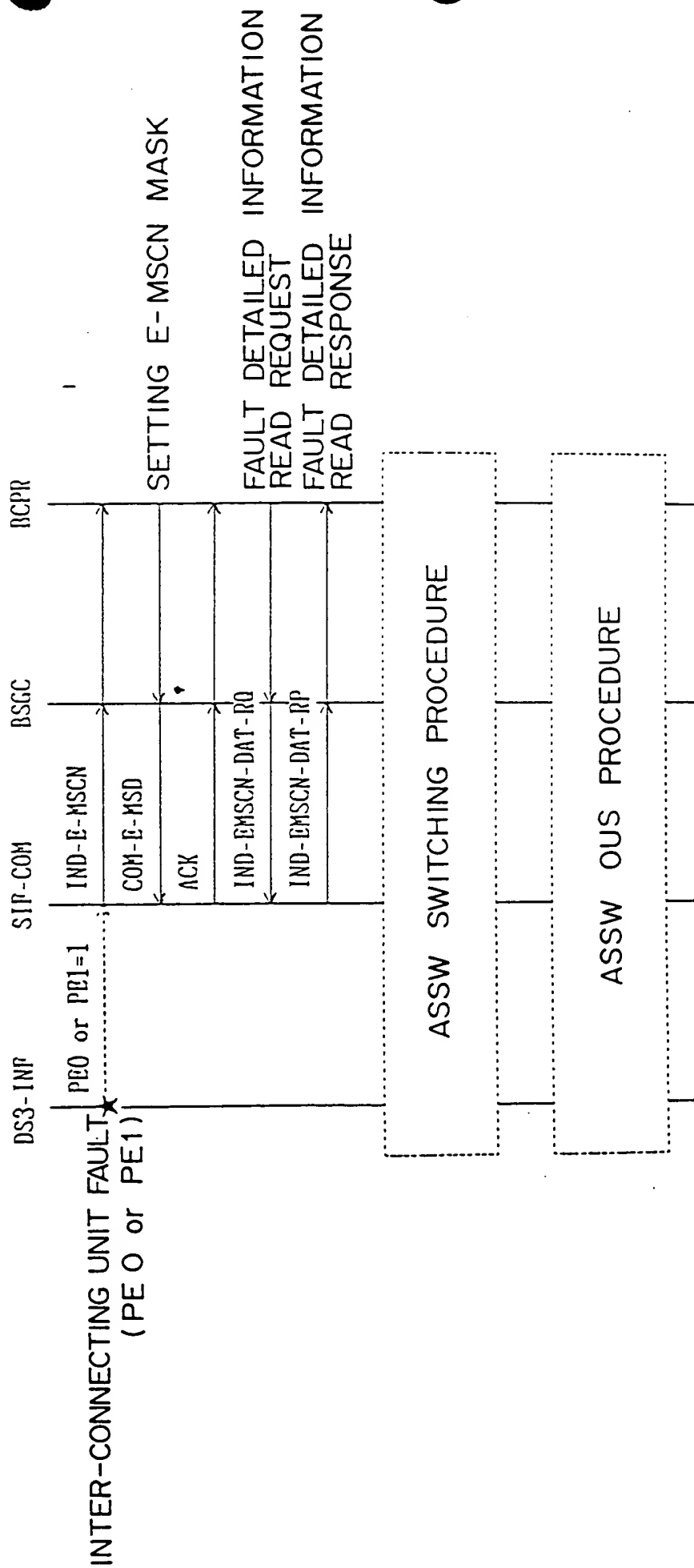


FIG. 76

(4) DS3-SMDS INTERFACE HARDWARE FAULT

⑤ SIFSH COMMON UNIT - DS3 SMDS IN INTER-CONNECTING UNIT FAULT (SBY SYSTEM)

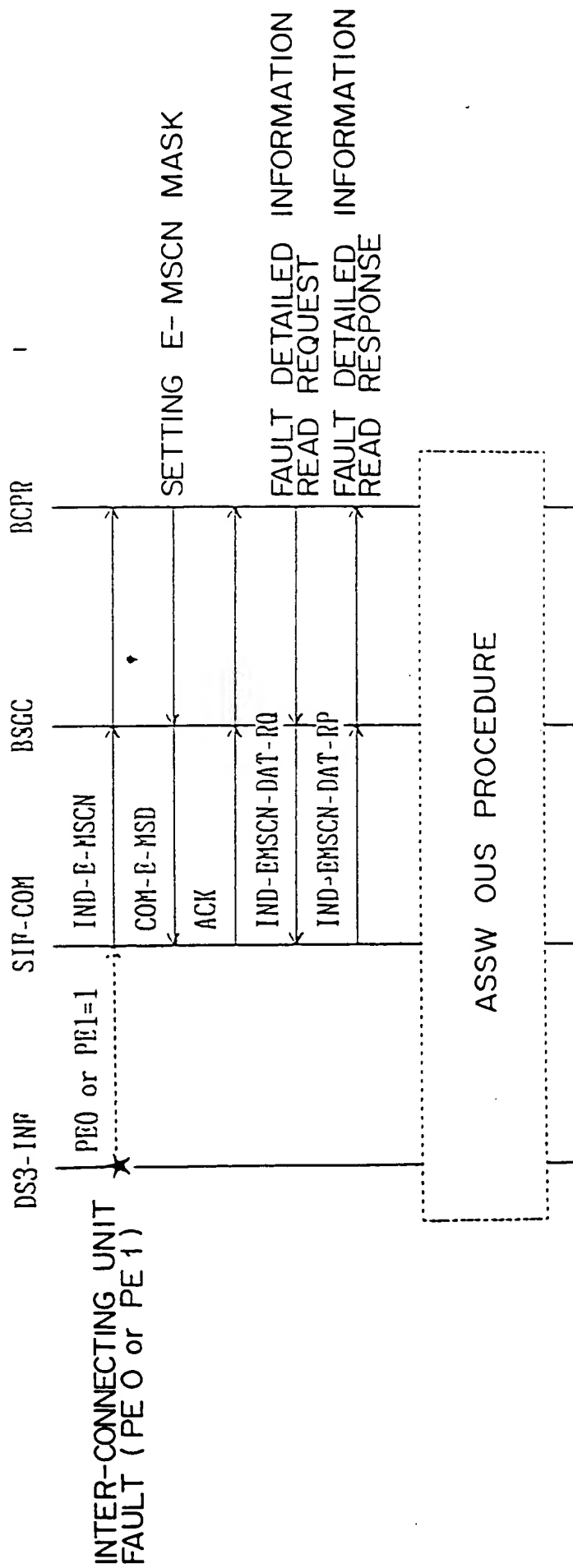


FIG. 77

(5) DS3/PLCP LAYER ALARM PROCESS

#016ROW D6

#020ROW D6

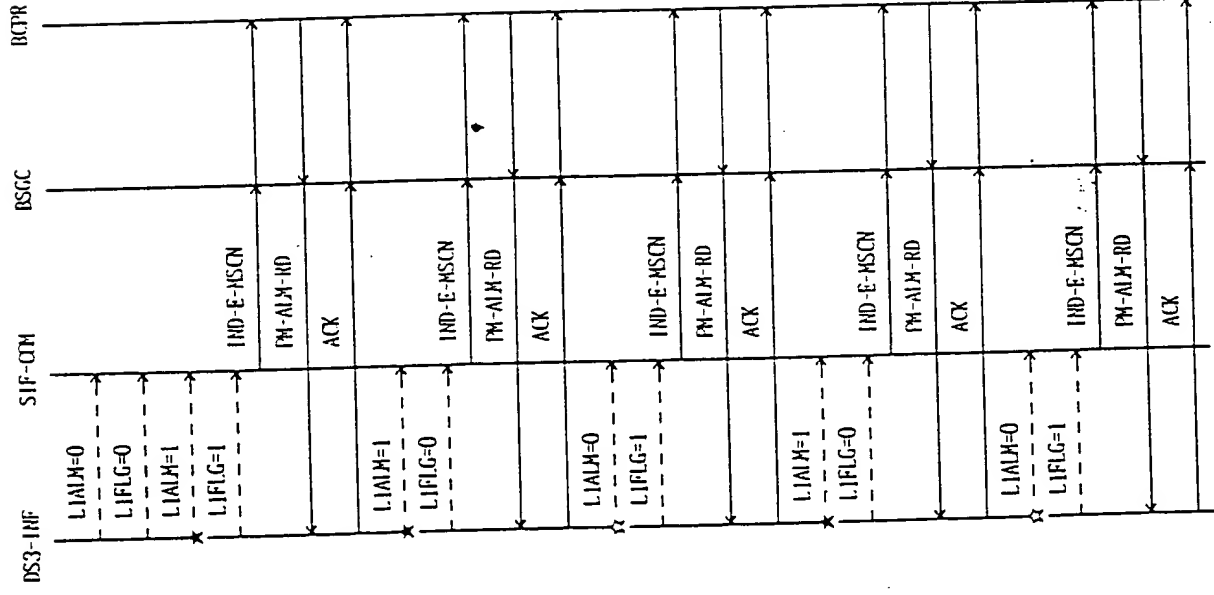
GENERATION OF DS3/PLCP ALARM
(DS3RED=1)

SENDING DETAILED INFORMATION
GENERATION OF DS3/PLCP ALARM
(DS3RED=0, DS3AIS=1)

SENDING DETAILED INFORMATION
RECOVERY OF DS3/PLCP ALARM
(DS3AIS=0)

GENERATION OF DS3/PLCP ALARM
(POOF=1)

RECOVERY OF DS3/PLCP ALARM
(POOF=0)



(6) D/Q-TIMER NOTIFICATION AND PM DATA COLLECTION WHEN DS3/PLCP TCA OCCURS

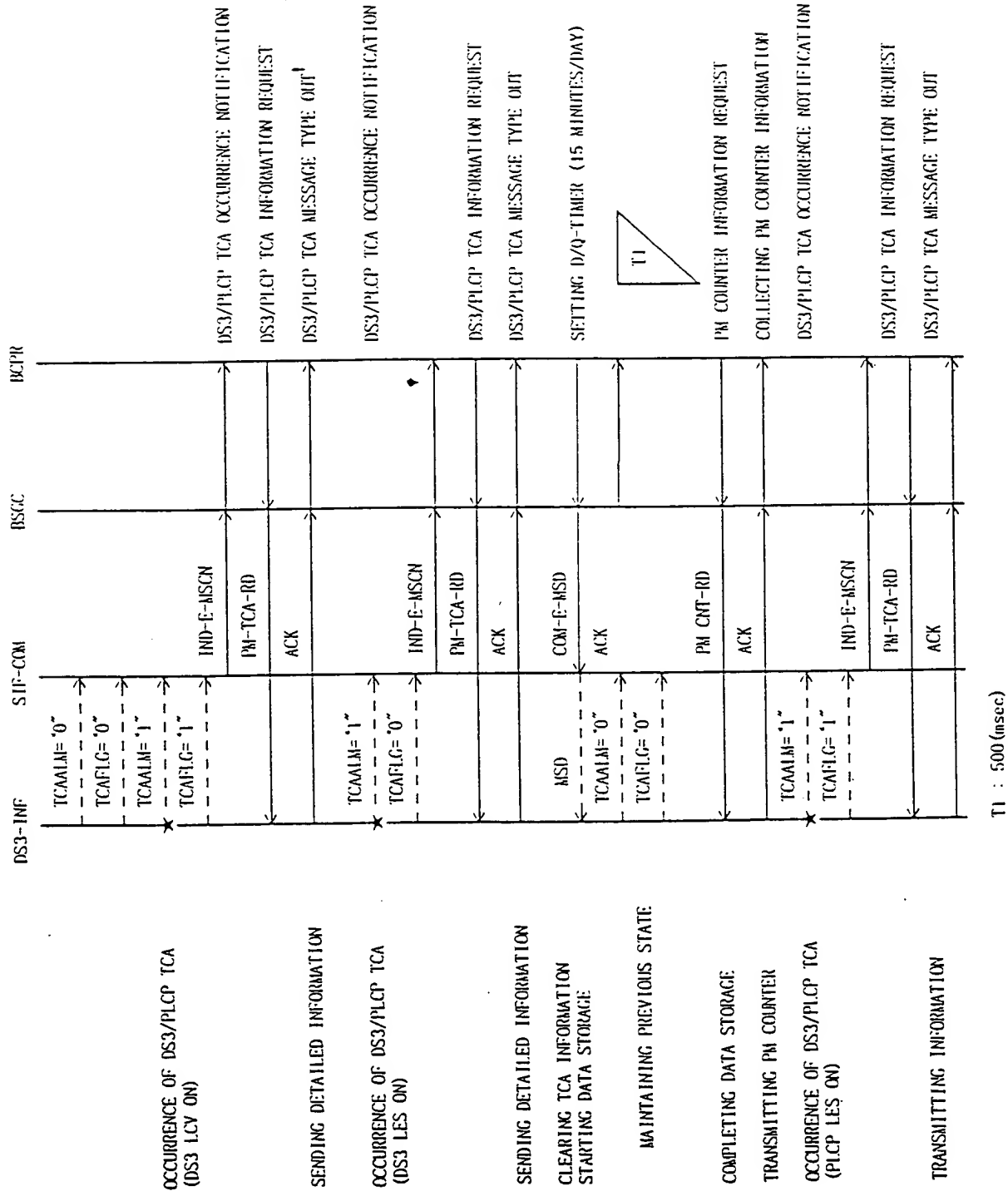


FIG. 79

(6) D/O-TIMER NOTIFICATION AND BUFFER DATA COLLECTION WHEN DS3/PLCP TCA OCCURS

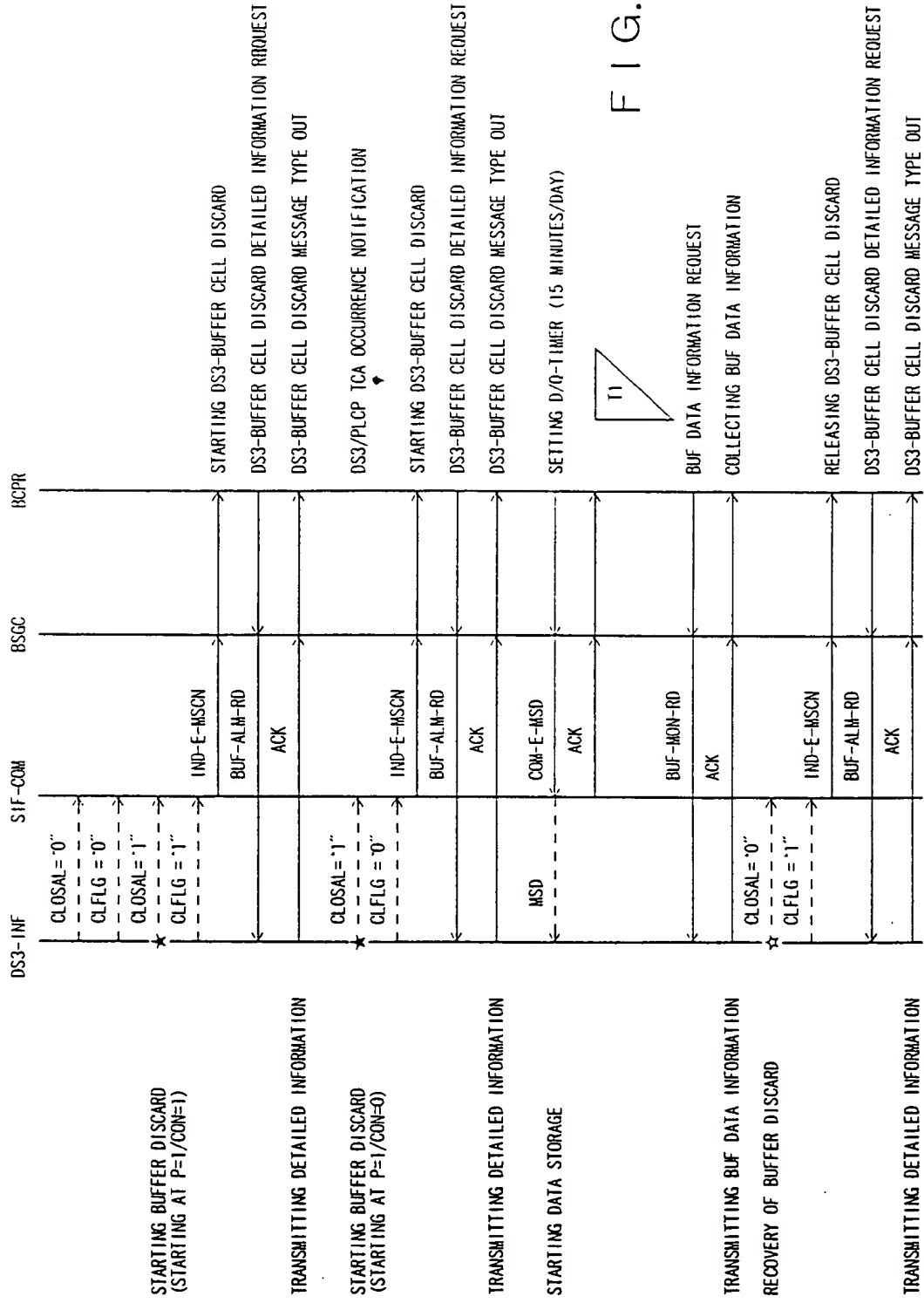


FIG. 80

(8) SETTING PVC PATH TEST SPECIAL NUMBER VPI / VCI CELL

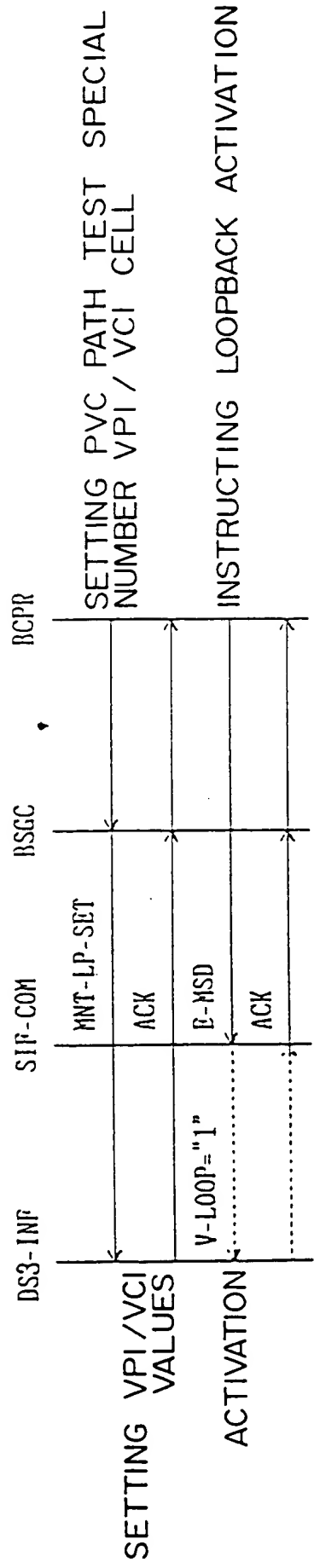


FIG. 81

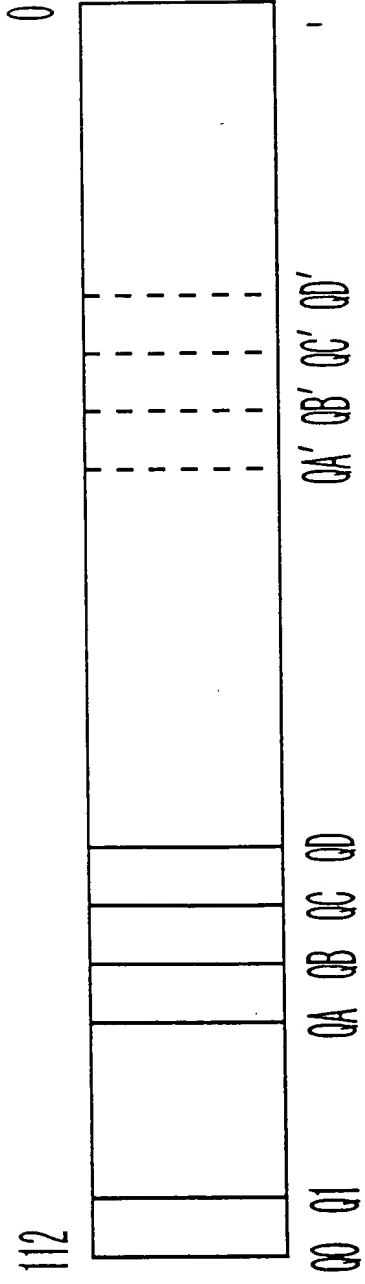


FIG. 82 .

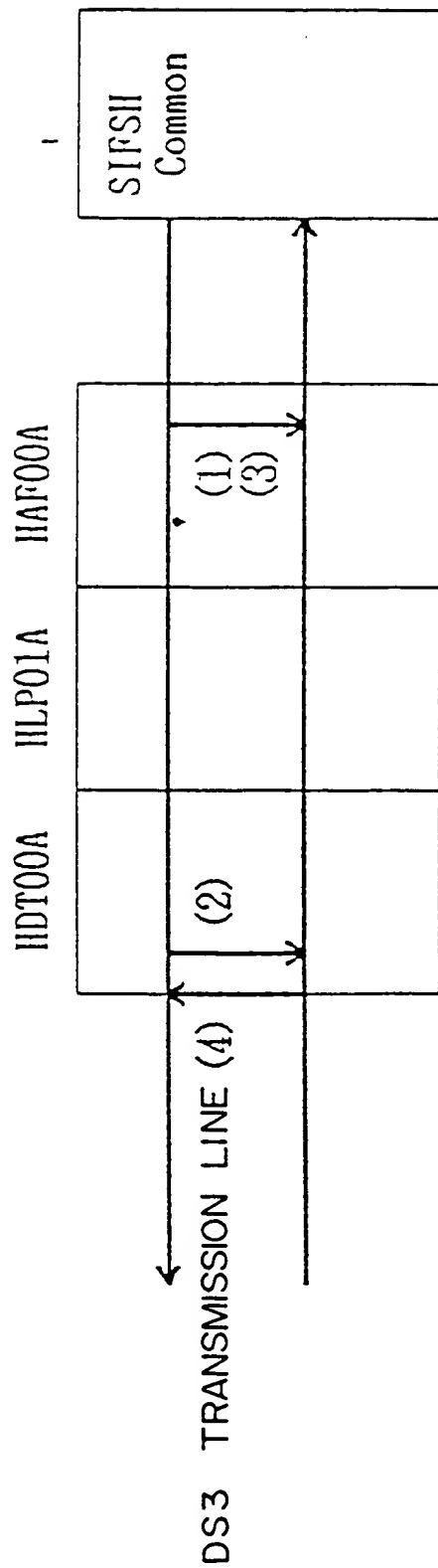


FIG. 83

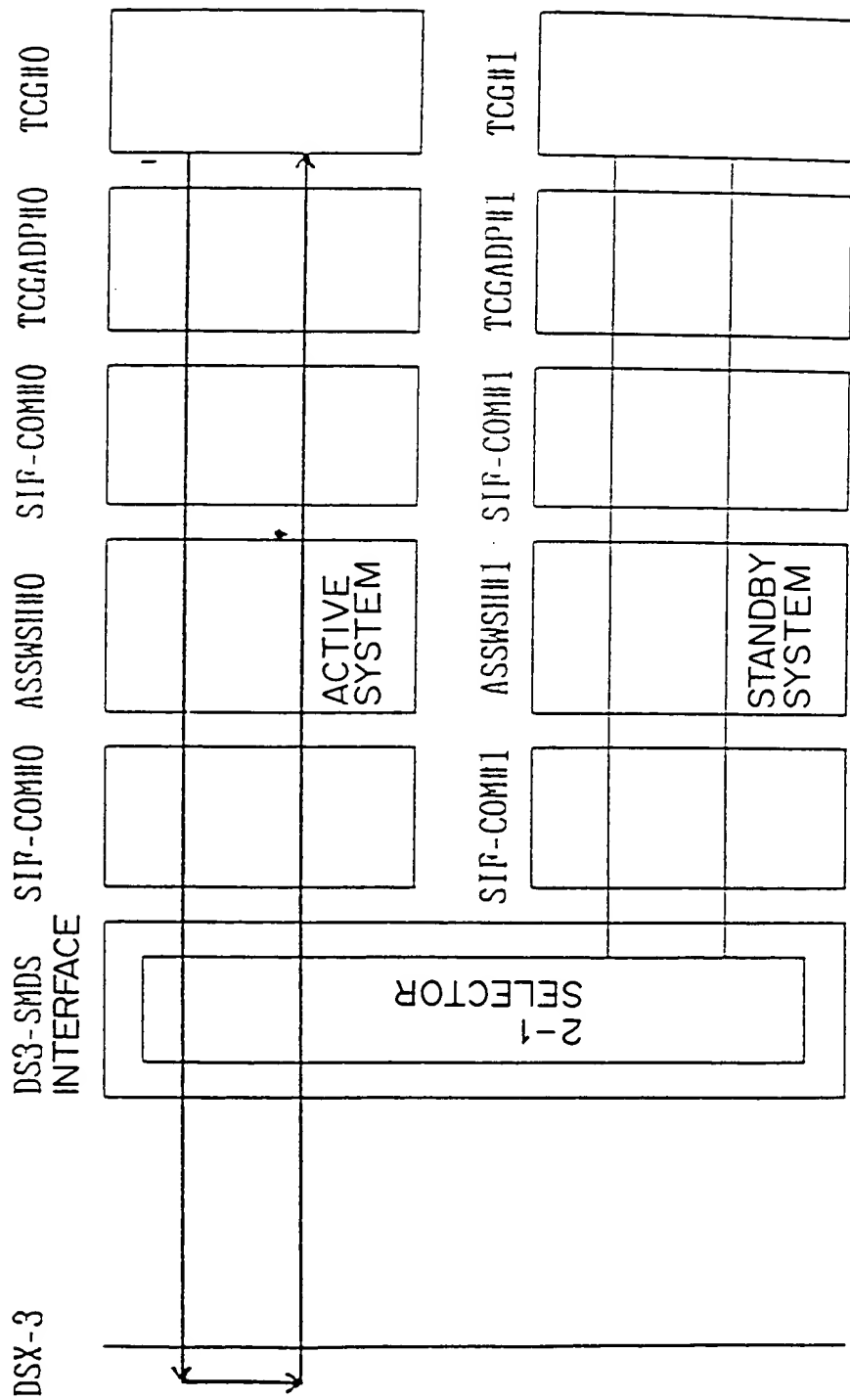


FIG. 84

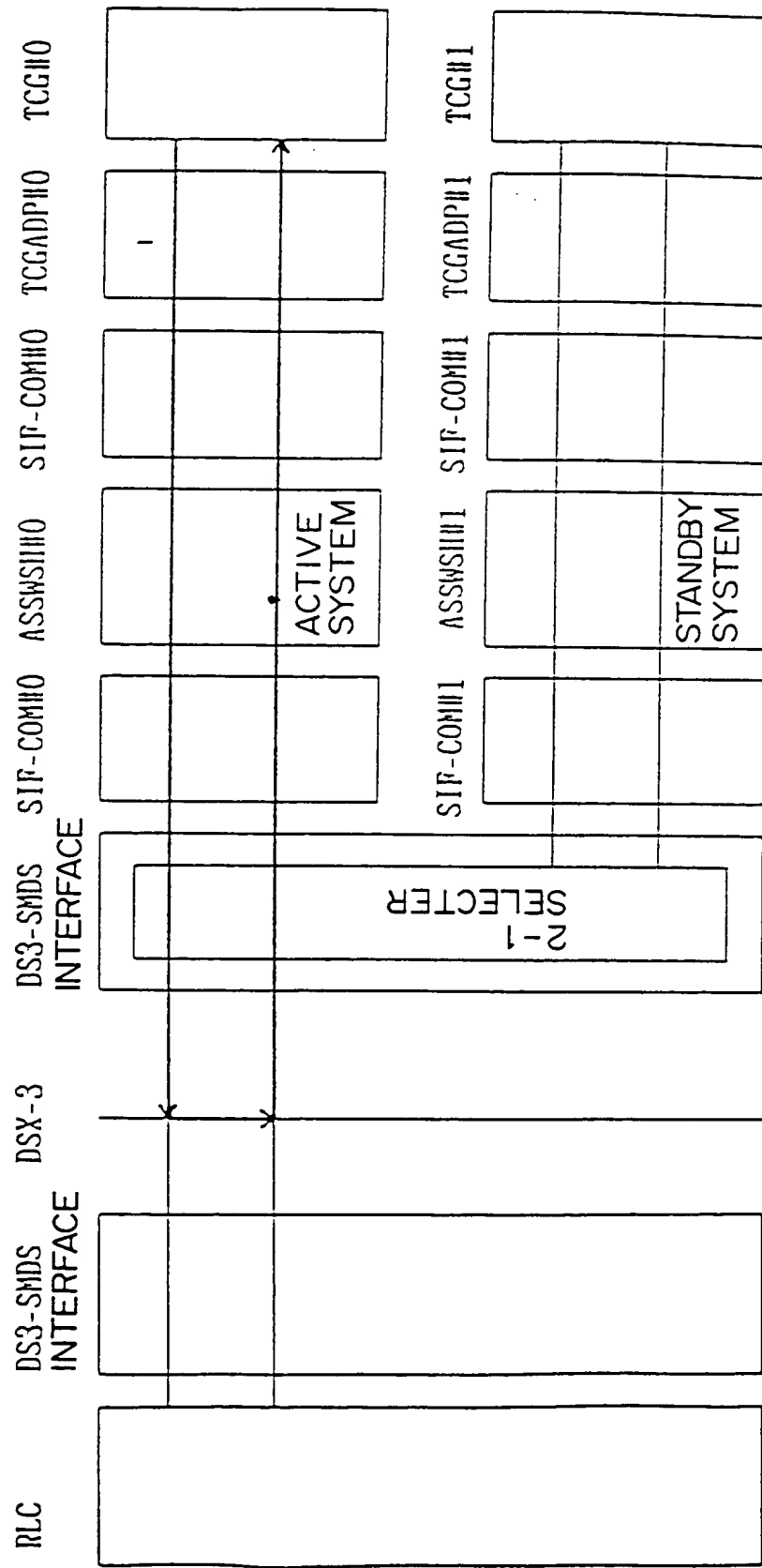
[illegible]

FIG. 58

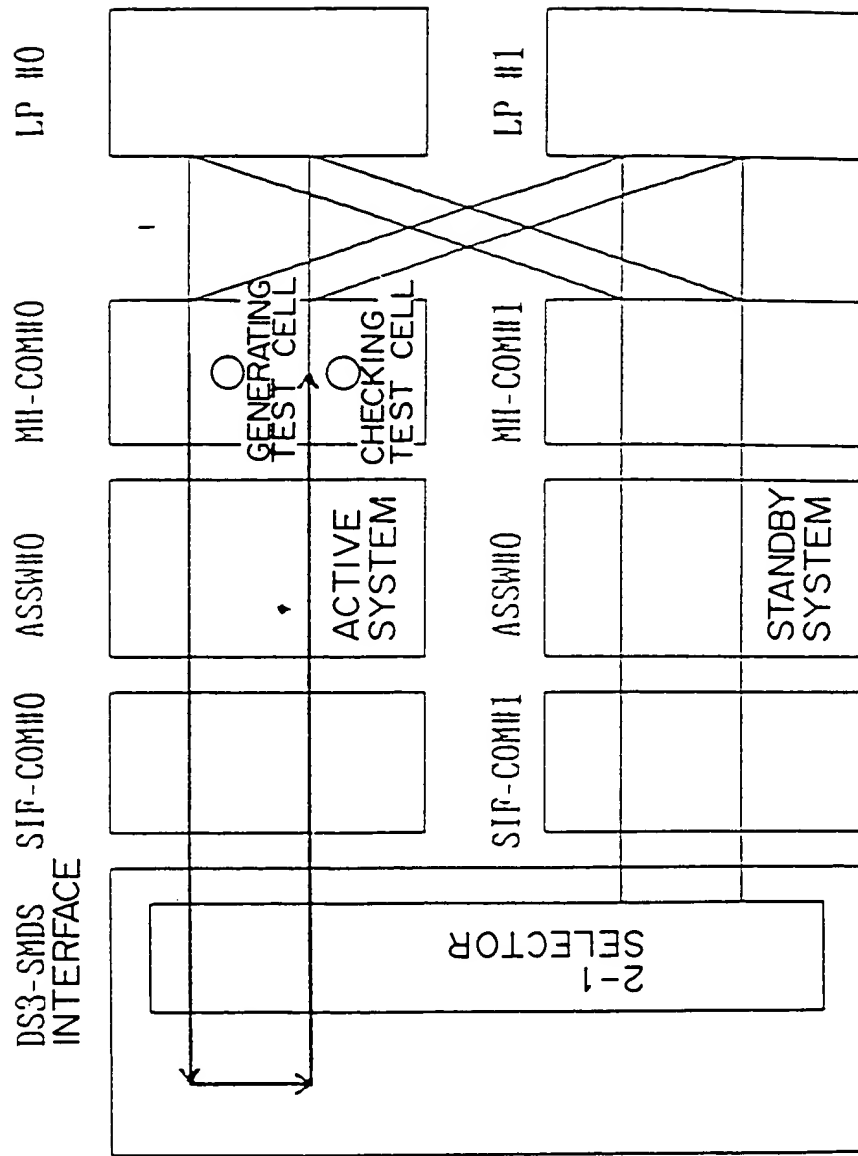
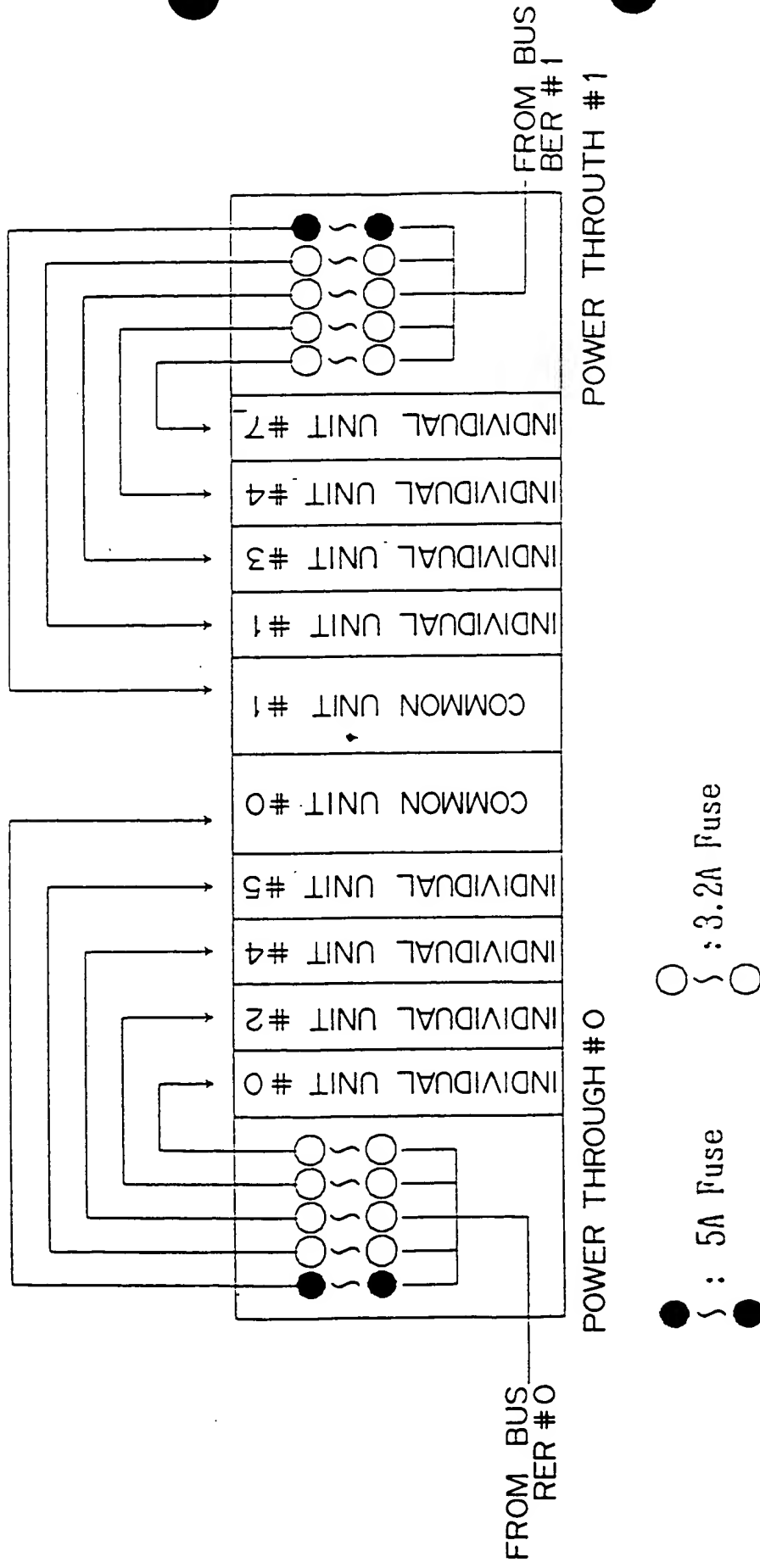


FIG. 86



NOTE 1 : IN INDIVIDUAL UNIT PACKAGE, EVEN-NUMBER LINES ARE ACCOMMODATED IN LEFT HALF WHILE ODD-NUMBER LINES ARE ACCOMMODATED IN RIGHT HALF.

FIG. 87

1

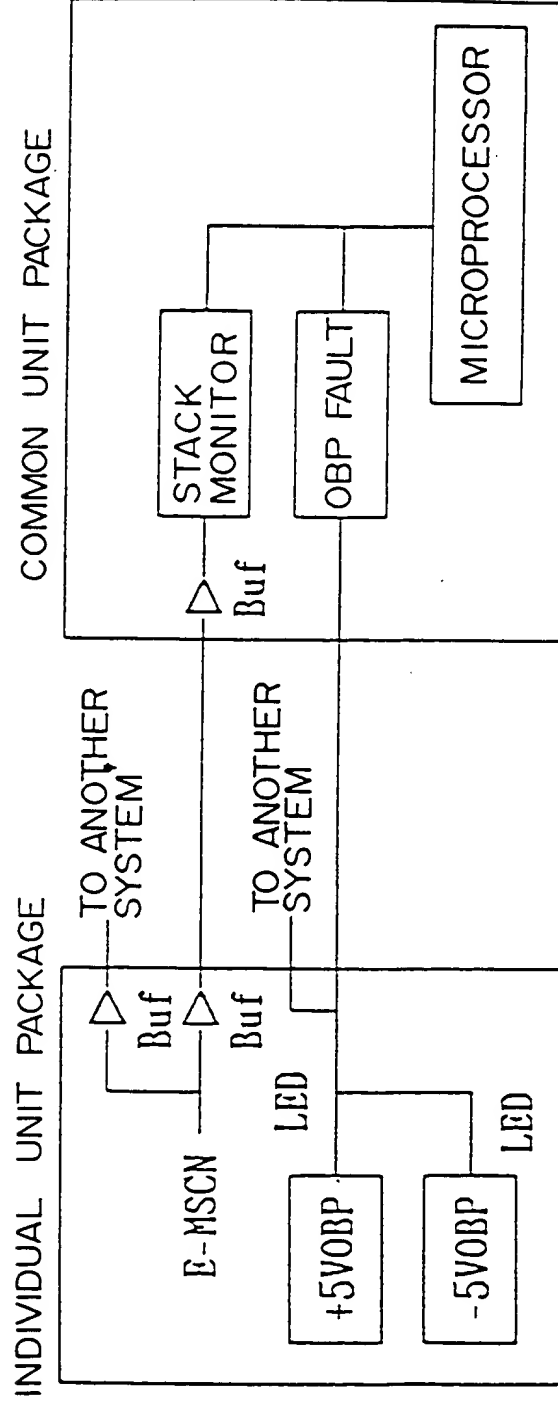


FIG. 88

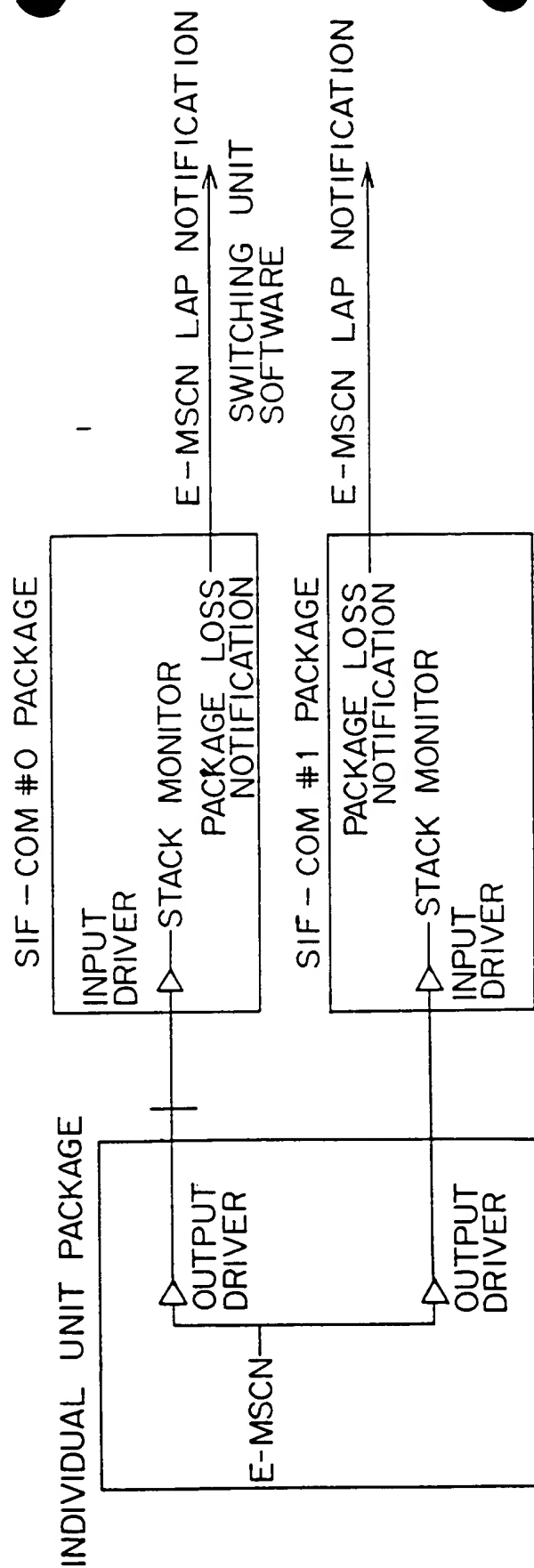


FIG. 89

66920*E72260

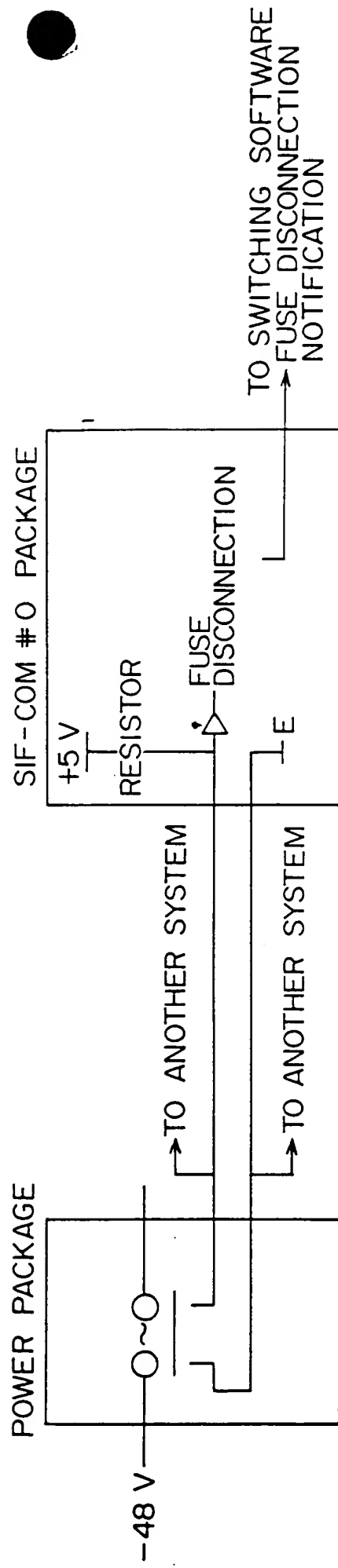


FIG. 90

#0 SYSTEM ACT	#1 SYSTEM ACT	ACT STATE
0	0	MAINTAINING PREVIOUS STATE
1	0	#1 SYSTEM ACT
0	1	#0 SYSTEM ACT
1	1	MAINTAINING PREVIOUS STATUS

FIG. 91

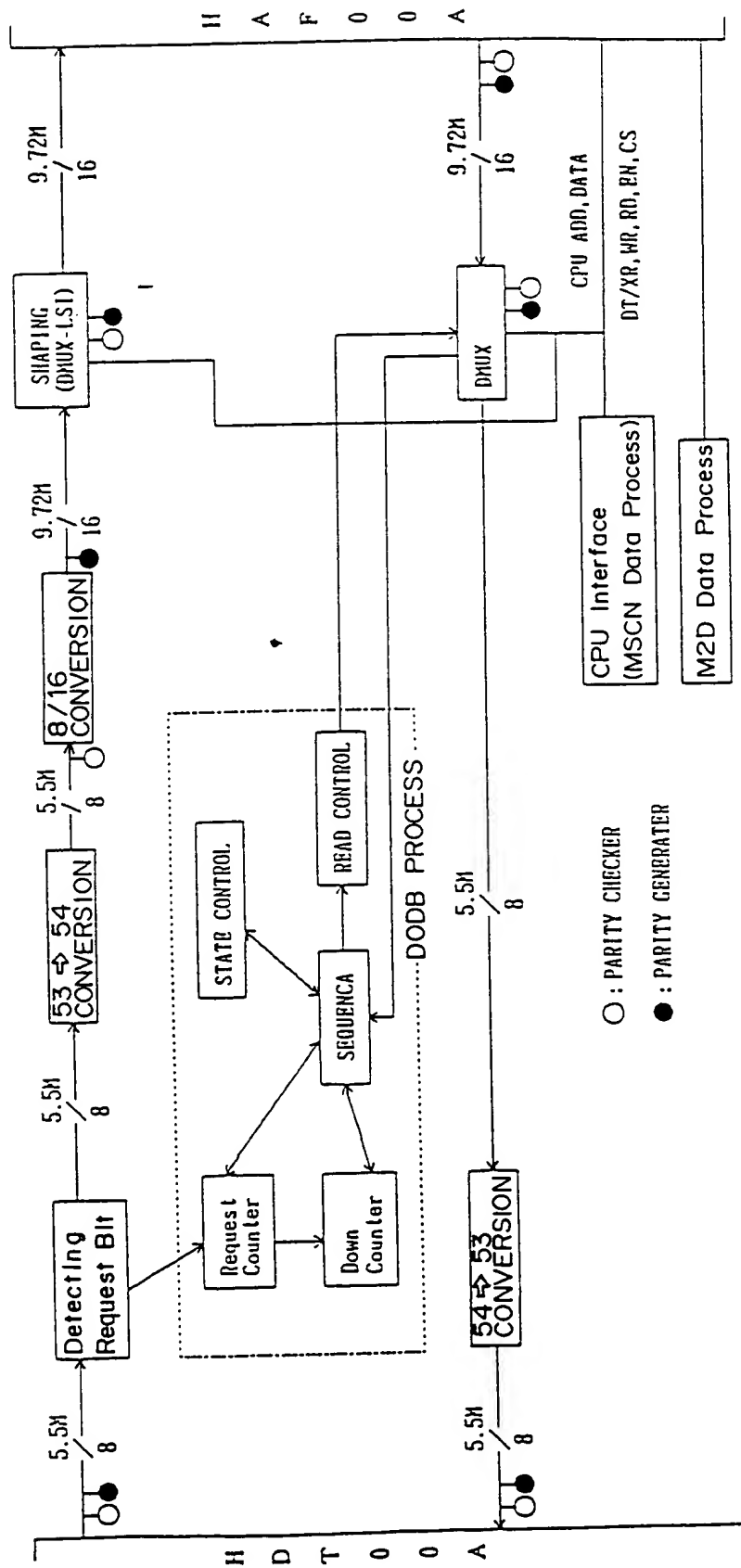
[illegible]

FIG. 92

MEMORY SPACE		CONTROL CS	I/O SPACE		CONTROL CS
FFFF (H)	ROM Area	USC	FFFF (H)	BLANK	
E000 (H)	BLANK		0380 (H)	DS3 CONTROL INF CONTROL REGISTER Area	PCS6
18000 (H)	UP DMUX LSI CONTROL REGISTER Area	MCS3	0300 (H)	DS3 SWITCH INF CONTROL REGISTER Area	PCS5
16000 (H)	DOWN DMUX LSI CONTROL REGISTER Area	MCS2	0280 (H)	DEQUEUE	PCS4
14000 (H)	EGCLAD LSI CONTROL REGISTER Area	MCS1	0200 (H)	DS3 LINE INF CONTROL REGISTER Area	PCS3
12000 (H)	EGCLAD DUAL PORT RAM Area	MCS0	0180 (H)	DS3 LSI CONTROL REGISTER Area	PCS2
10000 (H)	BLANK		0100 (H)	HAPLE2 LSI CONTROL REGISTER Area	PCS1
08000 (H)			0080 (H)	UP SELN1 LSI	
00000 (H)	SRAM Area	LCS	0040 (H)	DOWN SELN1 LSI	PCS0
			0000 (H)		

FIG. 93

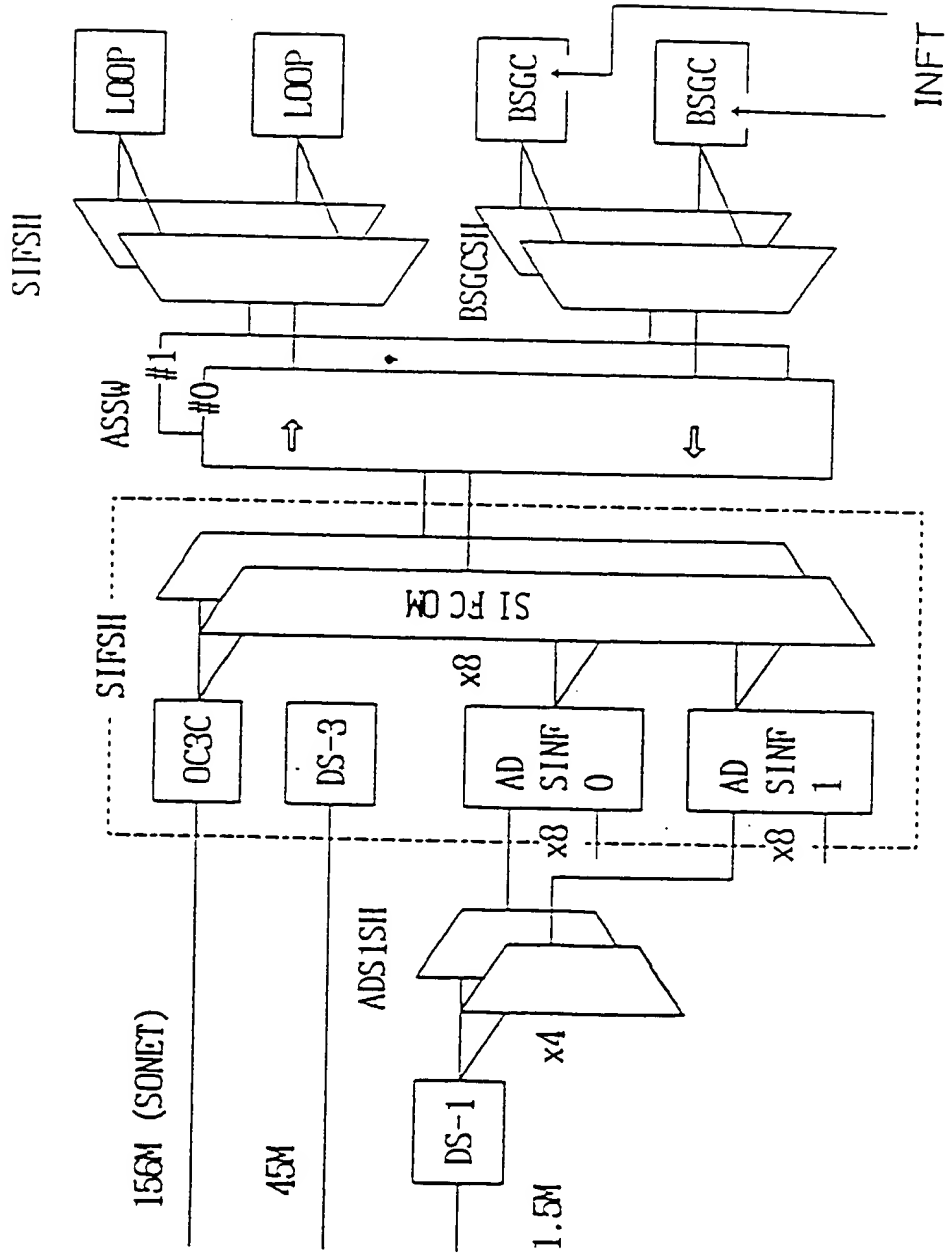


FIG. 94

669300 0122260

PKG NAME	FUNCTION
HSF01A	Shelf common controller
HMX04A	Shelf common up highway multiplexer
HMX05A	Shelf common down highway demultiplexer A
HMX06A	Shelf common down highway demultiplexer B
HPT01A	-48V power supply

FIG. 95

669260-122260

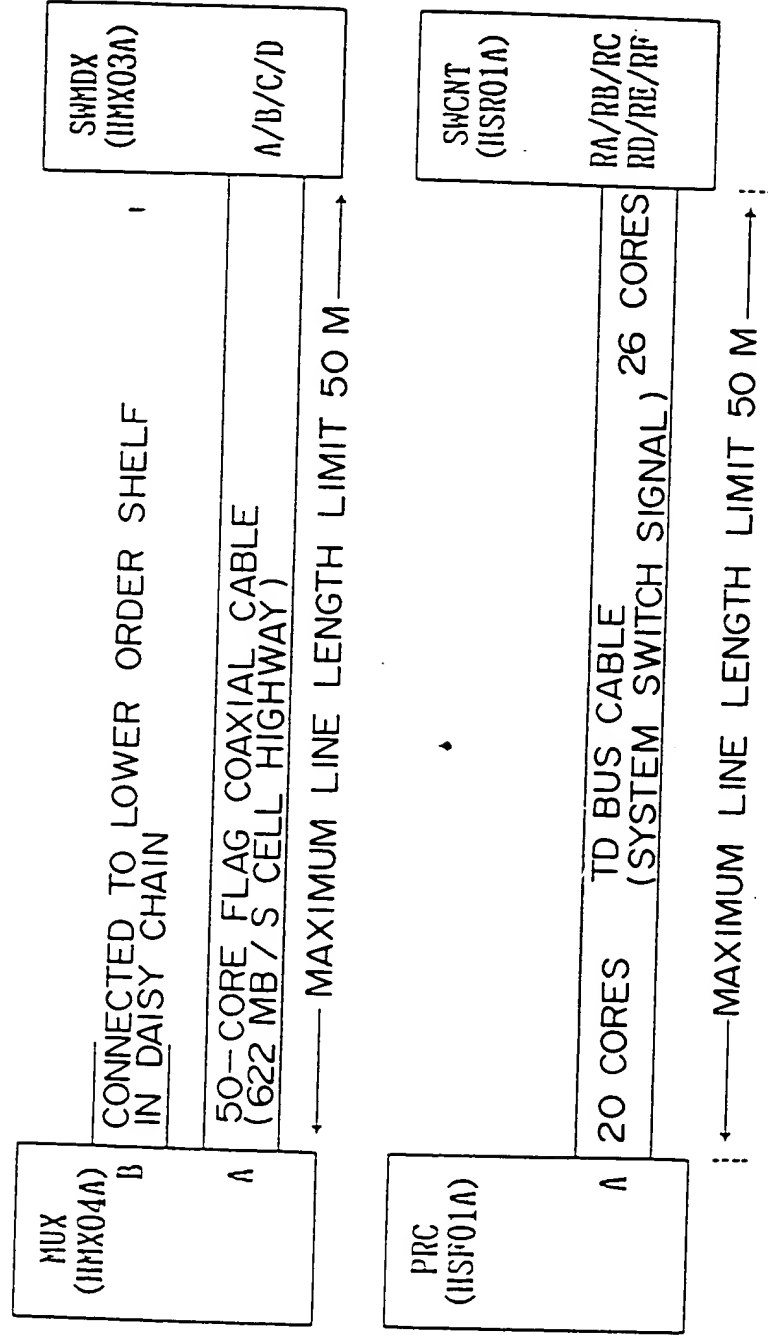


FIG. 96

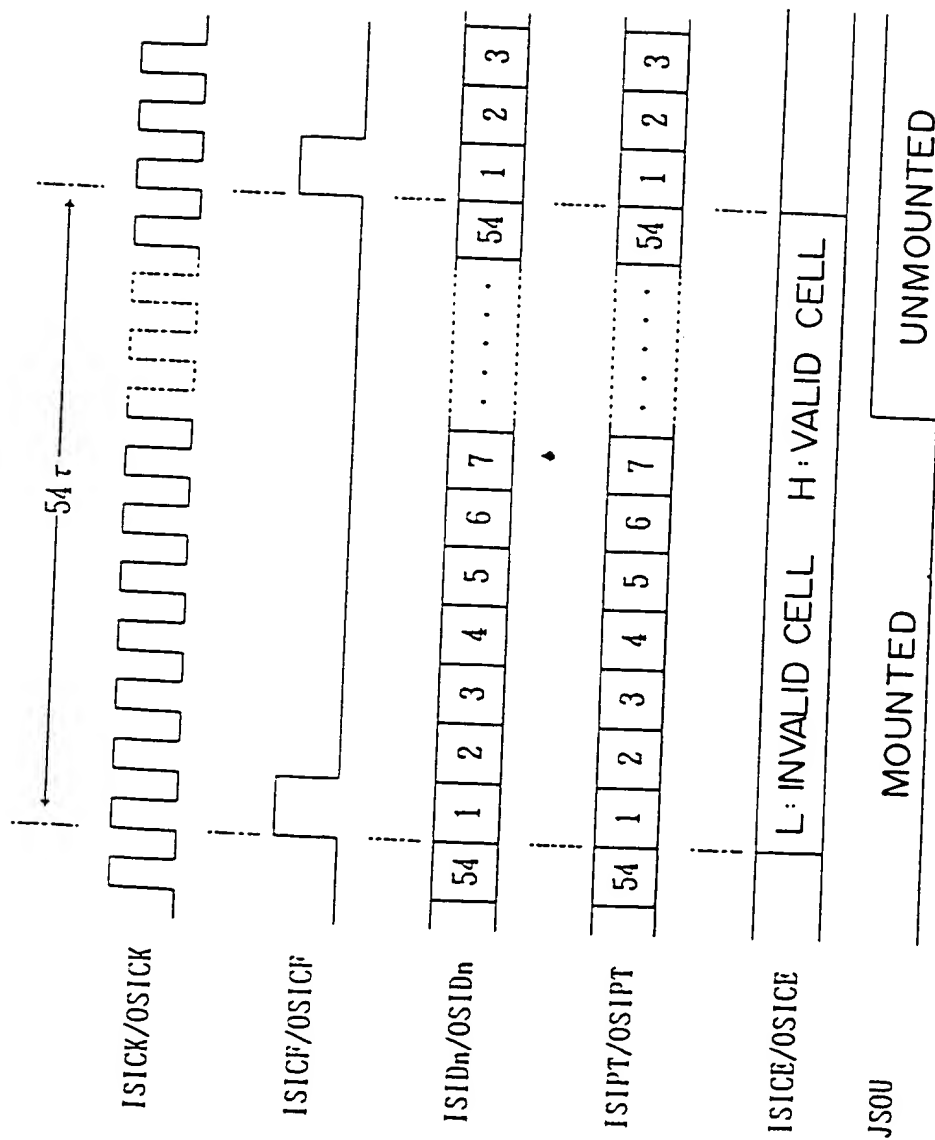


FIG. 97

SYSTEM SELECT SIGNAL		SIFSH-A ACTIVE SYSTEM
SWITCH SELECT INDICATOR IN PRESENT SYSTEM	SWITCH SELECT INDICATOR IN OTHER SYSTEMS	
SELECTING SYSTEM 0	SELECTING SYSTEM 0	SYSTEM 0
SELECTING SYSTEM 1	SELECTING SYSTEM 1	SYSTEM 0
SELECTING SYSTEM 0	SELECTING SYSTEM 1	MAINTAINING OLD SYSTEM
SELECTING SYSTEM 1	SELECTING SYSTEM 0	MAINTAINING OLD SYSTEM

FIG. 99

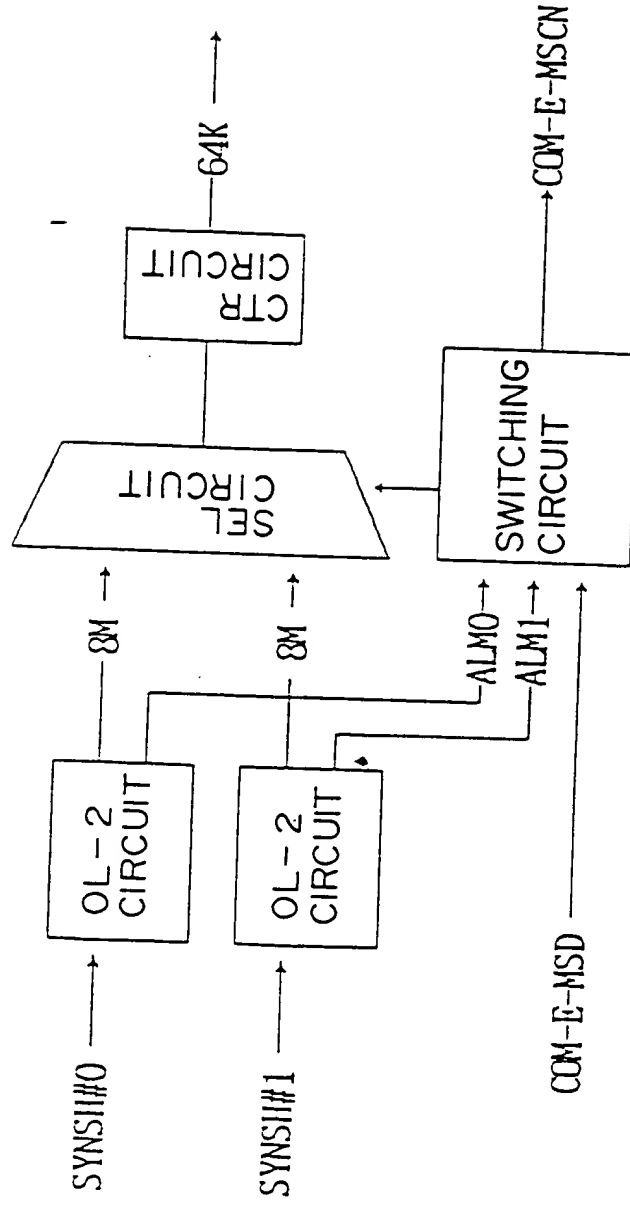


FIG. 100

COM-E-MSD INSTRUCTION		OL-2 CIRCUIT ALARM STATE		SELECTED SYSTEM (COM-E-MSCN)
SYSTEM # 0	SYSTEM # 1	SYSTEM # 0	SYSTEM # 1	
OFF	OFF	○	○	MAINTAINING OLD SYSTEM
ON	OFF	○	○	SYSTEM # 0
OFF	ON	○	○	SYSTEM # 1
(NOTE 1) ON		○	○	MAINTAINING OLD SYSTEM
Don't Care		○	X	SYSTEM # 0
Don't Care		X	○	SYSTEM # 1
Don't Care		X	X	MAINTAINING OLD SYSTEM

NOTE 1 : BOTH SYSTEMS CANNOT BE SELECTED AT COM-E-MSD
WHEN SOFTWARE / FIRMWARE OPERATE NORMALLY.

FIG. 101

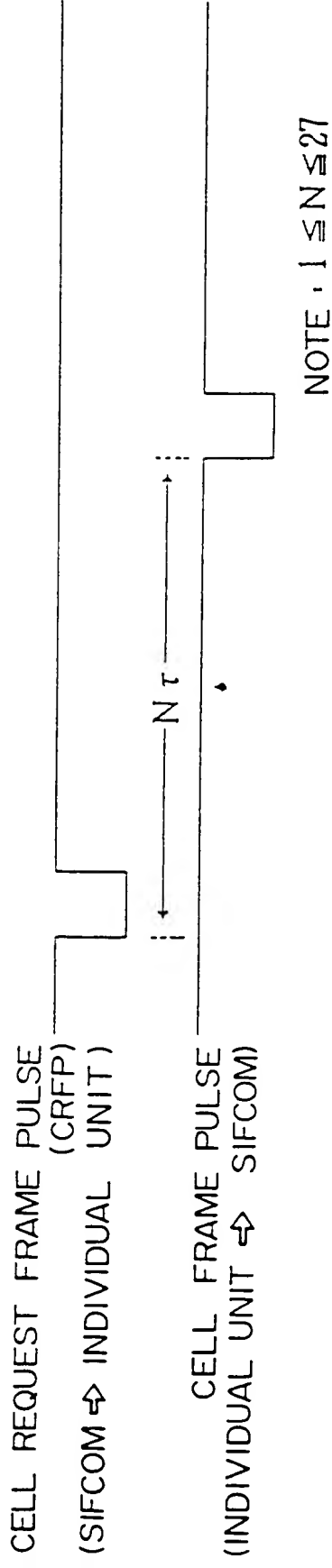


FIG. 103

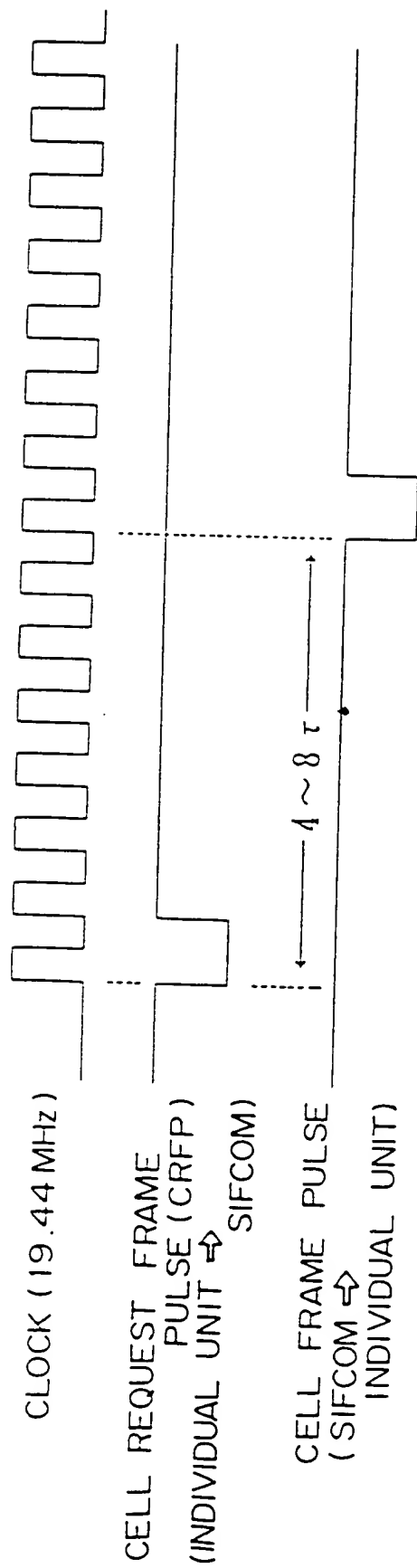


FIG. 104

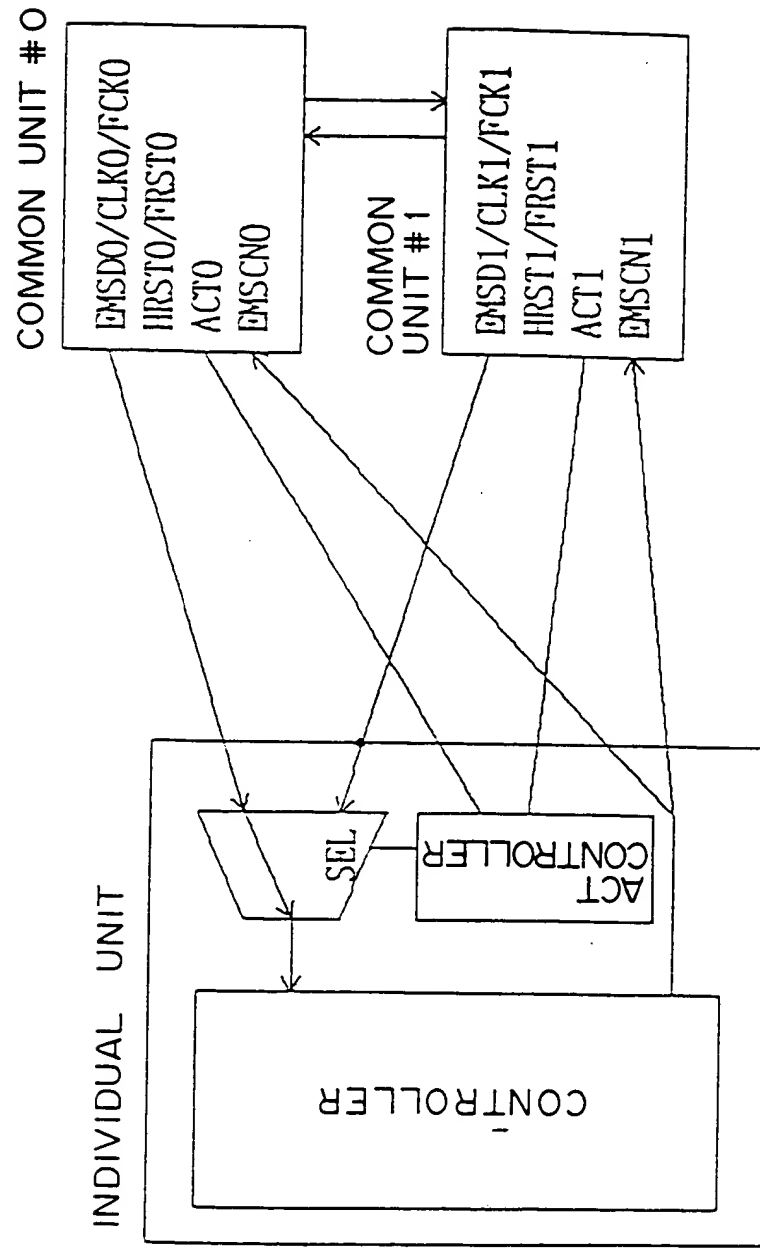


FIG. 105

0927213-03309

ACT0	ACT1	SYSTEM SELECTION
H	H	MAINTAINING PREVIOUS STATE
H	L	#1 ACT
L	H	#0 ACT
L	L	MAINTAINING PREVIOUS STATE

FIG. 106

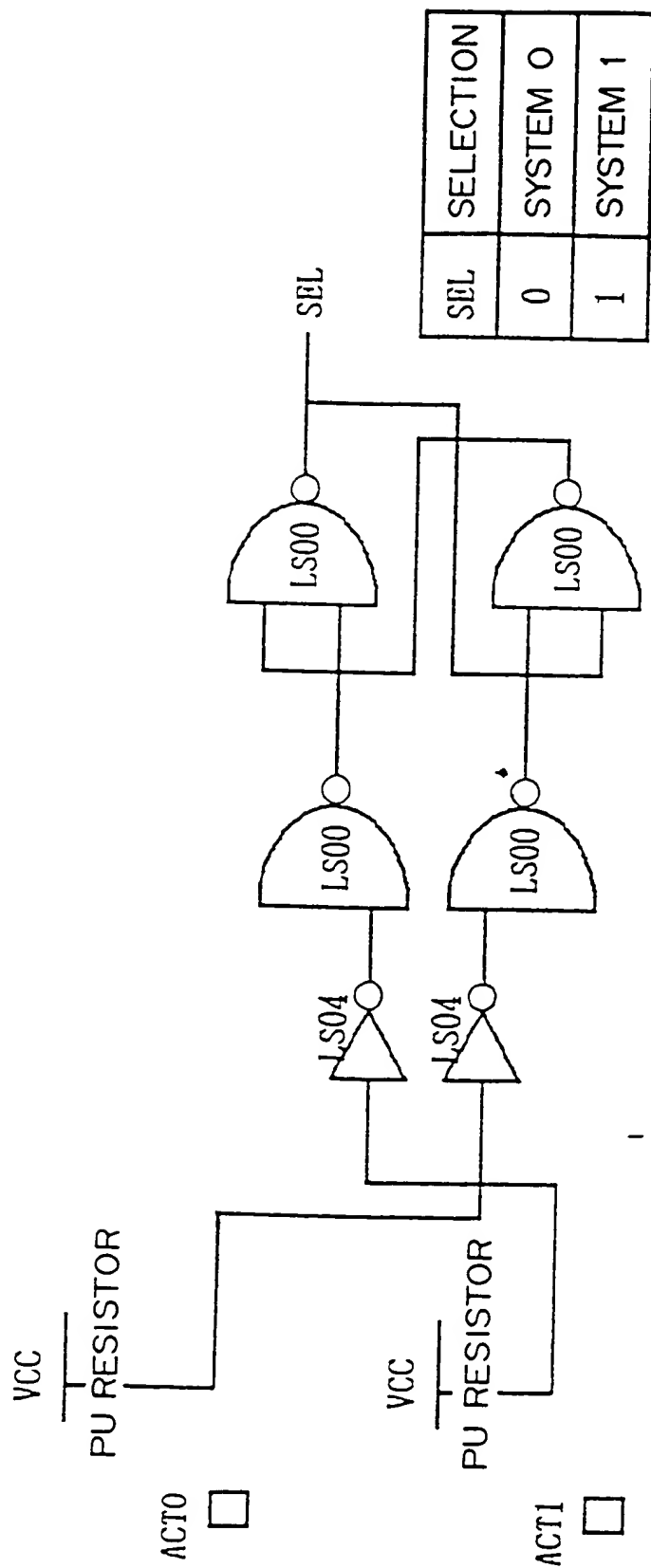


FIG. 107

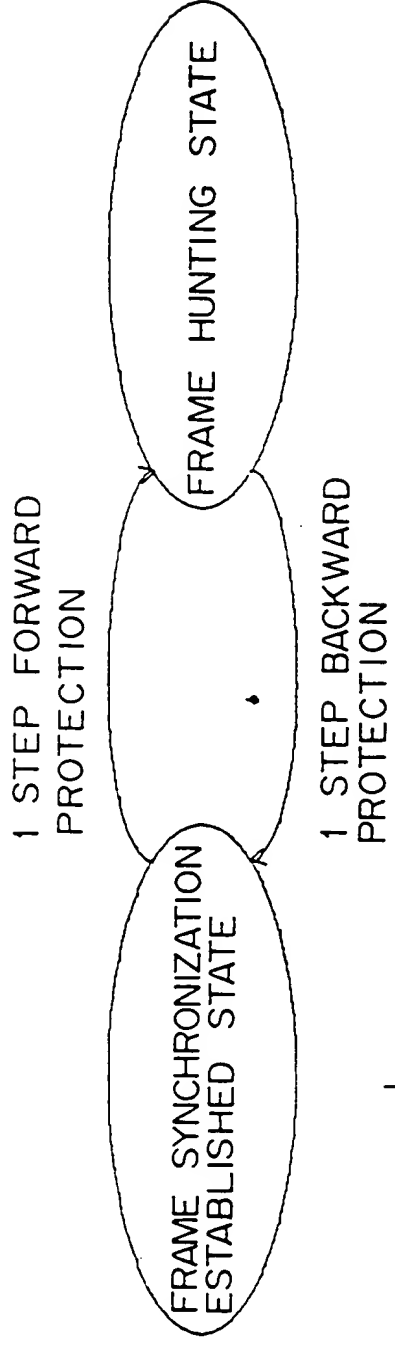
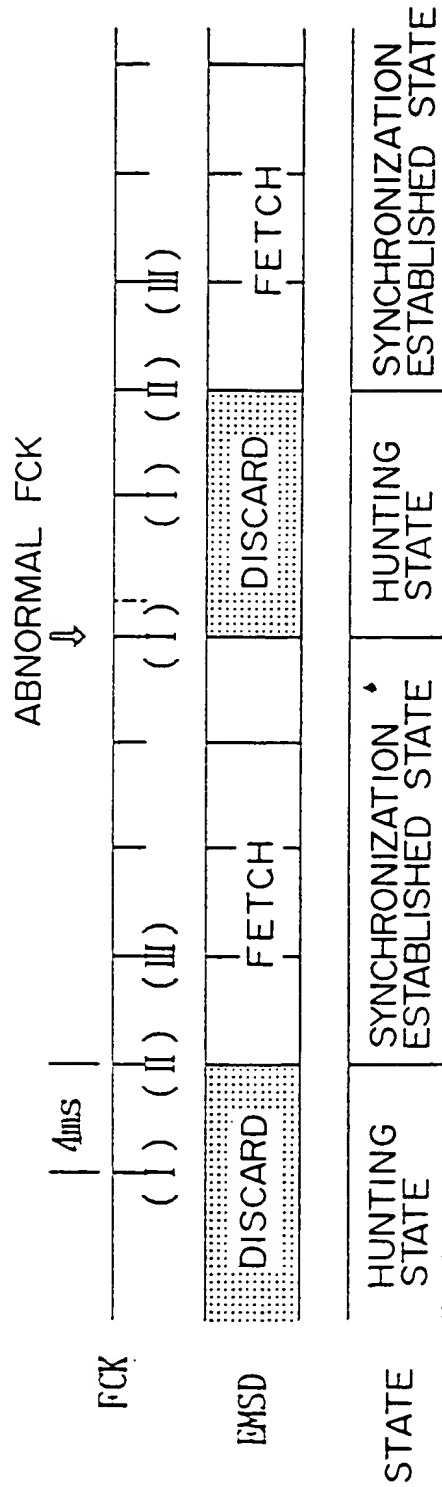


FIG. 109



- (I) FRAME SYNCHRONIZATION START REFERENCE FCK
(II) FIRST NORMAL FCK
(III) SECOND NORMAL FCK

FIG. 110

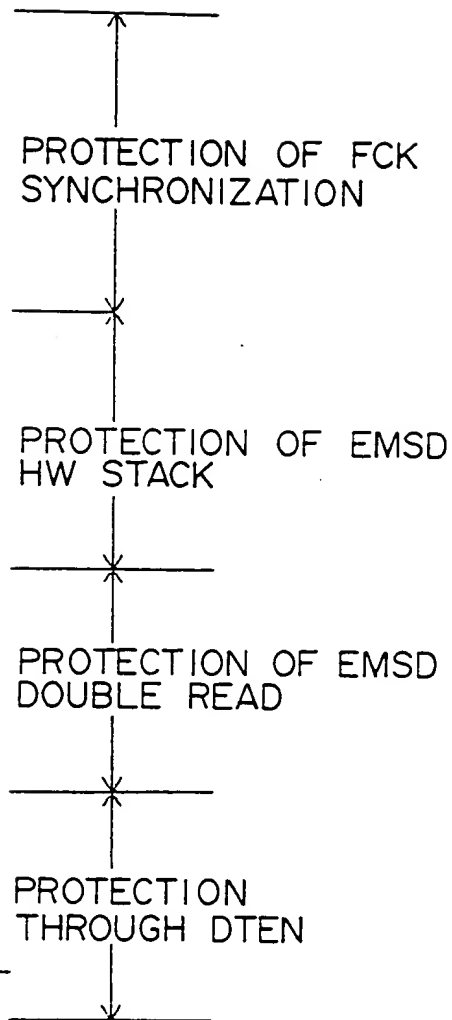
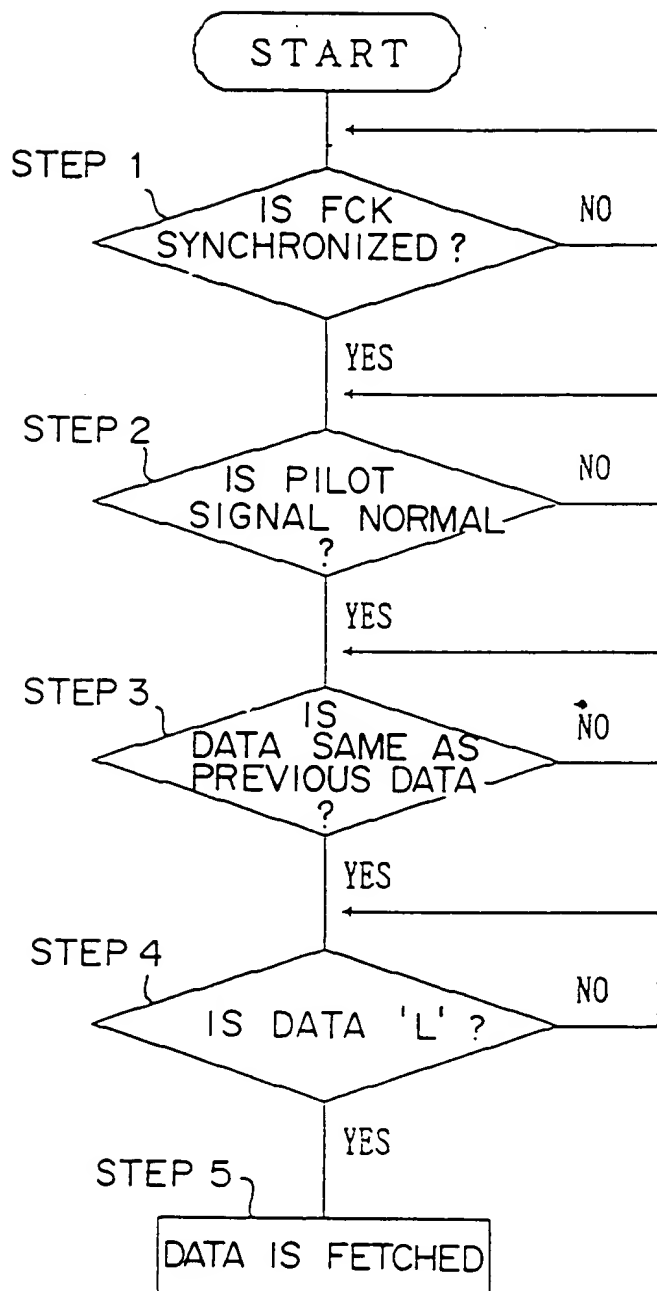
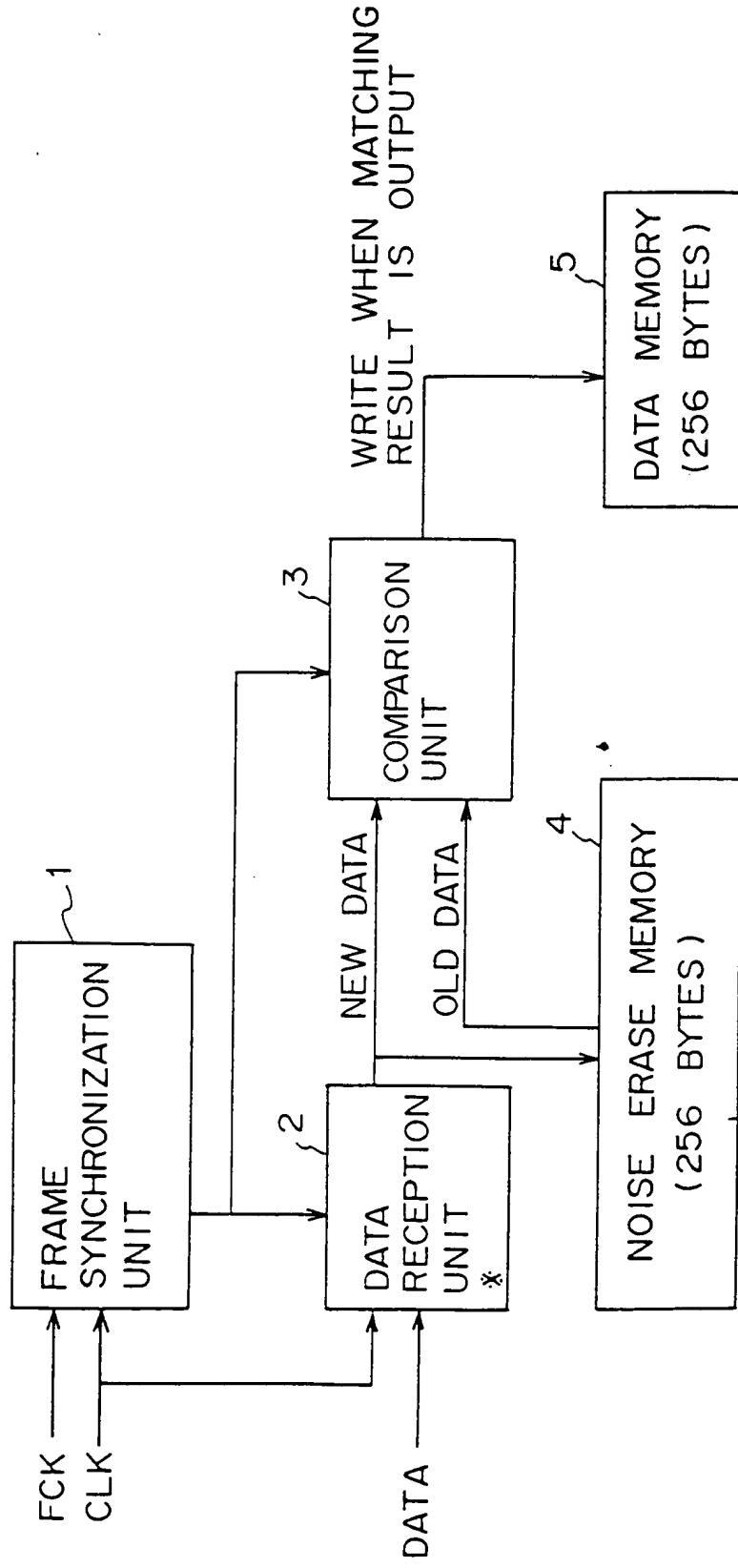


FIG. 112



* : PILOT SIGNAL IS CHECKED AND DTEM MONITOR IS PERFORMED IN THIS BLOCK.

FIG. 113

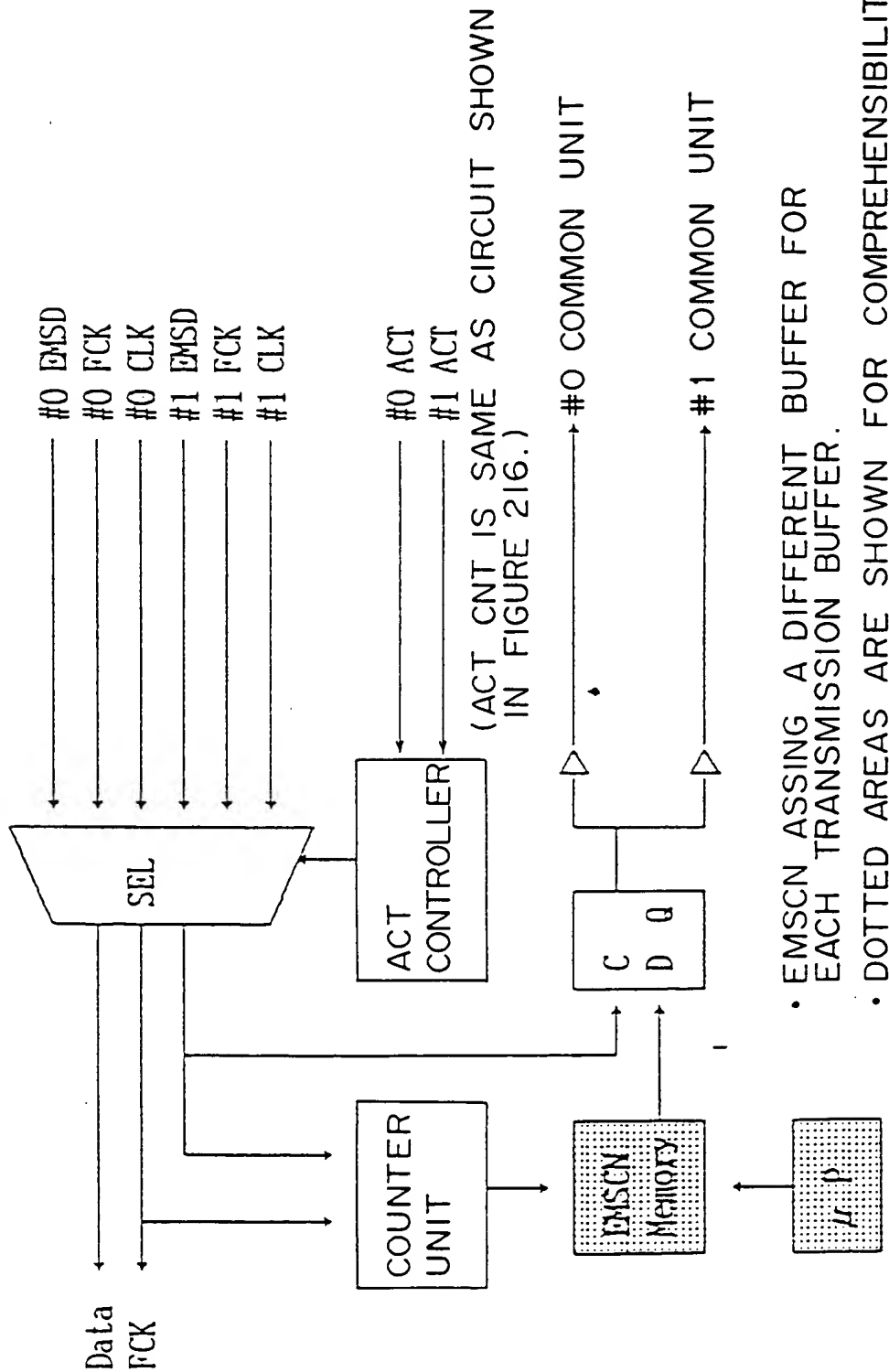


FIG. 114

FAULT	INDIVIDUAL UNIT		COMMON UNIT	
	FAULT DETECTING METHOD	FAULT NOTIFYING METHOD	FAULT DETECTING METHOD	TYPE OF FAULT
EMSD HW STACK	PLT0/1 ASYNCHRONIZATION	EMSCN(PLTF)	EMSCN(PLTF)	EMSD HW STACK
512 CLOCK STACK	INDIVIDUAL UNIT LOCKED	EMSCN STACK	EMSCN PLT0/1 STACK	EMSCN HW STACK
FCK STACK	FCK STACK	EMSCN(SYNCF)	EMSCN(SYNCF)	FCK ASYNCHRONIZATION
EMSCN HW STACK			EMSCN PLT0/1 STACK	EMSCN HW STACK

FIG. 115

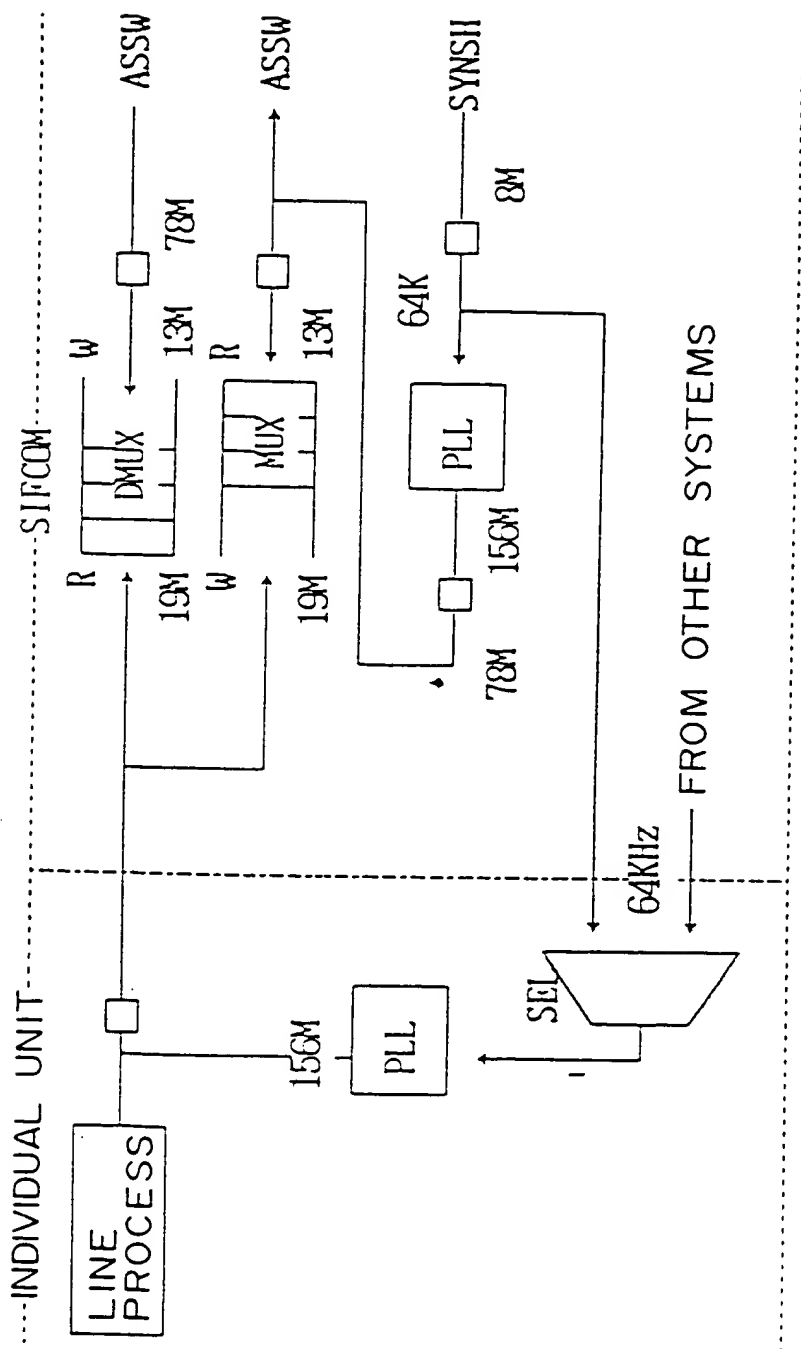


FIG. 116

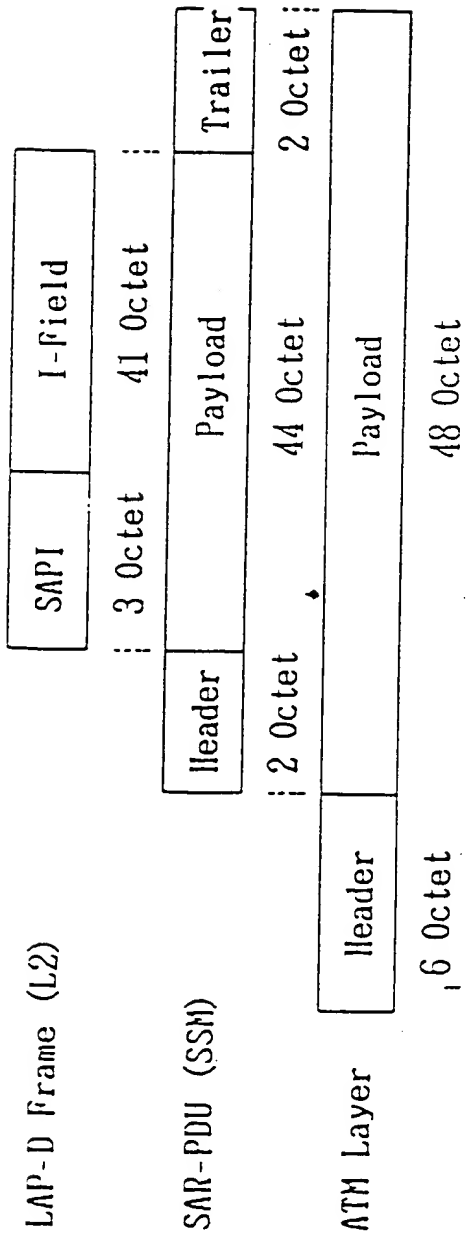
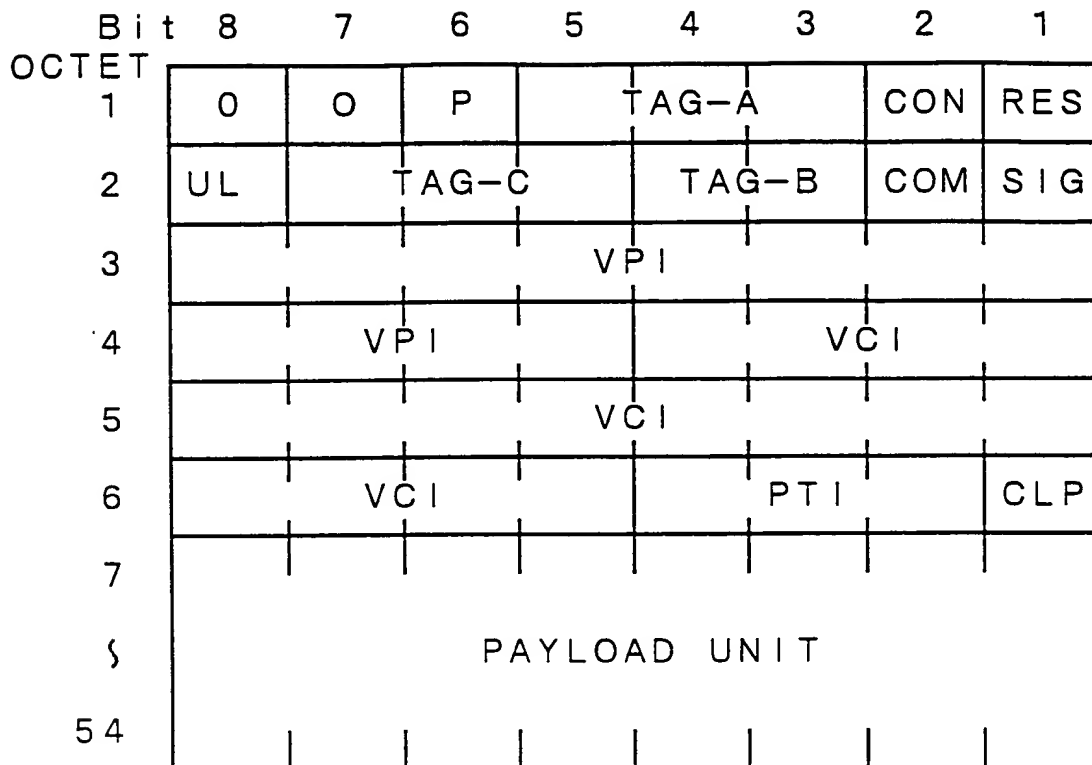
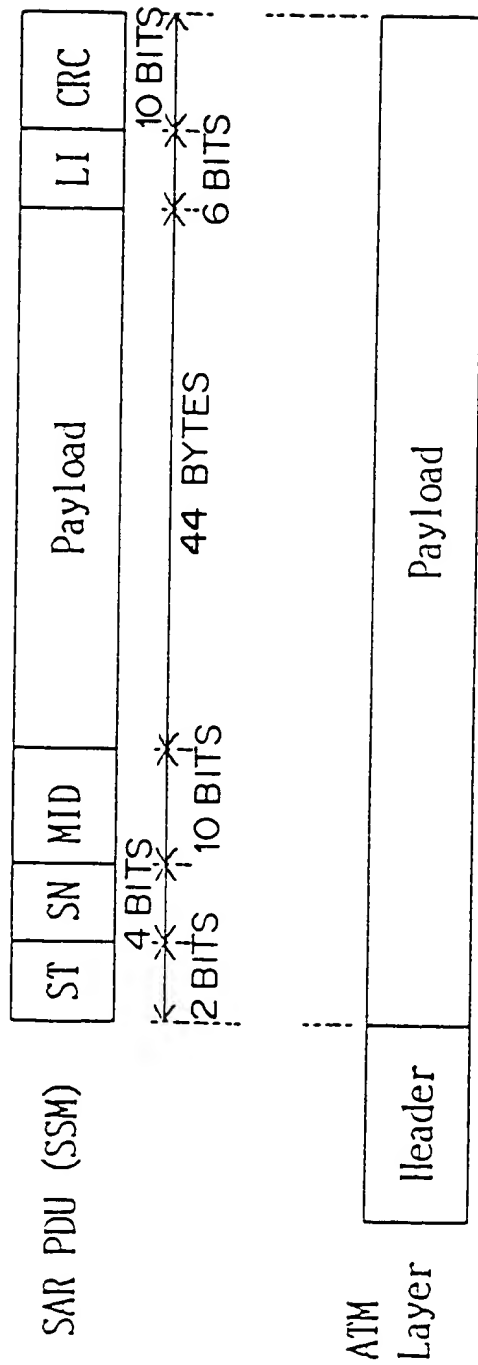


FIG. 117



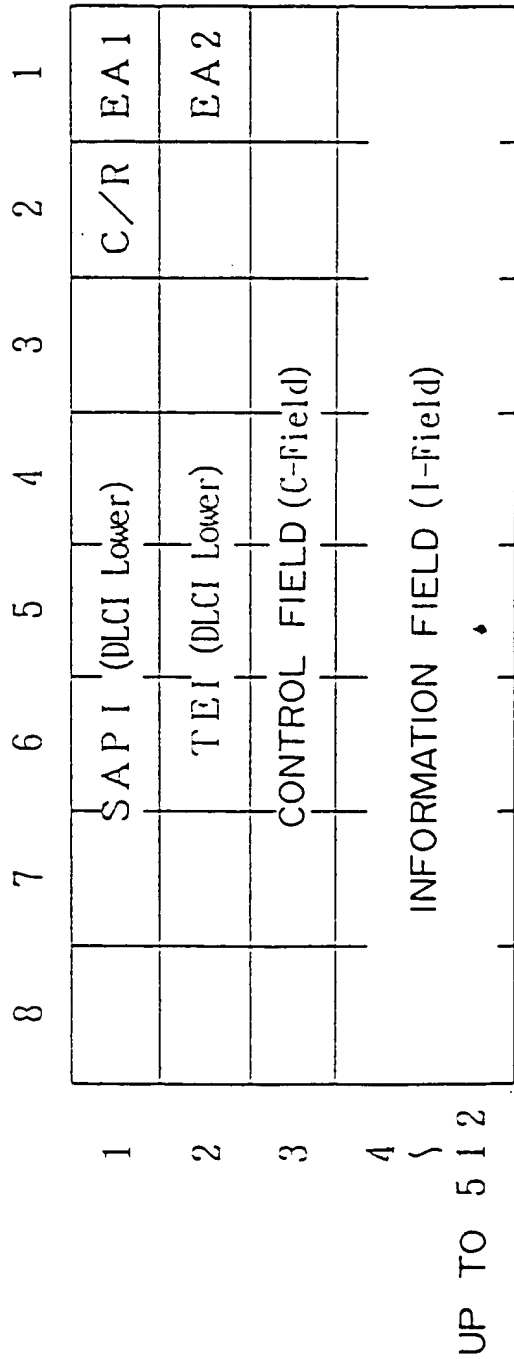
- O : INTERNAL CELL INDICATOR.
INTRA-STATION COMMUNICATIONS CELL IS FIXED TO "1".
- P : QUALITY INDICATOR.
HIGH QUALITY IS FIXED TO "1" BY FIRMWARE.
- CON : HIGH PRIORITY CLASS.
HIGH PRIORITY IS FIXED TO "1" BY FIRMWARE.
- RES : FORCED BLANK CELL INDICATOR. FIXED TO "0".
- COM : COMMON UNIT SIGNALLING SPECIFICATION OF "1"
(COMMON UNIT IS SPECIFIED).
- SIG : SIGNALING SPECIFICATION TAG OF "1" (SIGNALING).
- VPI : FIXED VALUE IS DEFINED
WHEN INTRA-STATION SIGNALING IS ADOPTED.
- VCI : FIXED VALUE IS DEFINED
WHEN INTRA-STATION SIGNALING IS ADOPTED.
- PTI : FIXED VALUE OF "000"
- CLP : FIXED VALUE OF "0"
- TAG-A: CELL ROUTING INDICATOR
- TAG-B: CELL ROUTING INDICATOR
- TAG-C: CELL ROUTING INDICATOR

FIG. 118



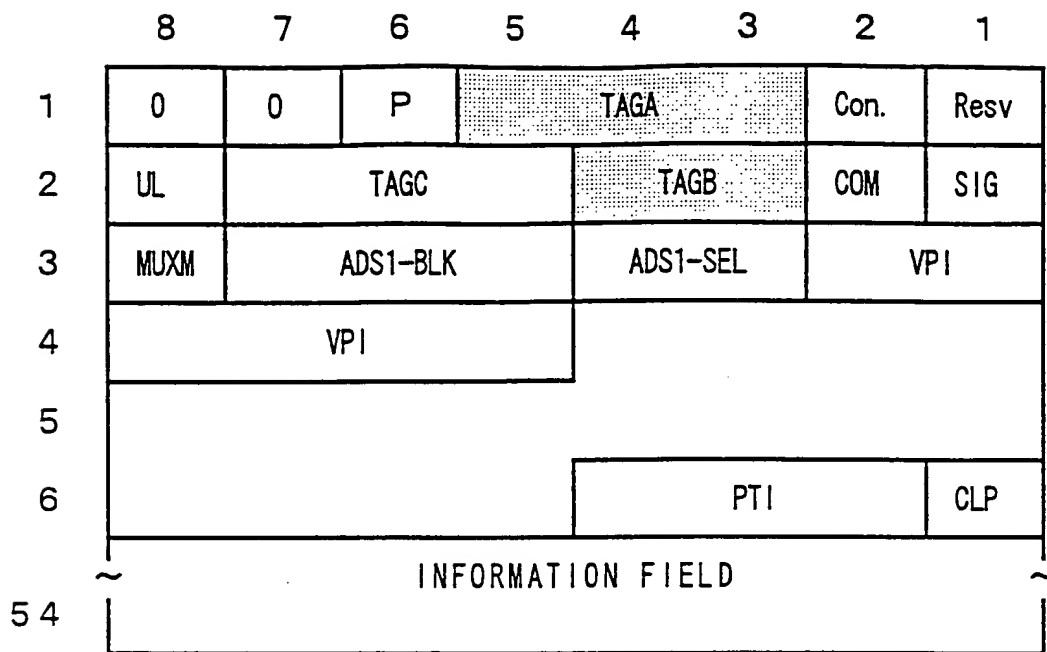
- ST : SEGMENT TYPE (BOM="00"/ COM="01"/ EOM="10"/ SSM="11")
- SN : SEQUENCE NUMBER ("0000" ⇒ "1111" CYCLIC INCREMENT)
- MID : NOT DEFINED WHEN INTRA - STATION SIGNALING IS ADOPTED
(RECEIVED CELL D.C./ TRANSMITTED CELL ALL BITS "0")
- LI : LENGTH INDICATOR (SIGNIFICANT BYTE LENGTH INDICATOR
IN PAYLOAD (BOM, COM, = "101100" SSM, EOM = OPTIONAL LENGTH)
- CRC : CRC (CRC-10 FOR ST, SN, MID, AND PAYLOAD)

FIG. 119



SAP I : ALL BITS ARE SET TO "0" AS FIXED VALUE.
TEI : ALL BITS ARE SET TO "0" AS FIXED VALUE.
C/R : COMMAND = "0" / RESPONSE = "1"
EA 1 : EXTENSION ADDRESS "0" AS FIXED VALUE.
EA 2 : EXTENSION ADDRESS "1" AS FIXED VALUE.
CONTROL FIELD : SABM = "01111111" / UA = "01110011" /
UI = "00000011" / RR = "00000001"

FIG. 120



- 0 : FIXED VALUE (COPY INDICATOR.
'0" INDICATES ONE TO ONE TRANSMISSION)
- 0 : INTERNAL TEST CELL INDICATOR ('0" INDICATES
A USER CELL WHILE '1" INDICATES INTERNAL CELL)
- P : HIGH PRIORITY CLASS ('0" FOR HIGHER PRIORITY;
AND '1" FOR LOWER PRIORITY.)
- Con. : CONGESTION CONTROL (IMPORTANT CALLS
FROM POLICE AND FIRE DEPARTMENTS ARE IDENTIFIED)
- Resv : RESERVE BITS
USED TO IDENTIFY INSIGNIFICANT CELL
WHEN SYSTEMS ARE SWITCHED IN BSGCSH.
- TAGA : 2.4G 4×4 HIGHWAY IS SELECTED IN SW (AHM SPECIFICATION)
(2 BITS ONLY ARE UNED IN 3 BITS. POSITION AND POLARITY
OF REMAINING ONE BIT ARE NOT CHECKED.)
- TAGB : 2.4G 622M×4 HIGHWAY IS SELECTED IN SW (AHM SPECIFICATION)
USED AS UL IN RMXSH
- TAGC : SELECTING 622M → 156M HIGHWAY -
- UL : HIGHER/LOWER ORDER IN DAISY CHAIN
- COM : SELECTING COMMON UNIT
USED TO IDENTIFY CELL FROM SIMPLEX/DUPLEX DEVICE IN BSGCSH.
- SIG : IDENTIFICATION OF INTRA-STATION LAP CELL
- MUXM : FOR DS1 CARDS IN AND AFTER MUX MULTICAST BIT MUX
- ADS1-SEL : SELECTING ADS1 CARD

FIG. 121

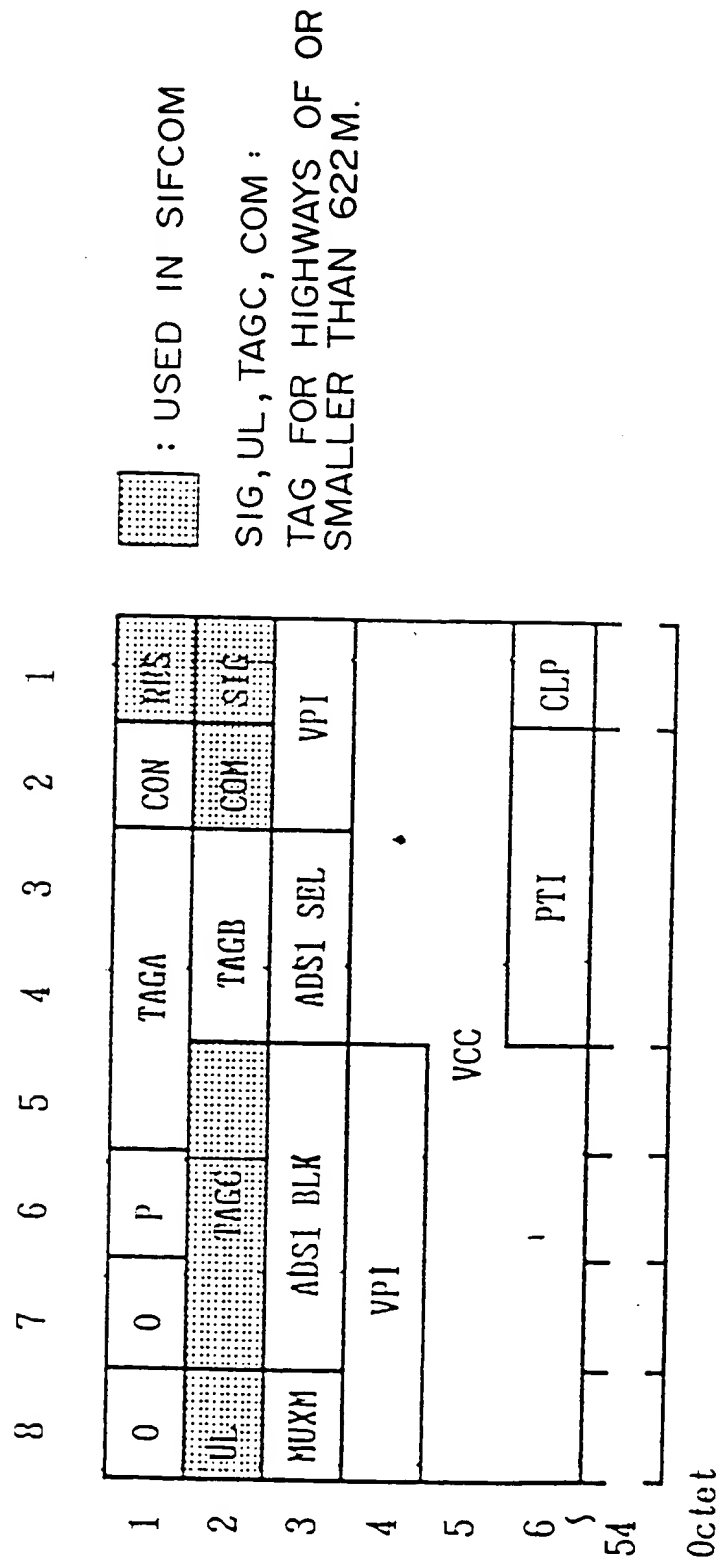
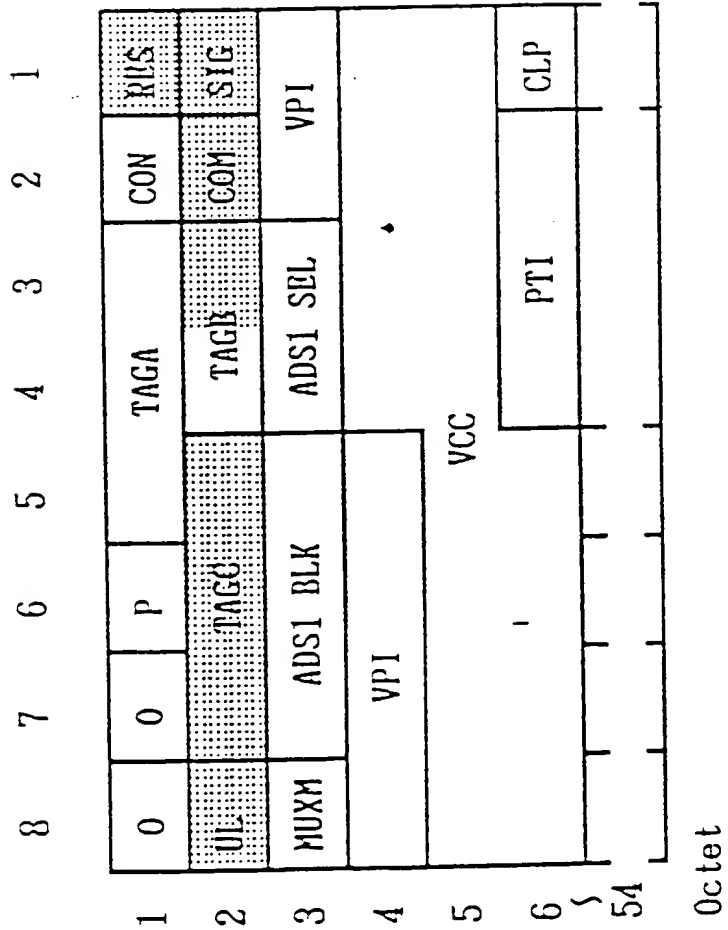


FIG. 122

SIG	UL	TAGC	COM	TRANSMISSION LINE
0/1	0	000	0	SIFSH#0 LINE0/SIGNALING
0/1	0	001	0	SIFSH#0 LINE1/SIGNALING
		}		}
0/1	0	111	0	SIFSH#0 LINE7/SIGNALING
0/1	1	000	0	SIFSH#1 LINE0/SIGNALING
0/1	1	001	0	SIFSH#1 LINE1/SIGNALING
		}		}
0/1	1	111	0	SIFSH#1 LINE7/SIGNALING
1	0	000	1	SIFSH#0 COM SIGNALING
1	1	000	1	SIFSH#1 COM SIGNALING

FIG. 123




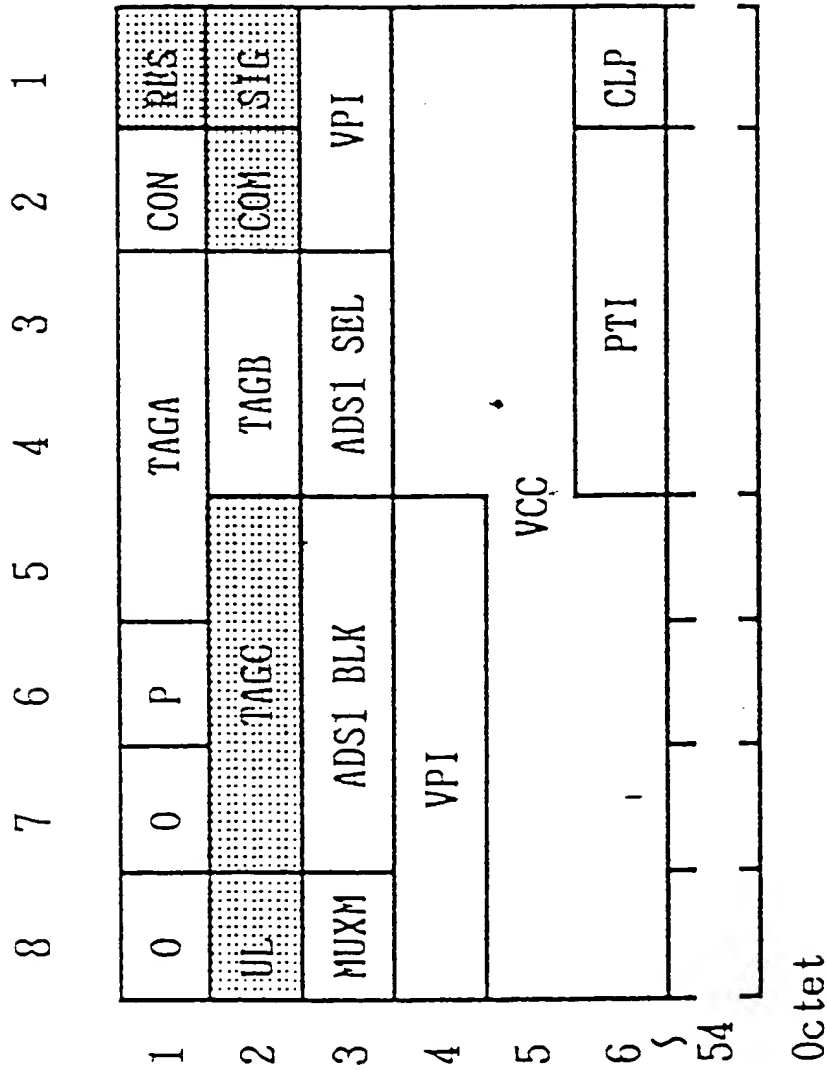
 : USED IN RMUXCOM
SIG, UL, TAGB, TAGC,
COM :
TAG FOR HIGHWAYS OF SMALLER
THAN 622M (ONLY LOWEST BIT
OF TAGB IS USED)

FIG. 124

SIG	UL	TAGB	TAGC	COM	TRANSMISSION LINE
0/1	0	0	000	0	RMUXSH#0 LINE0 / SIGNALING
0/1	0	0	001	0	RMUXSH#0 LINE1 / SIGNALING
			}		
0/1	0	0	111	0	RMUXSH#0 LINE7 / SIGNALING
0/1	1	0	000	0	RMUXSH#1 LINE0 / SIGNALING
0/1	1	0	001	0	RMUXSH#1 LINE1 / SIGNALING
			}		
0/1	1	0	111	0	RMUXSH#1 LINE7 / SIGNALING
0/1	1	1	000	0	RMUXSH#2 LINE0 / SIGNALING
0/1	1	1	001	0	RMUXSH#2 LINE1 / SIGNALING
			}		
0/1	1	1	111	0	RMUXSH#2 LINE7 / SIGNALING
1	0	0	000	1	RMUXSH#0 COM SIGNALING
1	1	0	000	1	RMUXSH#1 COM SIGNALING
1	1	1	000	1	RMUXSH#2 COM SIGNALING

FIG. 125



: USING BSGC - COM

SIG, UL, TAGC :

TAG FOR HIGHWAYS OF
OR SMALLER THAN 622M.

COM :

SIGNALING CELL FROM
SIMPLEX / DUPLEX UNITS

RES :

WHEN SYSTEMS ARE
SWITCHED

FIG. 126

SIG	ADS1 BLK	ADS1 SEL	
0	000 — } 1 1	0 0 } 1 1	USER CELL TO DTC 0/ Line 0 USER CELL TO DTC 0/ Line 3
0	111 — } 1 1	0 0 } 1 1	USER CELL TO DTC 7/ Line 0 USER CELL TO DTC 7/ Line 3
1	000 — } 1 1	0 0 } 1 1	LAP CELL TO DTC 0/ Line 0 LAP CELL TO DTC 0/ Line 3
1	111 — } 1 1	0 0 } 1 1	LAP CELL TO DTC 7/ Line 0 LAP CELL TO DTC 7/ Line 3

FIG. 128

669220-1

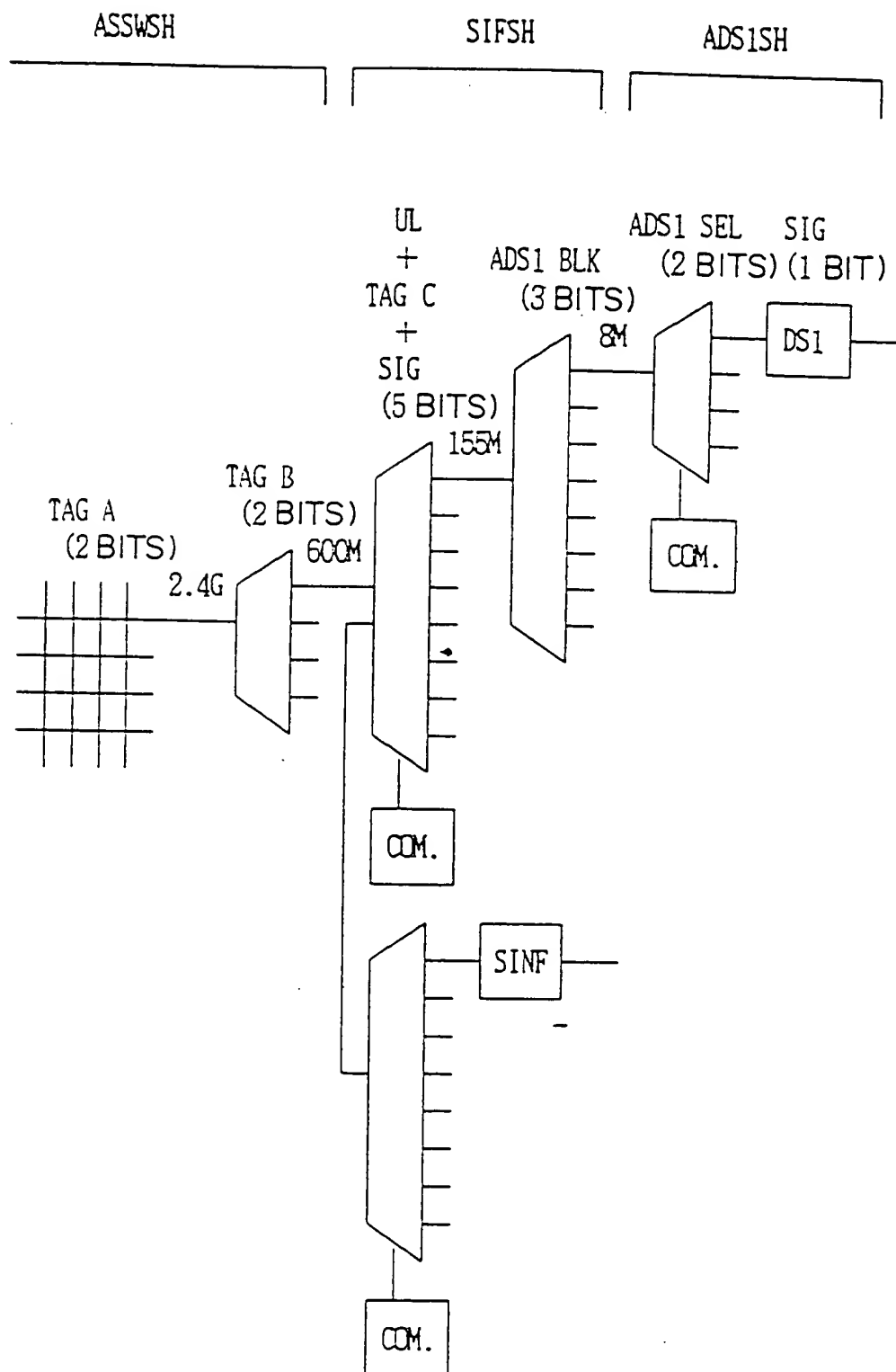


FIG. 129

66360-172200

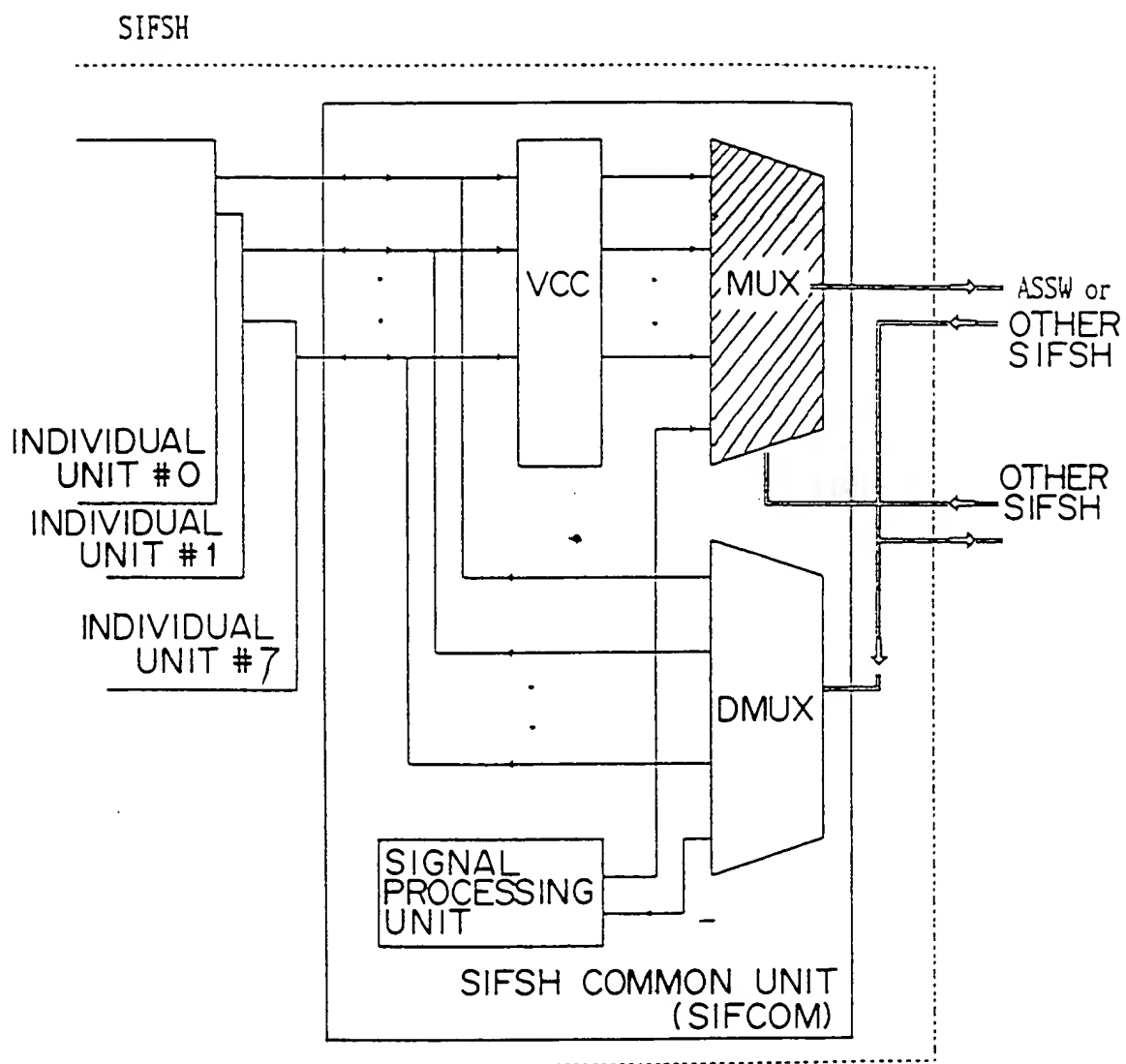
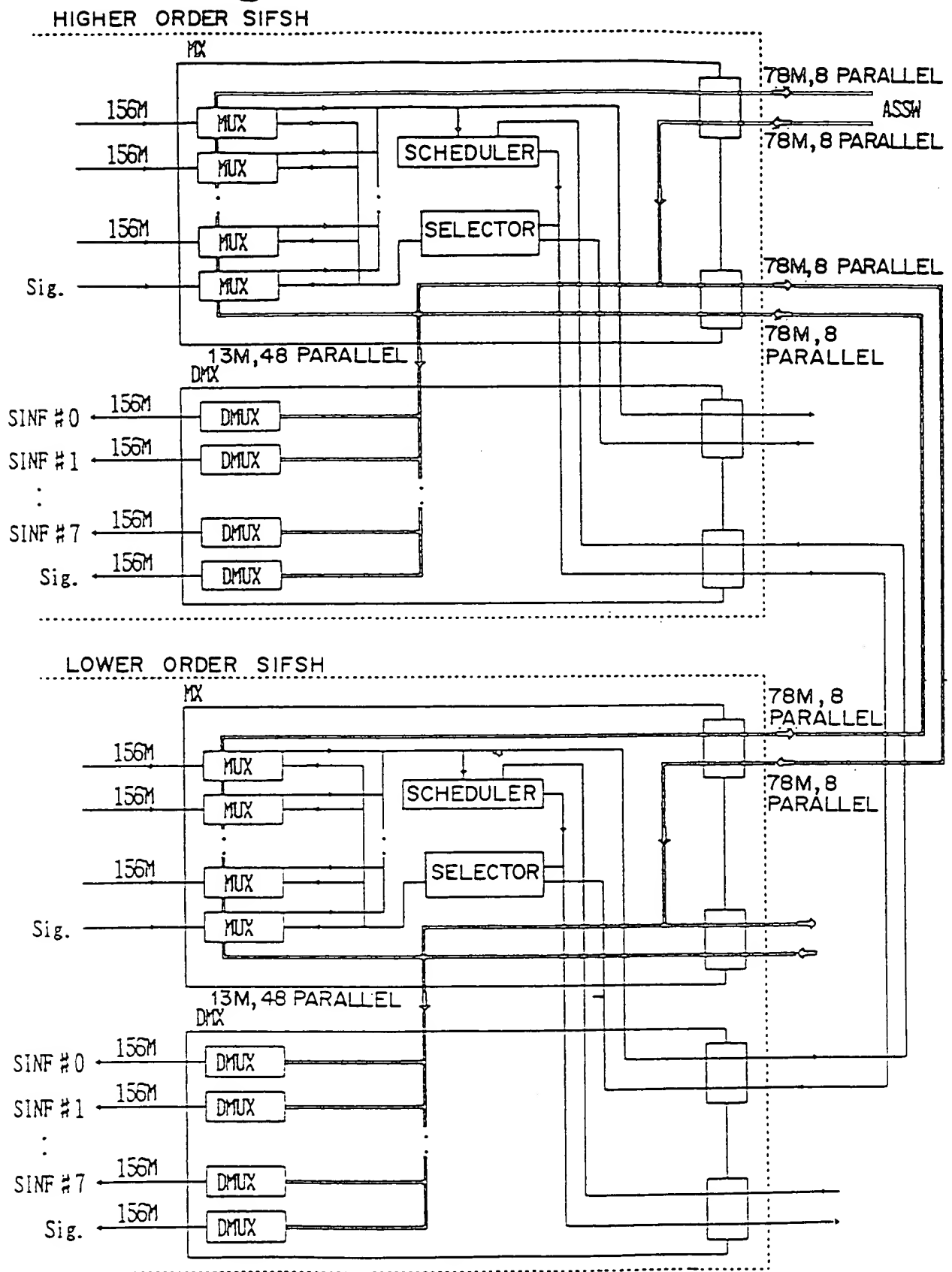


FIG. 130

66560-672260



SELECTOR: LOWER ORDER DEVICE IN DAISY CHAIN SELECTS SIGNAL FROM HIGHER ORDER.

FIG. 131

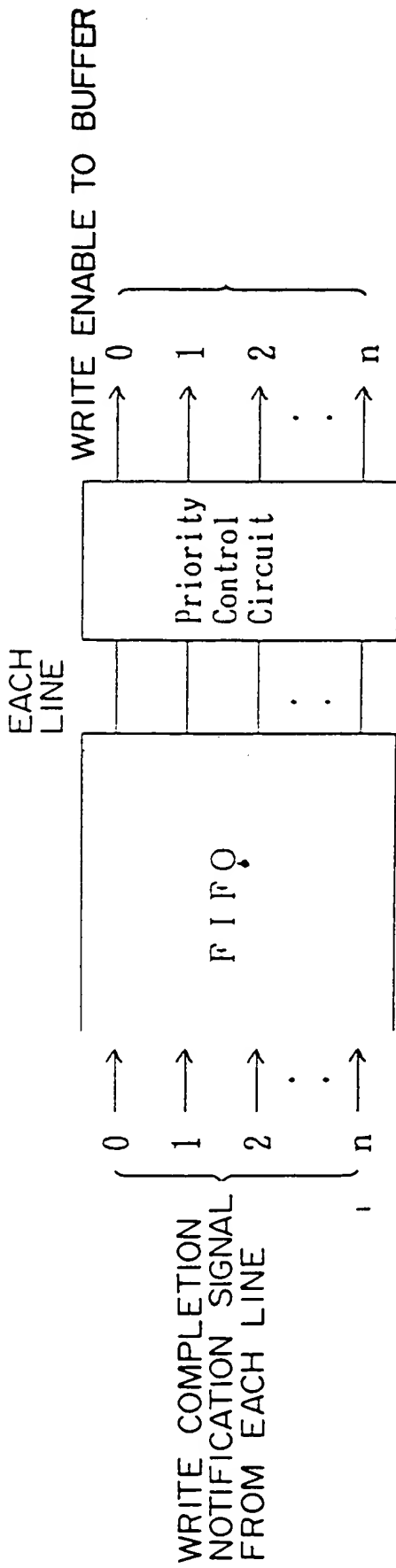
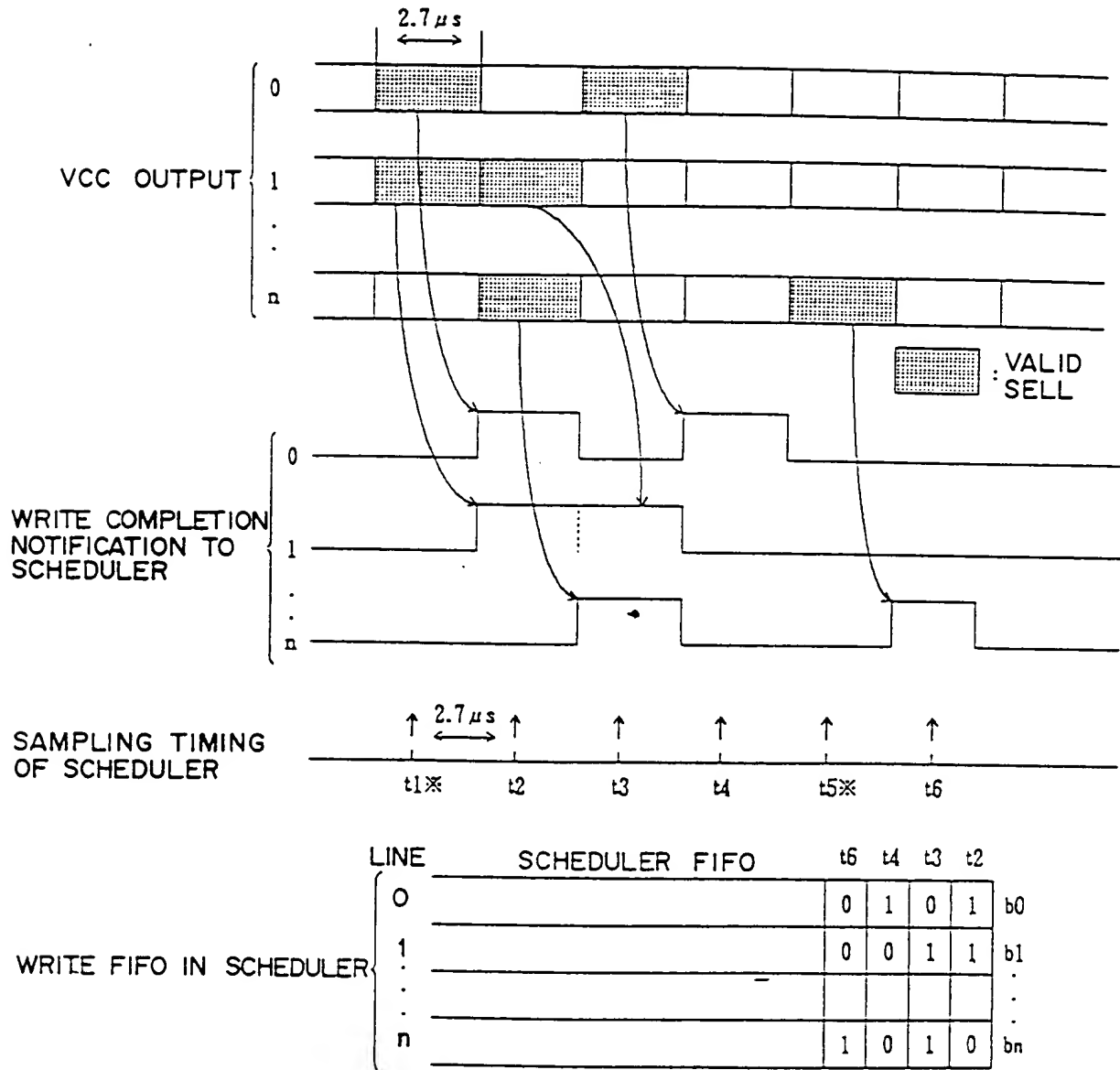
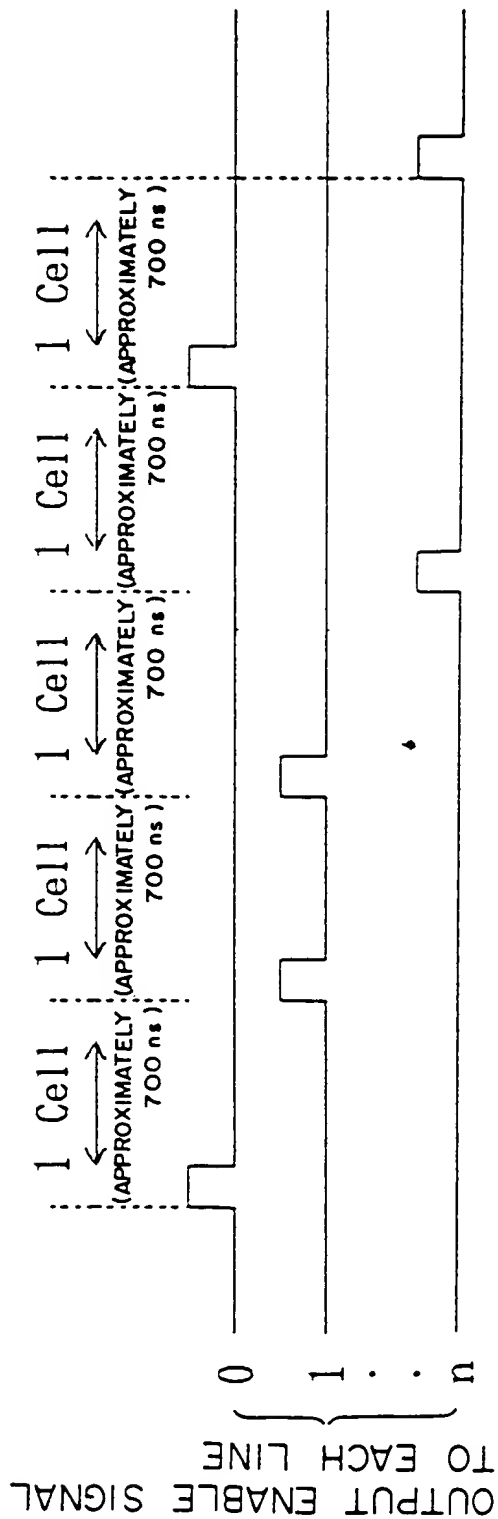


FIG. 133



* NO DATA IS WRITTEN TO FIFO AT TIMING AT WHICH NO CELLS EXIST IN ALL LINES.

FIG. 134



* WHEN FIFO DATA EQUAL TO OR LARGER THAN B2 AND SMALLER THAN BN IS ALLOWED

FIG. 135

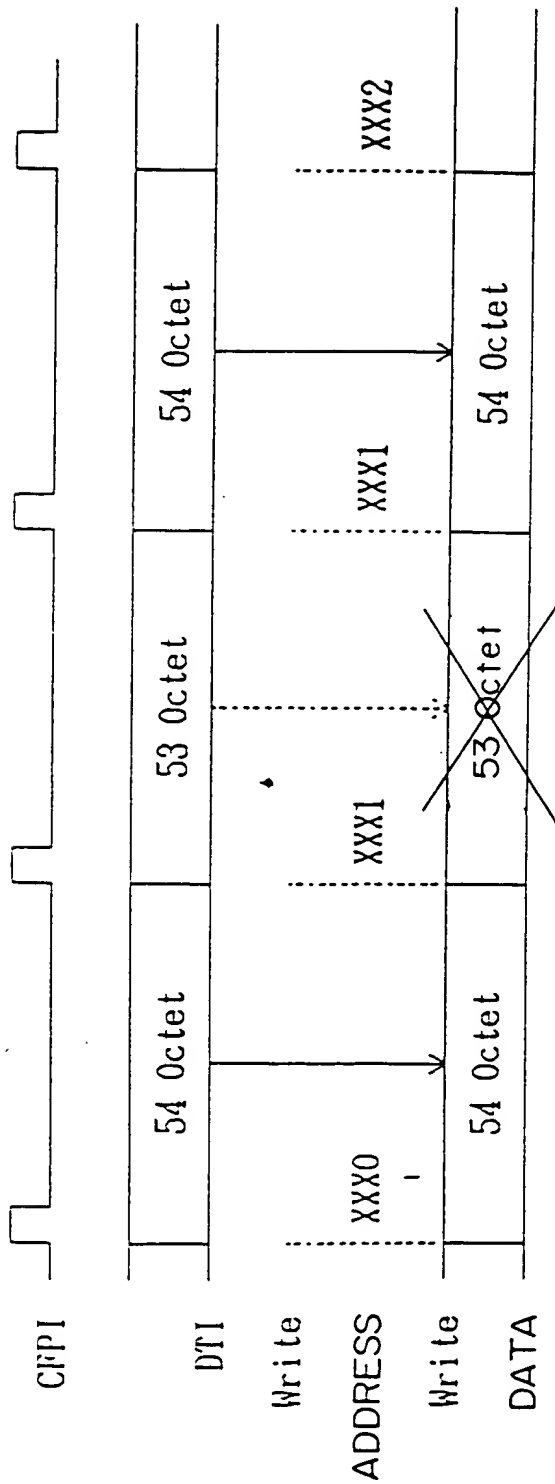


FIG. 136

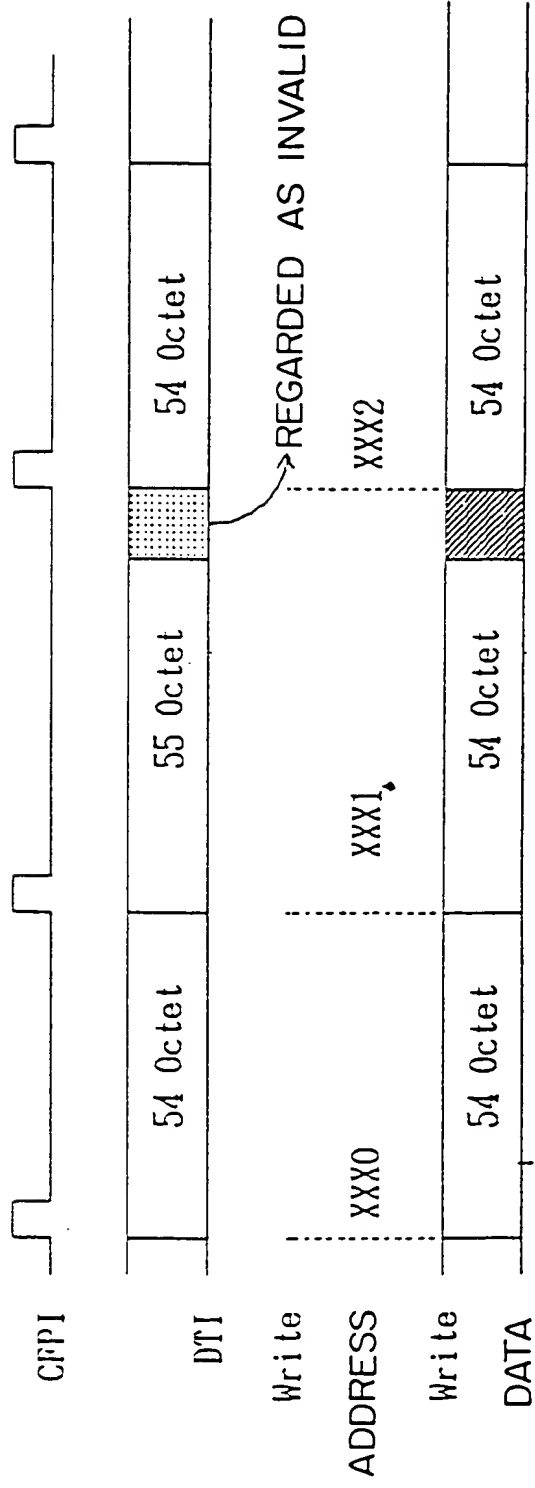


FIG. 137

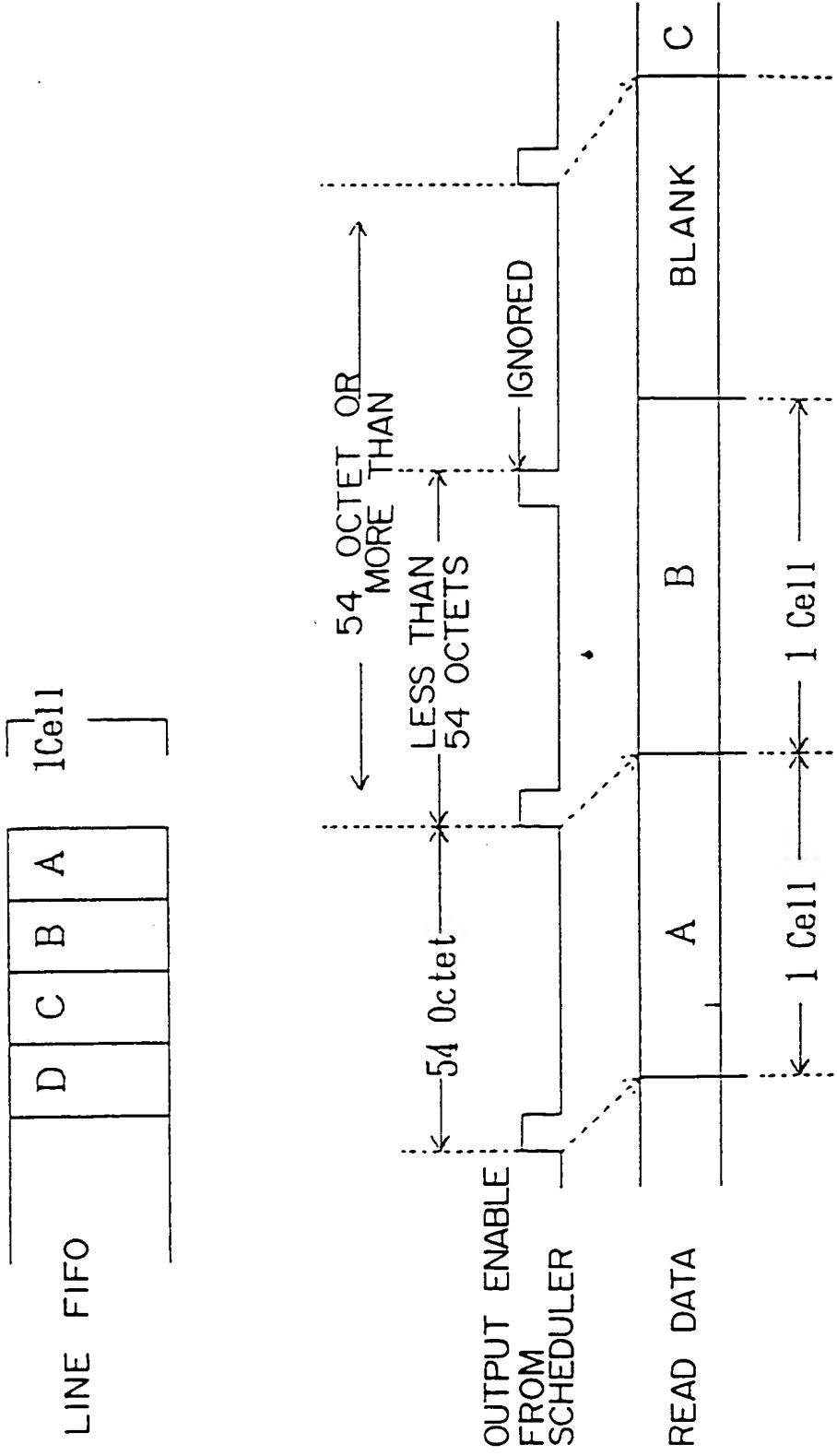
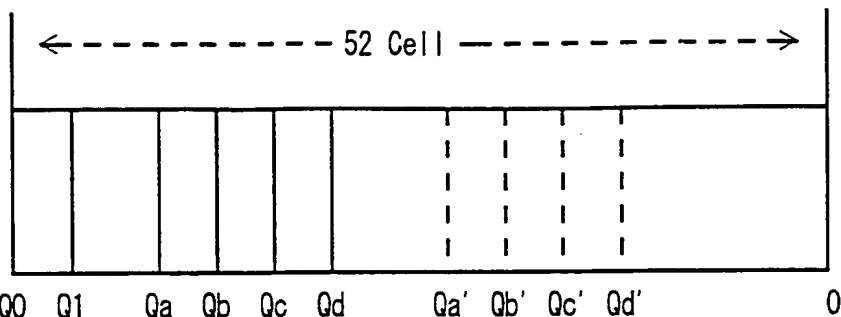


FIG. 138



- Q0 : PHYSICAL MAXIMUM OF BUFFER
- Q1 : PHYSICAL MAXIMUM OF BUFFER
- Qa : CELL DISCARD PROCESS STARTING THRESHOLD
OF CELL HAVING "P" BIT= "0", "CON" BIT= "0"
- Qb : CELL DISCARD PROCESS STARTING THRESHOLD
OF CELL HAVING "P" BIT= "0", "CON" BIT= "1"
- Qc : CELL DISCARD PROCESS STARTING THRESHOLD
OF CELL HAVING "P" BIT= "1", "CON" BIT= "0"
- Qd : CELL DISCARD PROCESS STARTING THRESHOLD
OF CELL HAVING "P" BIT= "1", "CON" BIT= "1"
- Qa' : CELL DISCARD PROCESS RELEASING THRESHOLD
OF CELL HAVING "P" BIT= "0", "CON" BIT= "0"
- Qb' : CELL DISCARD PROCESS RELEASING THRESHOLD
OF CELL HAVING "P" BIT= "0", "CON" BIT= "1"
- Qc' : CELL DISCARD PROCESS RELEASING THRESHOLD
OF CELL HAVING "P" BIT= "1", "CON" BIT= "0"
- Qd' : CELL DISCARD PROCESS RELEASING THRESHOLD
OF CELL HAVING "P" BIT= "1", "CON" BIT= "1"

F I G. 139

669360-672220

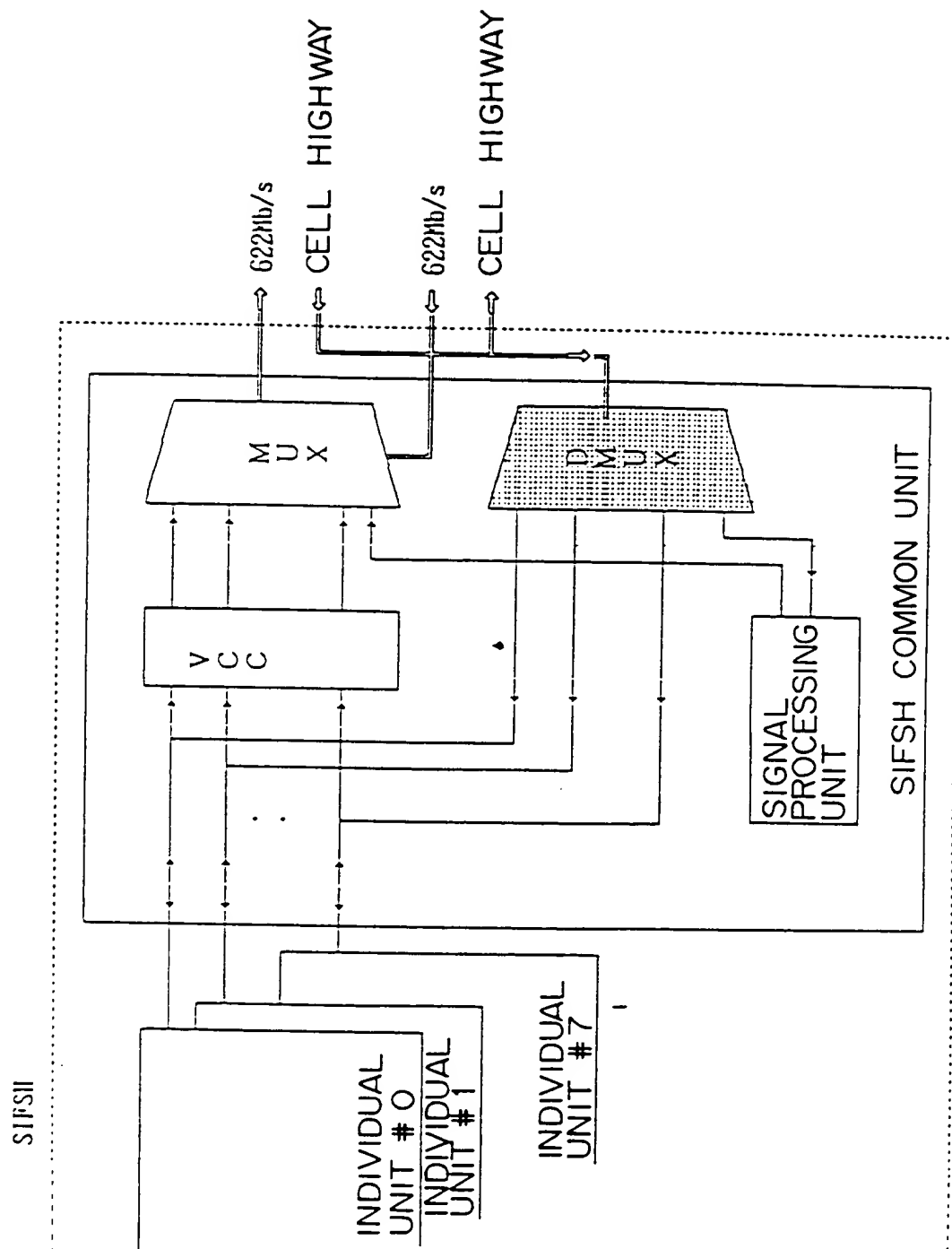


FIG. 140

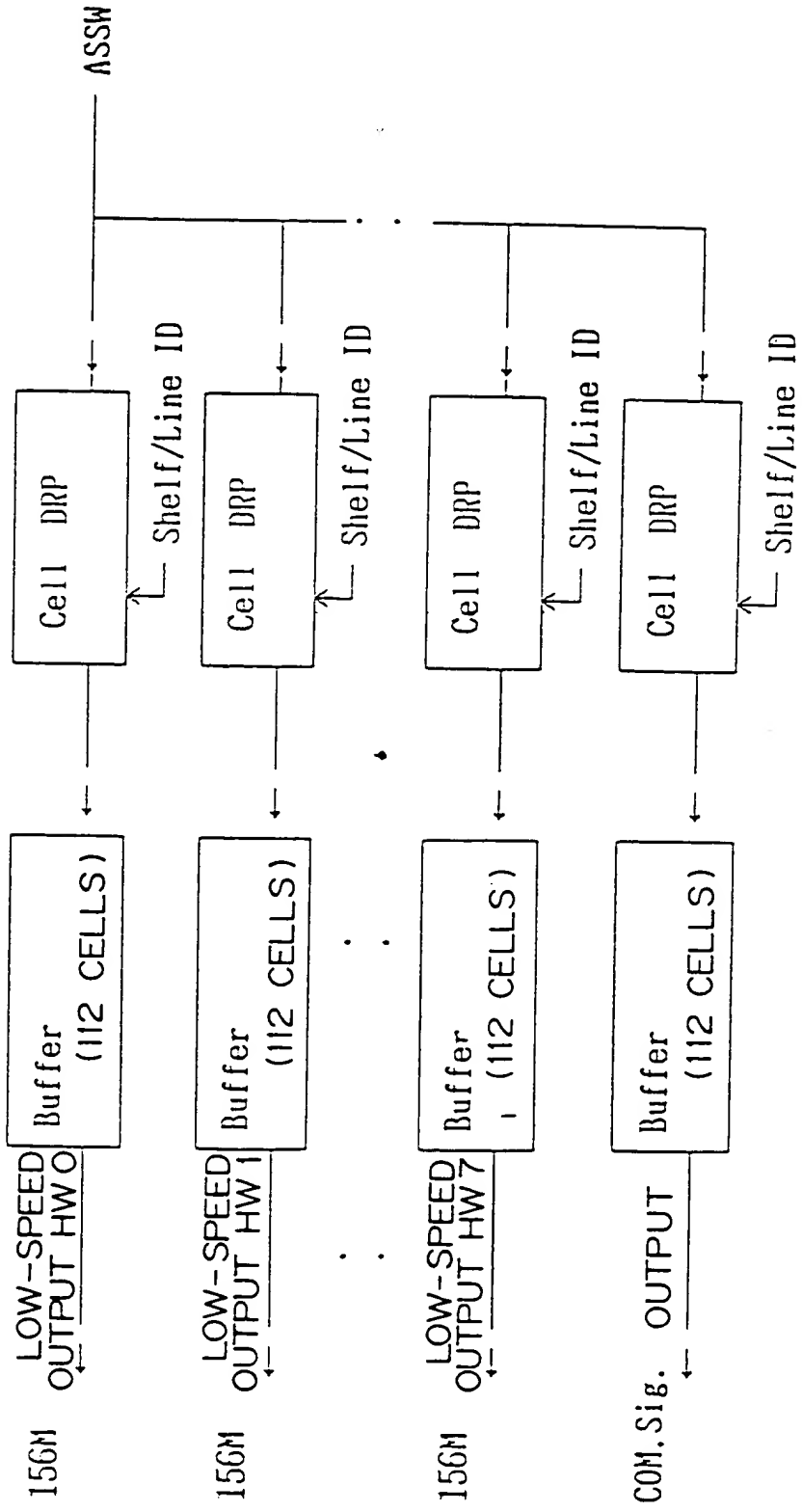
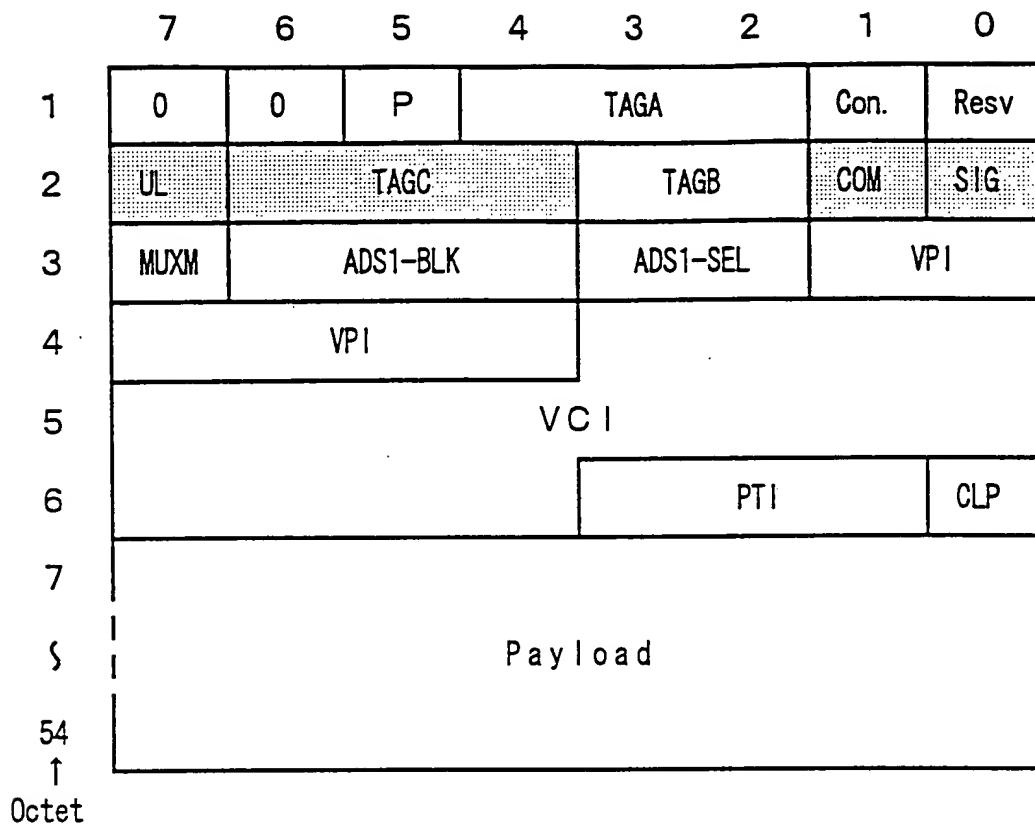


FIG. 141



- "0" : ONE-TO-ONE COMMUNICATIONS MODE (NO COPY MODE)
 0 : INTERNAL TEST CELL INDICATOR
 ('0':USER CELL, '1':INTERNAL CELL)
 P : QUALITY INDICATOR
 CON : PRIORITY CLASS INDICATOR
 RES : RESERVE BITS
 PTI : PAYLOAD TYPE
 TAGA : 2.4G 4×4 TAG
 TAGB : 2.4G → 600M 4 HIGHWAY TAG
 COM : SELECTING COMMON UNIT
 SIG, UL, TAGC : TAG FOR SMALLER THAN 600M
 MUXM : MUX MULTICAST
 ADS1 BLK : TAG FROM MUX TO ADS1 BLOCK
 ADS1 SEL : TAG TO ADS1
 : USED IN SIFCOM DMUX

FIG. 142

SIG	UL	TAGC	COM	TRANSMISSION LINE
0/1	0	0 0 0	0	SIFSH0 Line #0/Signal
0/1	0	0 0 1	0	" Line #1/Signal
		}		
0/1	0	1 1 1	0	SIFSH0 Line #7/Signal
0/1	1	0 0 0	0	SIFSH1 Line #0/Signal
0/1	1	0 0 1	0	" Line #1/Signal
		}		
0/1	1	1 1 1	0	SIFSH1 Line #7/Signal
1	0	0 0 0	1	SIFSH0 Common Signal
1	1	0 0 0	1	SIFSH1 Common Signal

FIG. 143

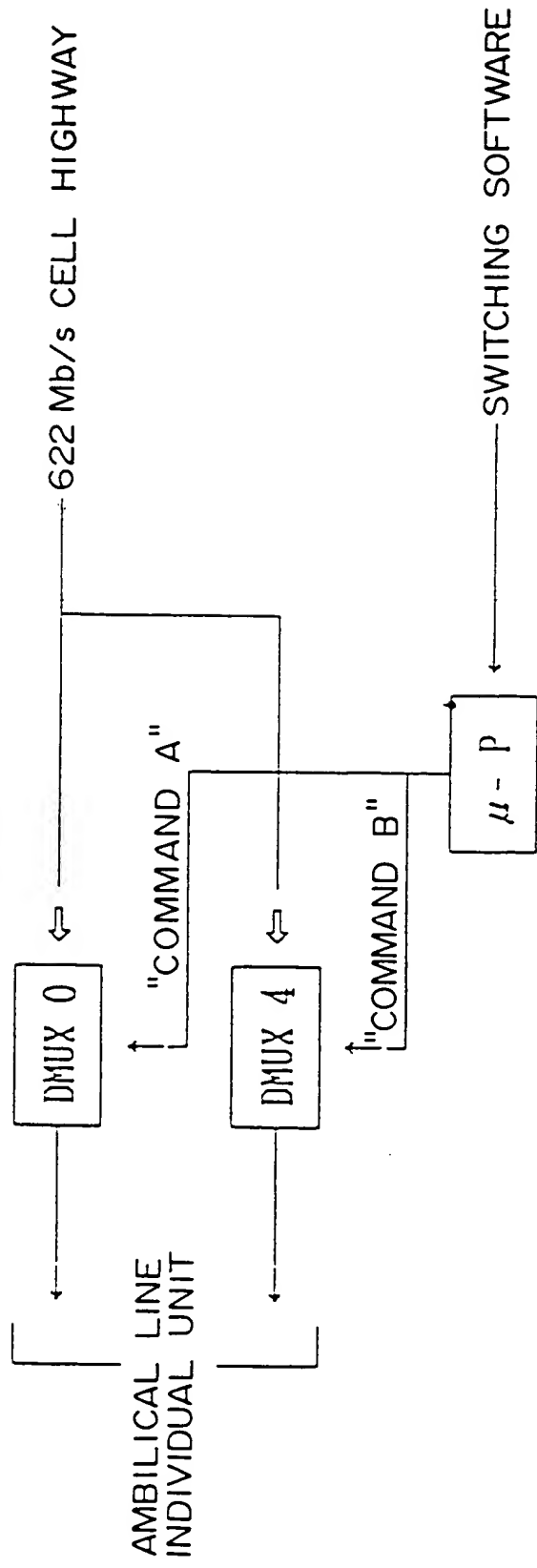


FIG. 144

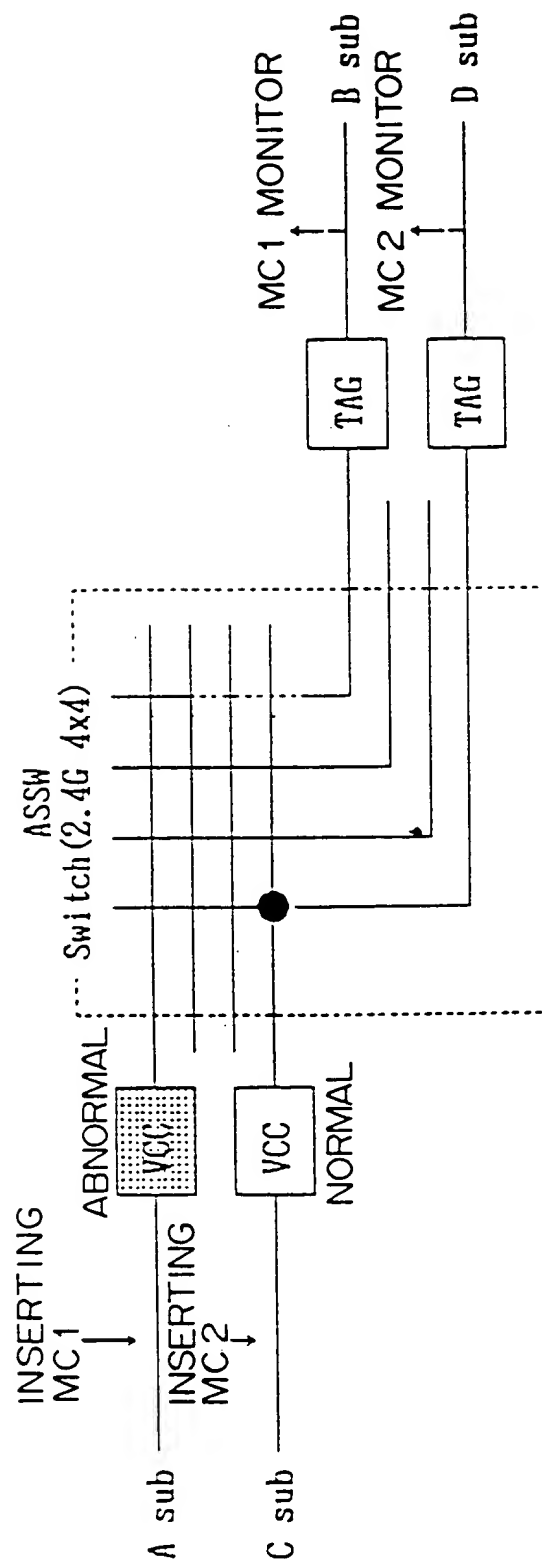


FIG. 146

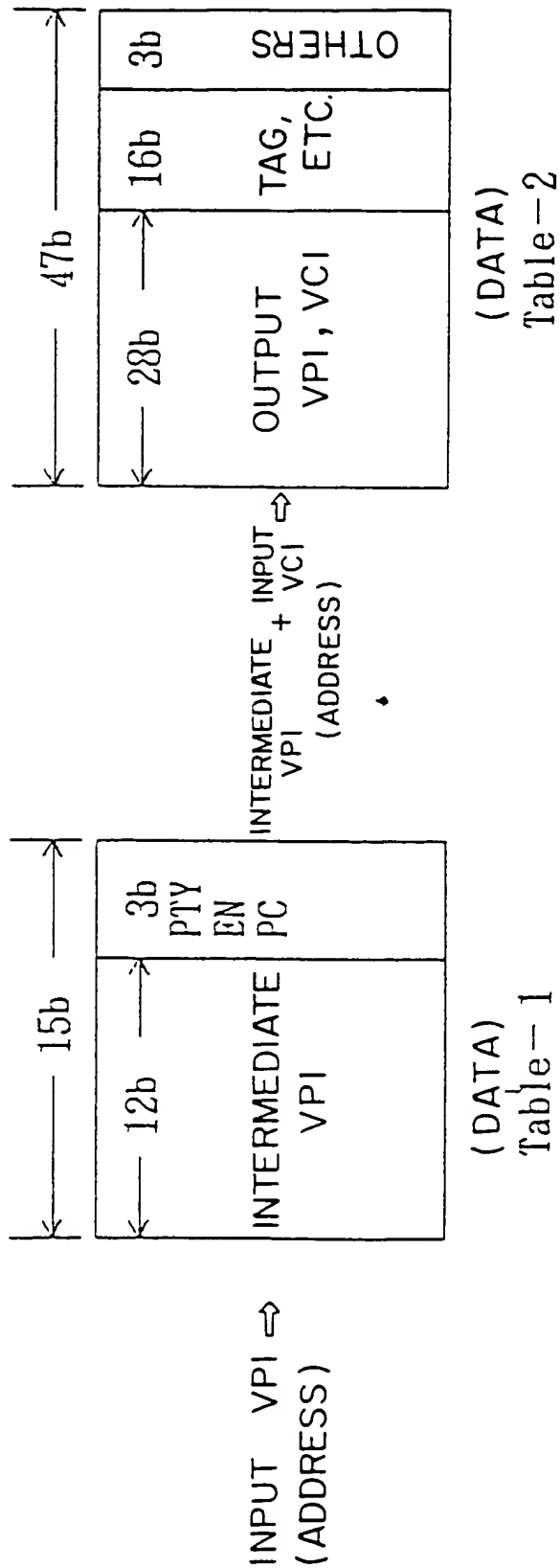


FIG. 147

66360-672260

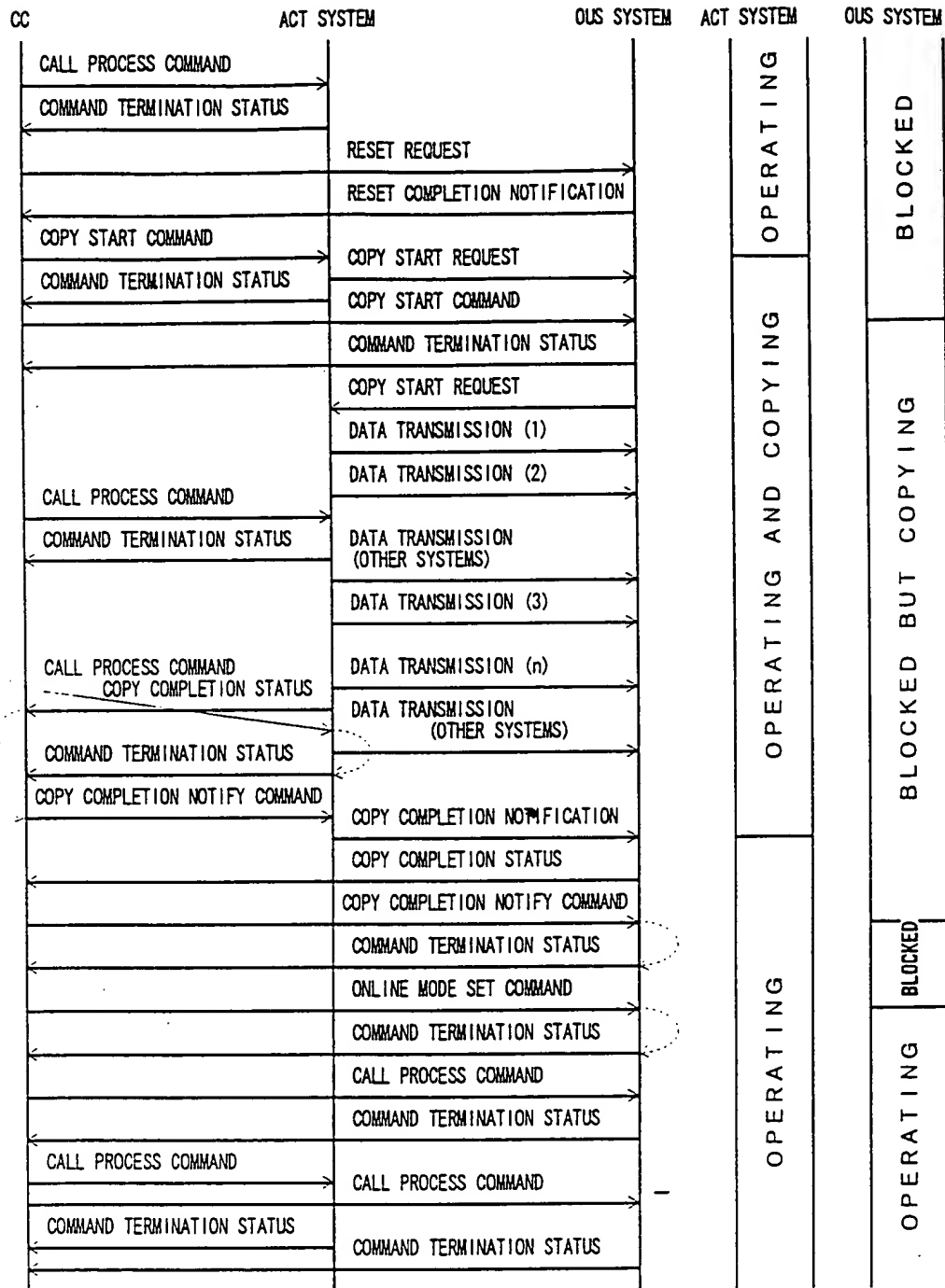


FIG. 148

ACT SYSTEM STATUS	OUS SYSTEM STATUS	IS COPY ALLOWED ?	PROCESS OF CC
COPY COMPLETION REPORT	COPY COMPLETION REPORT	O	COPY COMPLETION NOTIFICATION COMMAND IS ISSUED TO ACT SYSTEM AND OUS SYSTEM.
COPY COMPLETION REPORT	COPY DISABLED OR NOT REPORTED	x	COPY COMPLETION NOTIFICATION COMMAND IS ISSUED TO ACT SYSTEM. OUT SYSTEM IS RESET AND RETRIED. IF RETRY IS ALLOWED, VCC IS INDIVIDUALLY SET IN OUS SYSTEM.
COPY DISABLED OR NOT REPORTED	COPY COMPLETION REPORT	x	
COPY DISABLED OR NOT REPORTED	COPY DISABLED OR NOT REPORTED	x	

FIG. 149

66520-012200

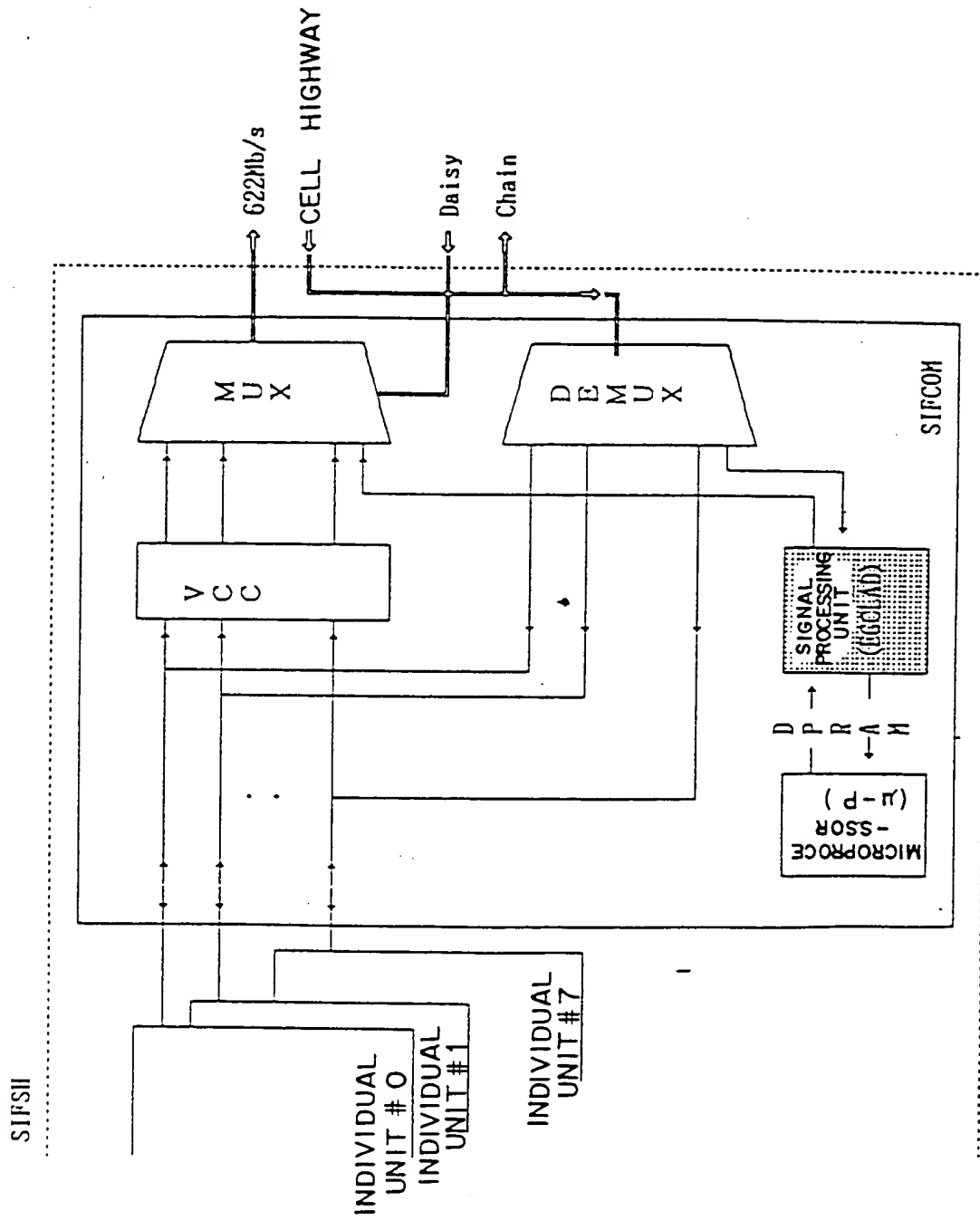
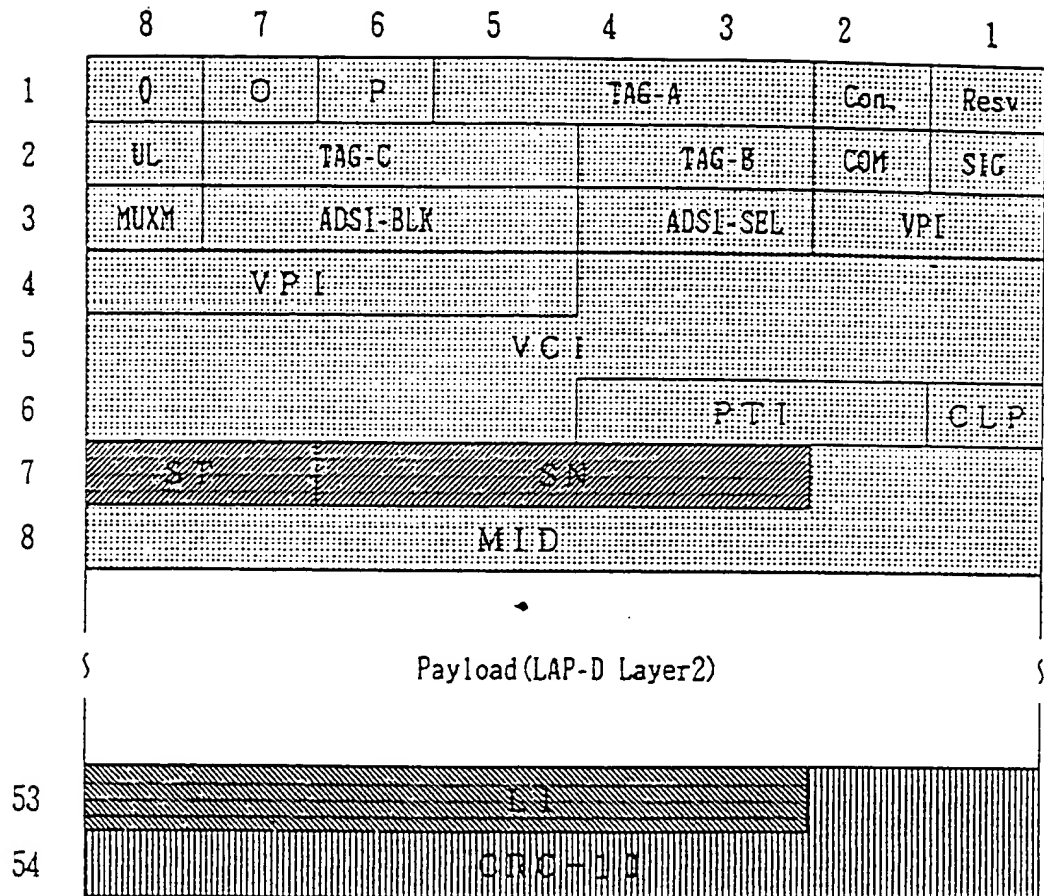


FIG. 150



 : SETTING AT μ
 : SETTING BY SEQUENCE GENERATING UNIT
 : SETTING BY FRAME GENERATING UNIT
 : SETTING BY CRC OPERATING UNIT

FIG. 152

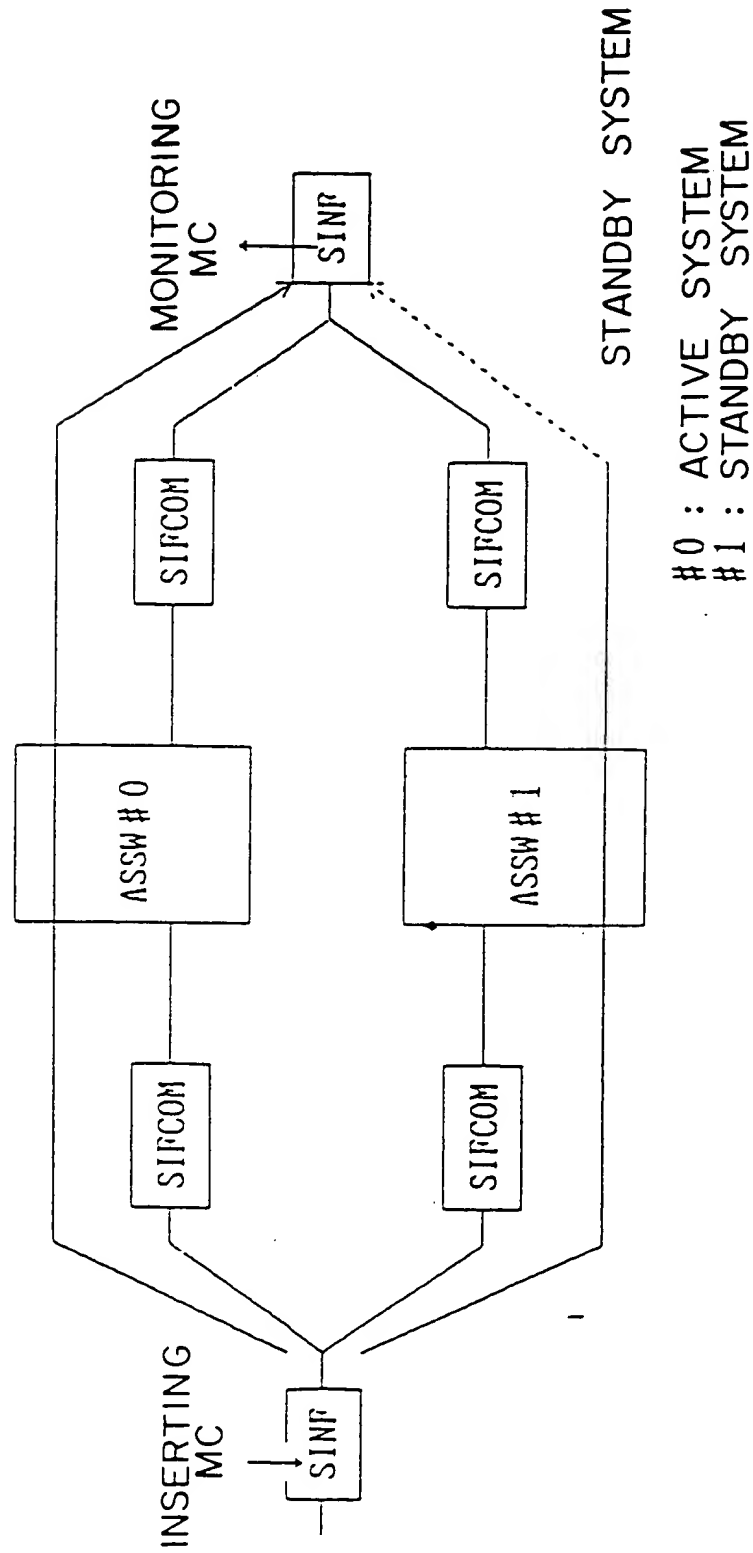


FIG. 153

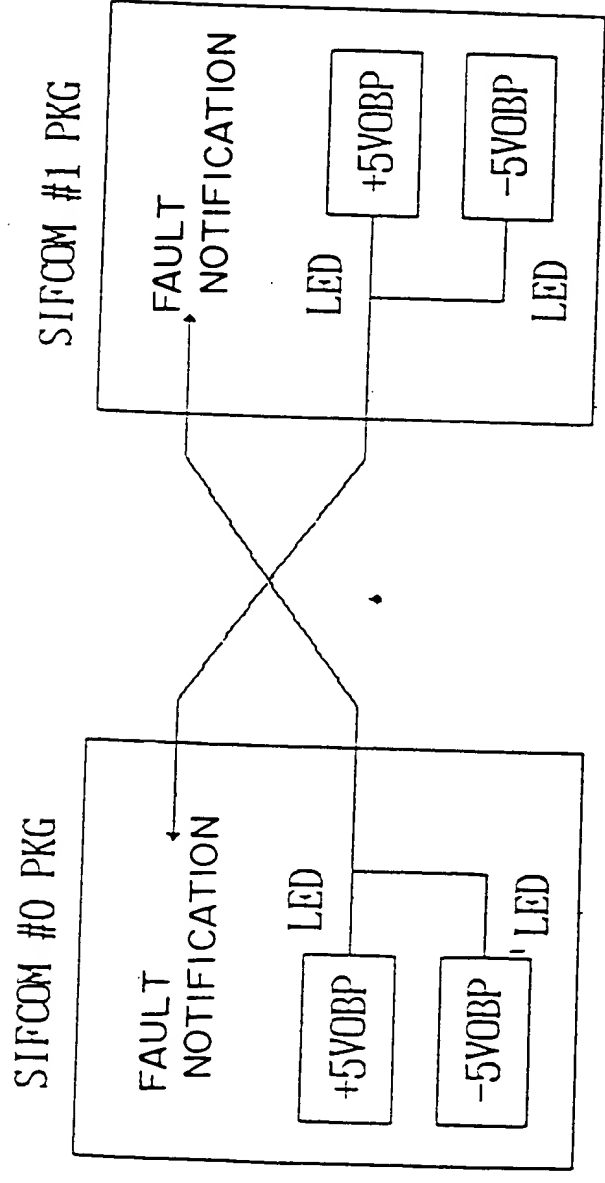


FIG. 155

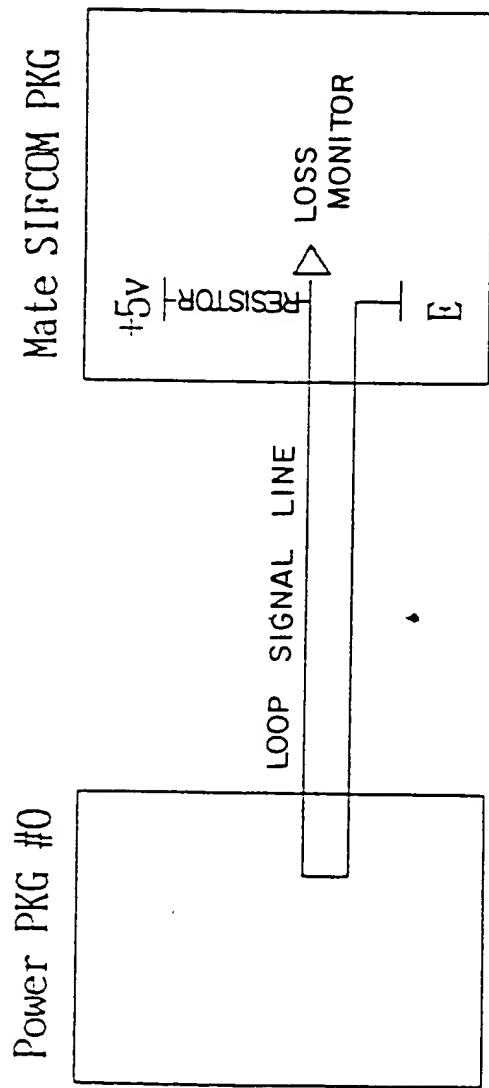


FIG. 157

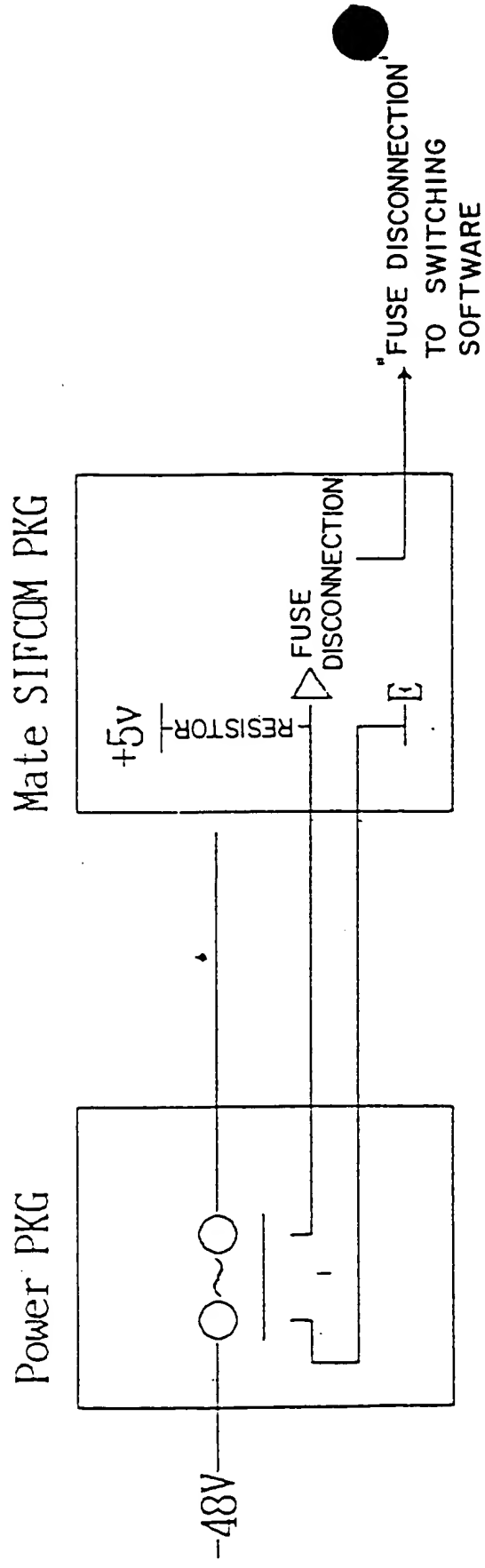


FIG. 158

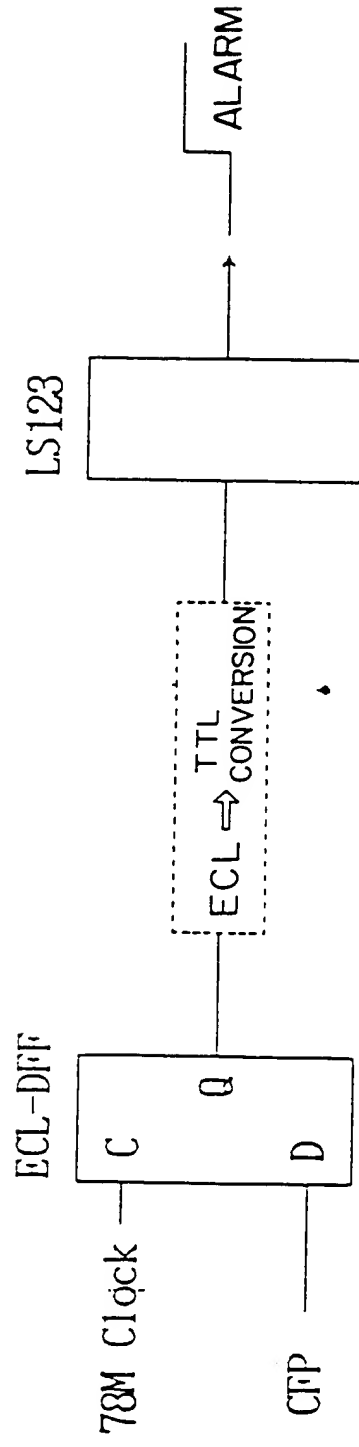


FIG. 159

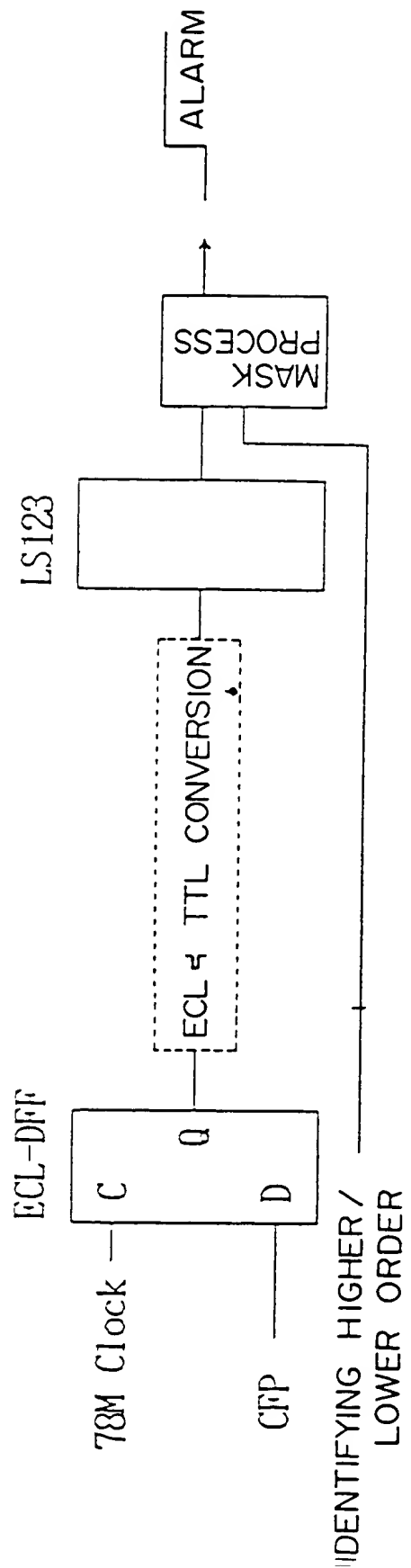


FIG. 160

669207E2260

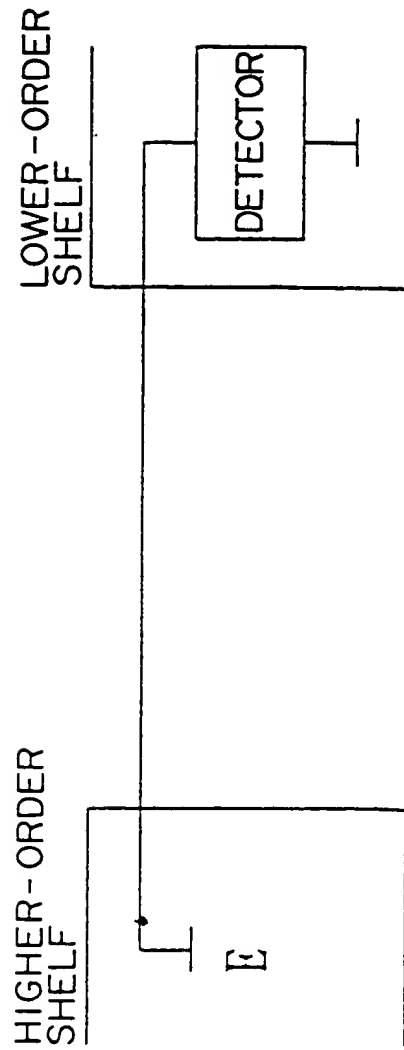


FIG. 161

FAULT POINT	DETECTION LOGIC AND DETECTION POINT	FAULT NOTIFICATION	DETECTION CYCLE
OBP FAULT, CLOCK DISCONNECTION, REF. CLOCK DISCONNECTION, WATCH DOG OVERFLOW	MATE SYSTEM SIFCOM FIRMWARE MONITORS PERIODICALLY.	REPORTED FROM SOFTWARE OF MATE SIFCOM	
PARITY ERROR DURING VCC COPY	ACT SYSTEM SIFCOM FIRMWARE MONITORS CONSTANTLY.	REPORTED FROM SOFTWARE OF ACT SYSTEM SIFCOM.	
INDIVIDUAL INTERFACE UNIT HARDWARE FAULT	HOME SYSTEM SIFCOM FIRMWARE MONITORS PERIODICALLY.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	1sec \times 2
COMMON UNIT HARDWARE FAULT	HOME SYSTEM SIFCOM FIRMWARE MONITORS PERIODICALLY, AND NOTIFY MATE SYSTEM THROUGH SIC.	REPORTED FROM SOFTWARE OF BOTH SYSTEM SIFCOMS	250ms \times 2
-48V DISCONNECTION (POWER PKG MISSING, AMPLIFIER CONNECTOR MISSING)	MATE SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF MATE SIFCOM	250ms \times 2
-48V INDIVIDUAL UNIT FUSE DISCONNECTION	SIFCOMS OF BOTH SYSTEMS PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	250ms \times 2
-48V COMMON UNIT FUSE DISCONNECTION	MATE SYSTEM SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF HOME SYSTEM SIFCOM.	250ms \times 2
SIFCOM PKG MISSING	MATE SYSTEM SIFCOM PERIODICALLY MONITORS.	REPORTED FROM SOFTWARE OF MATE SIFCOM	250ms \times 2

FIG. 163

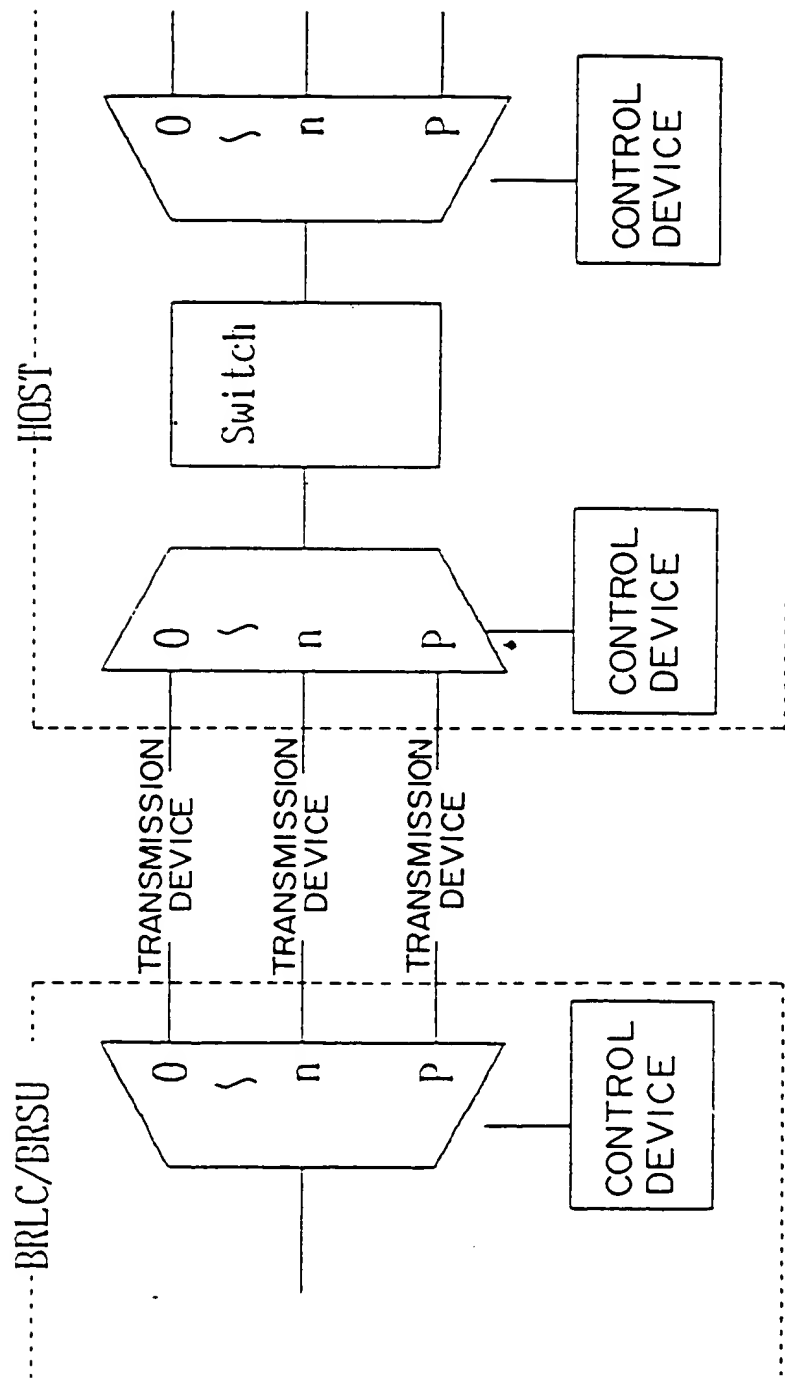
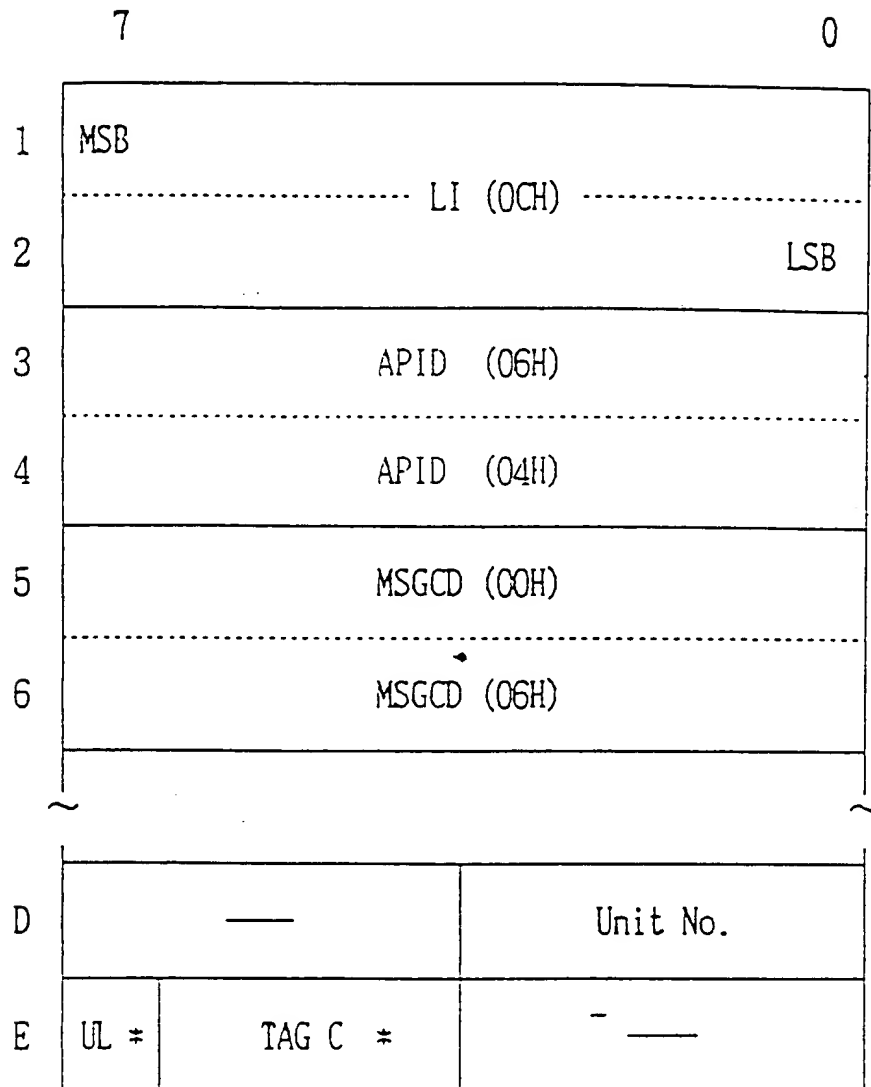


FIG. 164

669920-672260



* : VALUES OF UL AND TAG-C TO BE CHANGED

FIG. 166

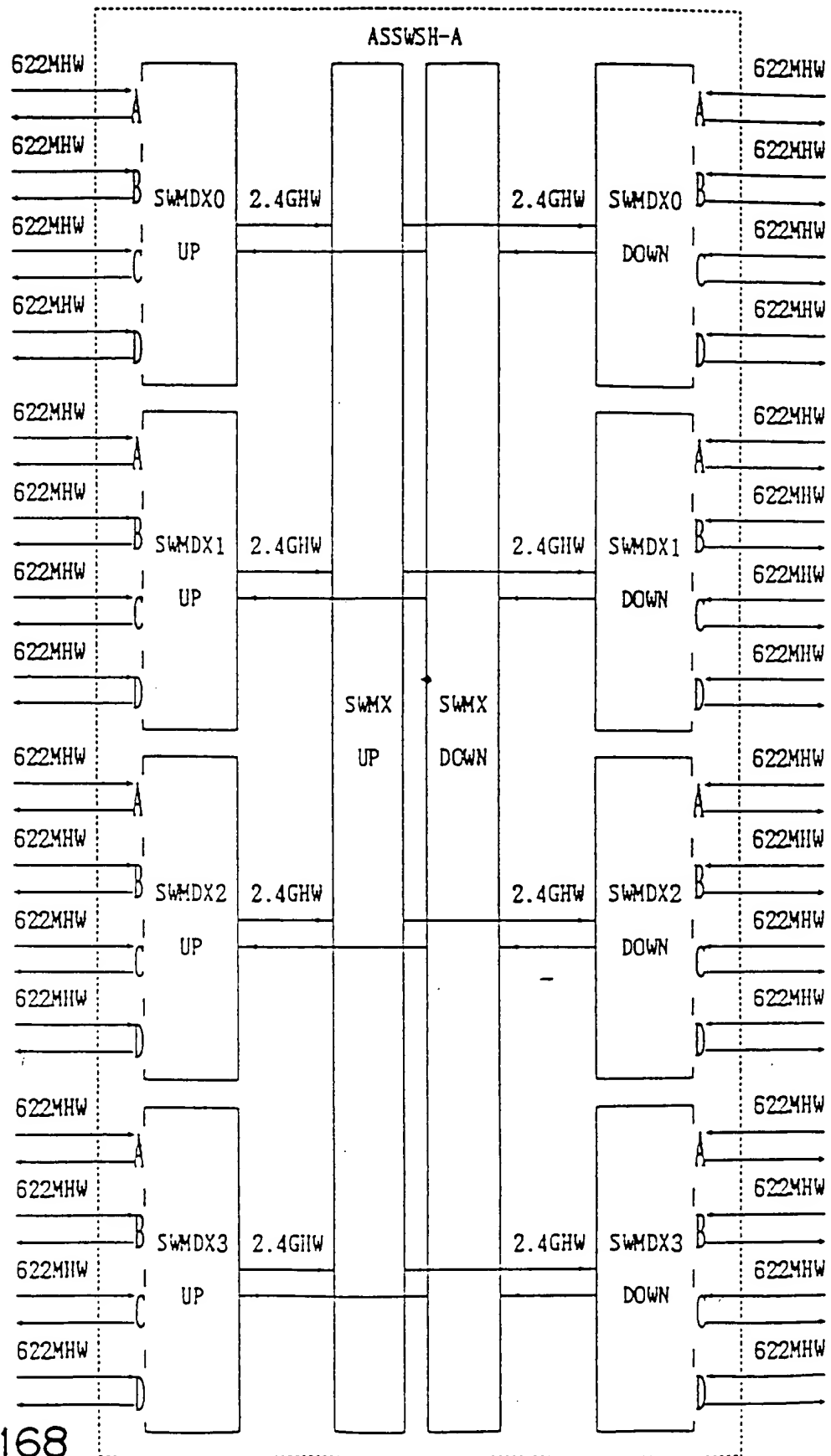


FIG. 168

	HWx7	HWx6	HWx5	HWx4	HWx3	HWx2	HWx1	HWx0
00	O	o	P		TAGA		CON	RES
01	UL		TAGC		TAGB		COM	SIG
02				VPI				
03		VPI				VCI		
04				VCI				
05		VCI				PT		CLP
06								
53								

```

0      : Fixed zero (COPY INDICATION 0 REFERS TO 1:1 COMMUNICATIONS.)
o      : Test bit
P      : Priority bit (CLP of copy) (0:High priority)
TAGA   : 2.4G 4x4 Switch TAG
TAGB   : 2.4GHW ⇒ 622MHW Demultiplex TAG
TAGC   : 622MHW ⇒ 155MHW Demultiplex TAG
CON     : Congestion Control bit (IMPORTANT CALL IDENTIFICATION)
RES     : reserve
COM     : COMMON UNIT IDENTIFICATION IN TERMINAL DEVICE (1:COMMON UNIT)
SIG     : INTRA-STATION LAP CELL (1: LAP CELL)

```

VPI : Virtual Path Identifier
VCI : Virtual Channel Identifier
PT : Payload Type
CLP : Cell Loss Priority bit

FIG. 170

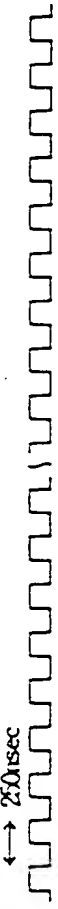



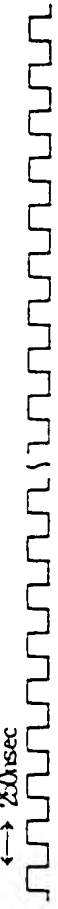




DIRECTION	SIGNAL NAME	BIT NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	REMARKS
PIFA→ASSW	SRC LK	1	V I I BALANCE (1, 1)		
	SWACK	1			BUS USE RIGHT PERMISSION
	RESET	1			PULSE WIDTH: 500 nsec P-ON-R or H-RST
	SYSEL	1			SBY ACT
ASSW→PIFA	SRC LK	1	V I I BALANCE (1, 1)		
	SIRQ	1			BUS USE REQUEST
	ALH	1			NORMAL VALUE ALARM
BI-DIRECTIONAL	SBO ~ 7	8	V I I BALANCE BI-DIRECT- IONAL		
	SPTY	1			

FIG. 171

MATE \Rightarrow SWCNT
SYSTEM

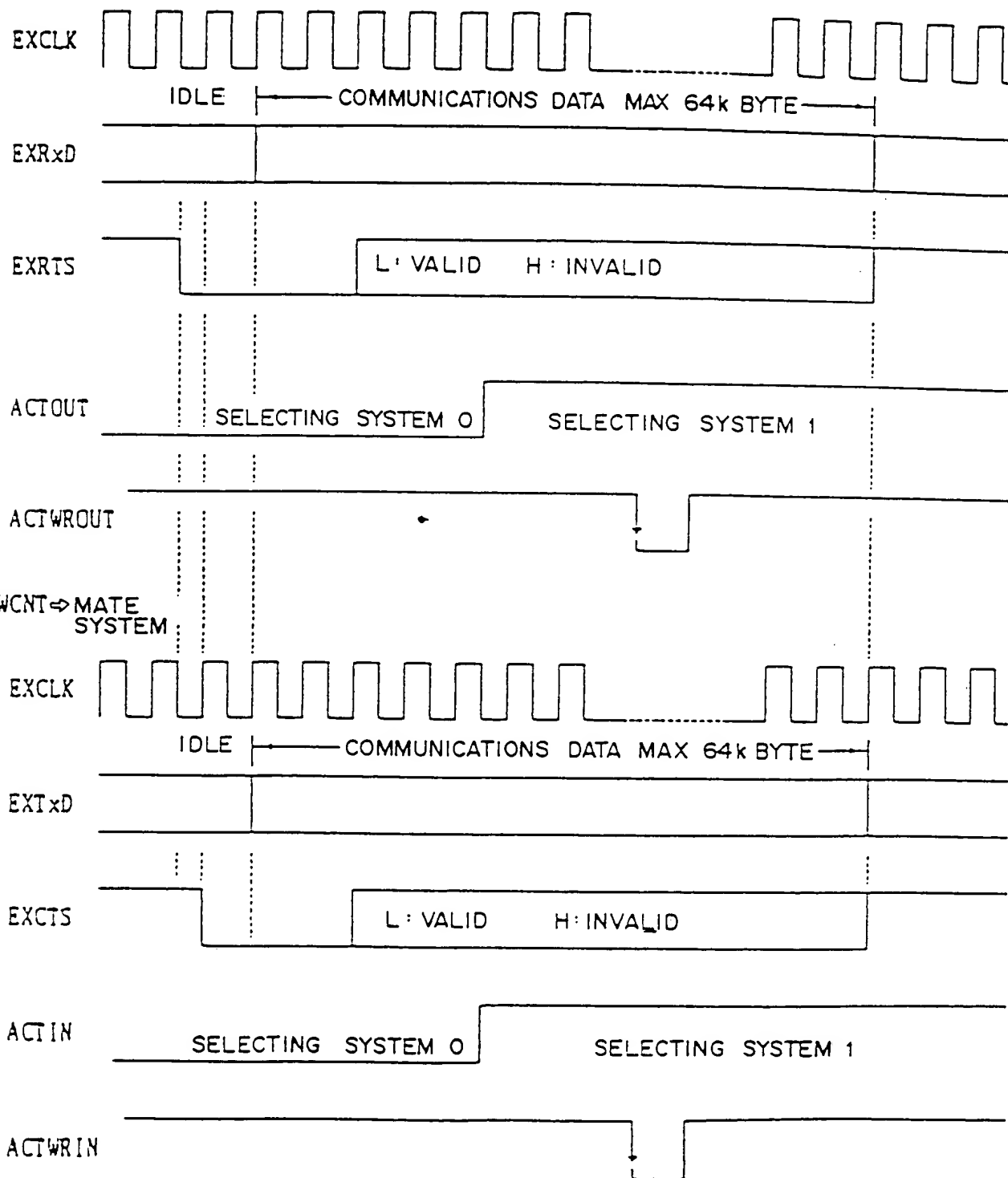


FIG. 172

669220-222222

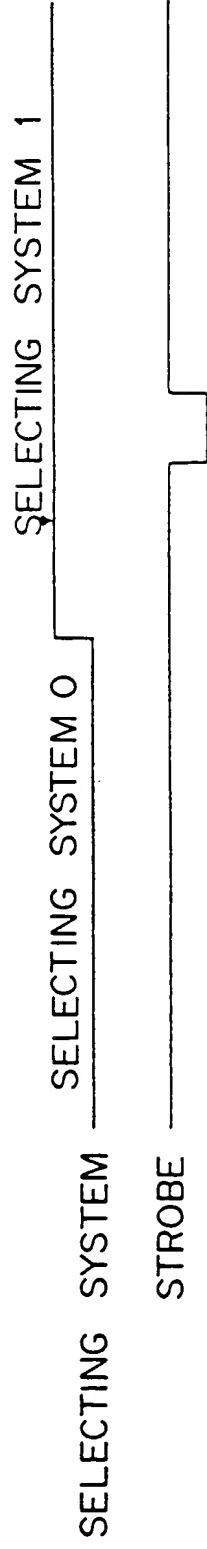


FIG. 173

SYSTEM SELECTION SIGNAL		SELECTION AT TERMINAL DEVICE
HOME SYSTEM SW SELECTION INDICATION	MATE SYSTEM SW SELECTION INDICATION	
SELECTING SYSTEM 0	SELECTING SYSTEM 0	SYSTEM 0
SELECTING SYSTEM 1	SELECTING SYSTEM 1	SYSTEM 1
SELECTING SYSTEM 0	SELECTING SYSTEM 1	RETAINING PREVIOUS STATE
SELECTING SYSTEM 1	SELECTING SYSTEM 0	RETAINING PREVIOUS STATE

FIG. 174

00000000000000000000000000000000

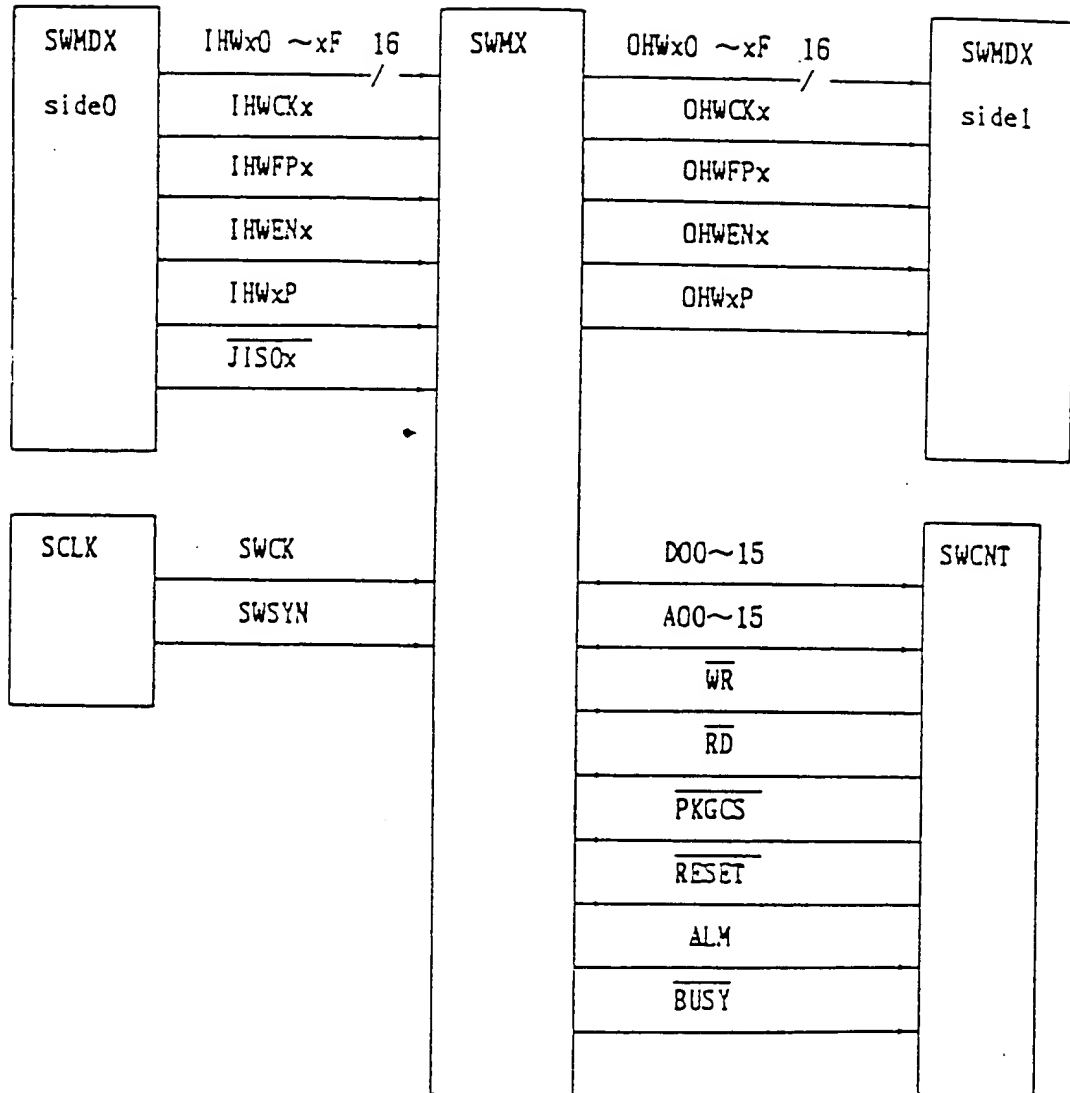


FIG. 175

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
IHWCKx	RECEIVING	ECL	155.52 MHz INPUT CLOCK
IHWxx		ECL	2.4G INPUT HW 16-BIT PARALLEL DATA
IHWFPx		ECL	INPUT CELL FRAME PULSE
IHWENx		ECL	INPUT CELL ENABLE
IHWxP		ECL	ODD PARITY FOR 16-BIT INPUT DATA
JISOx		TTL	2.4G HW IMPLEMENTATION INDICATION
SWCK		ECL	SW BUFFER READING 155.52 MHz CLOCK
SWSYN		ECL	
OHWCKx	SENDING	ECL	155.52 MHz OUTPUT CLOCK
OHWxx		ECL	2.4G OUTPUT HW 16-BIT PARALLEL DATA
OHWFPx		ECL	OUTPUT CELL FRAME PULSE
OHWENx		ECL	OUTPUT CELL ENABLE
OHWxP		ECL	ODD PARITY FOR 16-BIT OUTPUT DATA
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	RECEIVING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	SENDING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	—

FIG. 176

009220 6132250

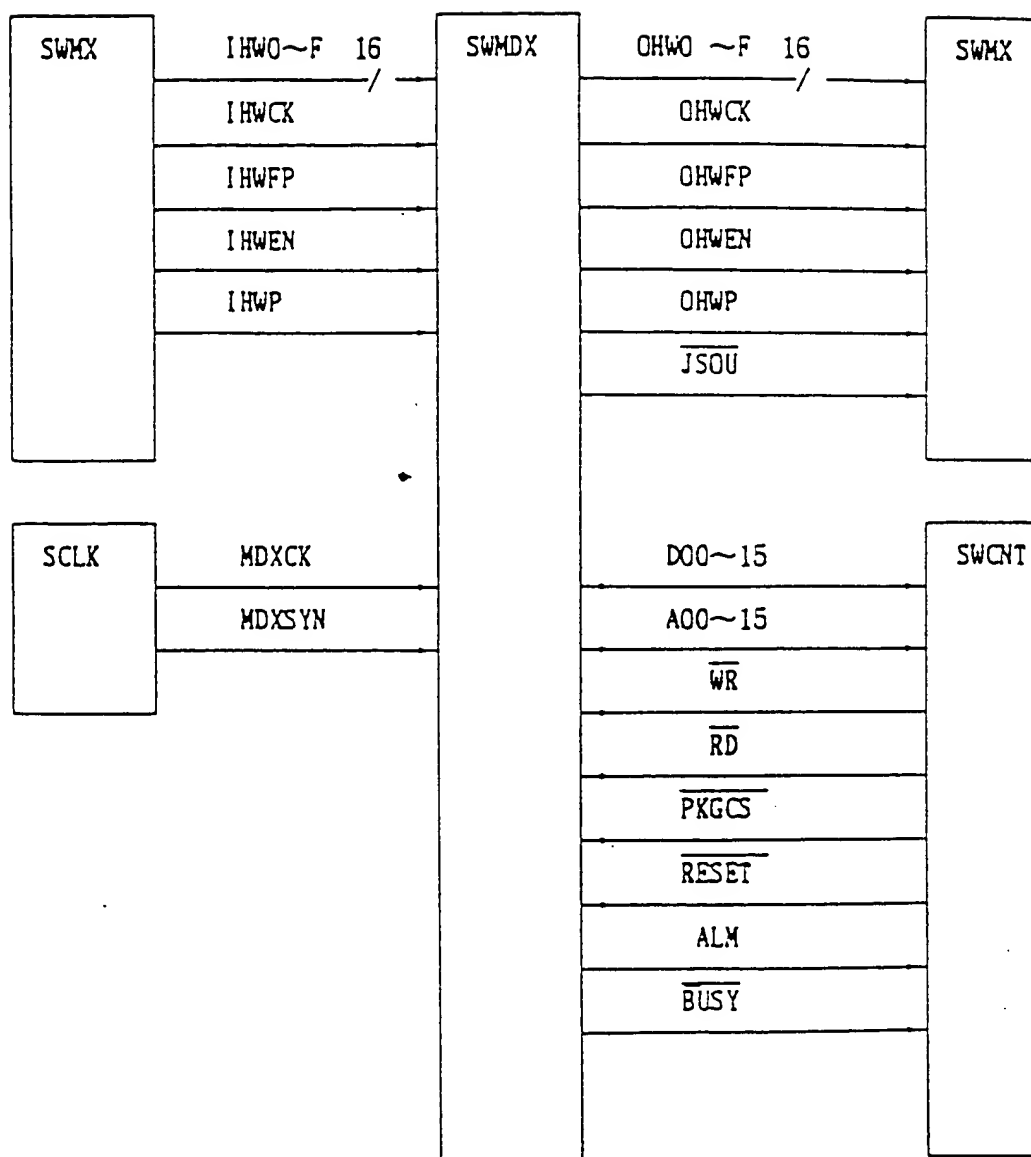


FIG. 177

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
IHWCK	RECEIVING	ECL	155.52 MHz INPUT CLOCK
IHWx		ECL	2.4G INPUT HW 16-BIT PARALLEL DATA
IHWFP		ECL	INPUT CELL FRAME PULSE
IHWEN		ECL	INPUT CELL ENABLE
IHWp		ECL	ODD PARITY FOR 16-BIT INPUT DATA
MDXCK		TTL	MUX BUFFER READING 155.52 MHz CLOCK
MDXSYN		ECL	
OHWCK	SENDING	ECL	155.52 MHz OUTPUT CLOCK
OHWx		ECL	2.4G OUTPUT HW 16-BIT PARALLEL DATA
OHWFP		ECL	OUTPUT CELL FRAME PULSE
OHWEN		ECL	OUTPUT CELL ENABLE
OHWP		ECL	ODD PARITY FOR 16-BIT OUTPUT DATA
JSOU		ECL ^o	2Z4G HW IMPLEMENTATION INDICATION
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	RECEIVING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	SENDING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	-

FIG. 178

665000 665000 665000

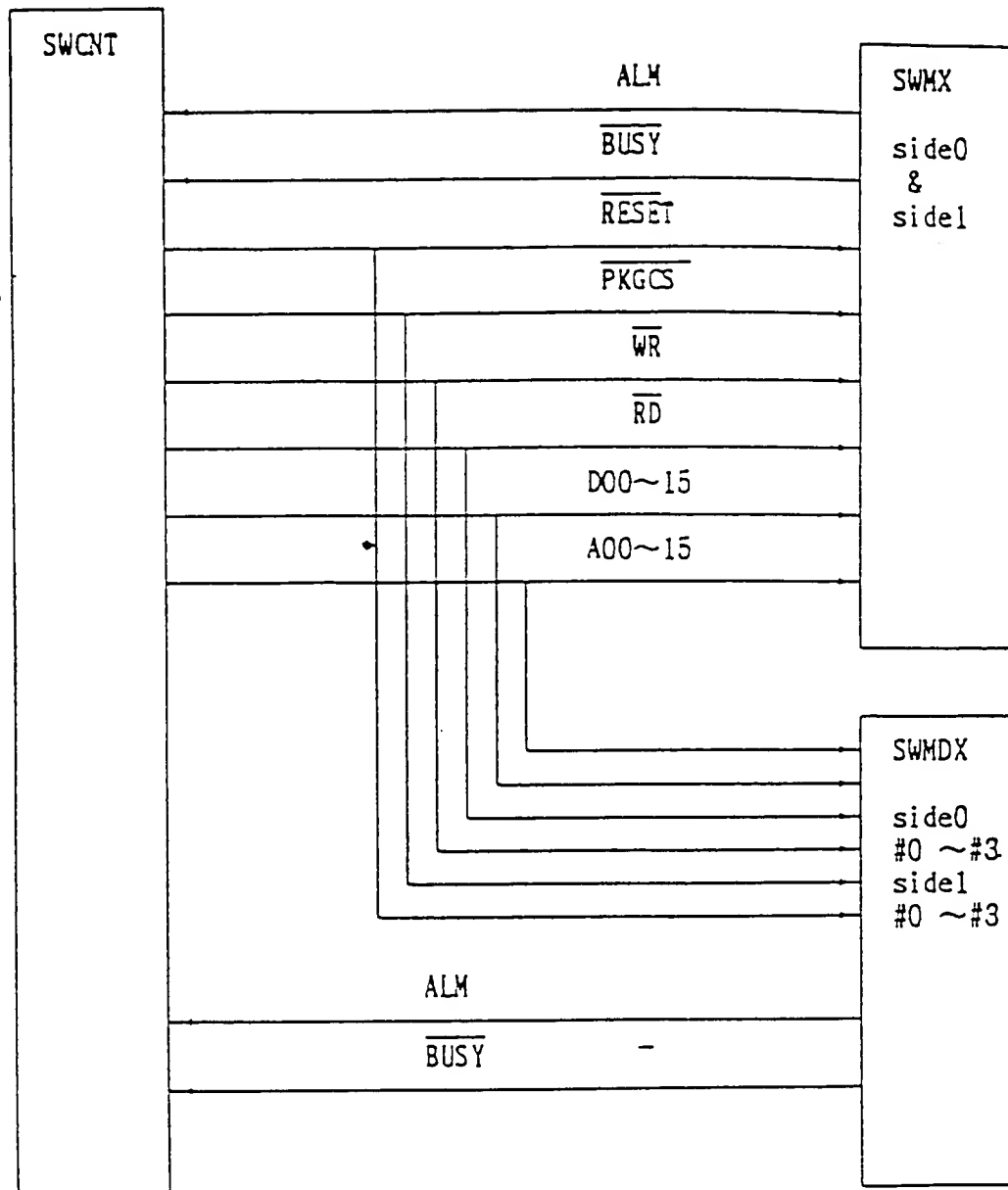


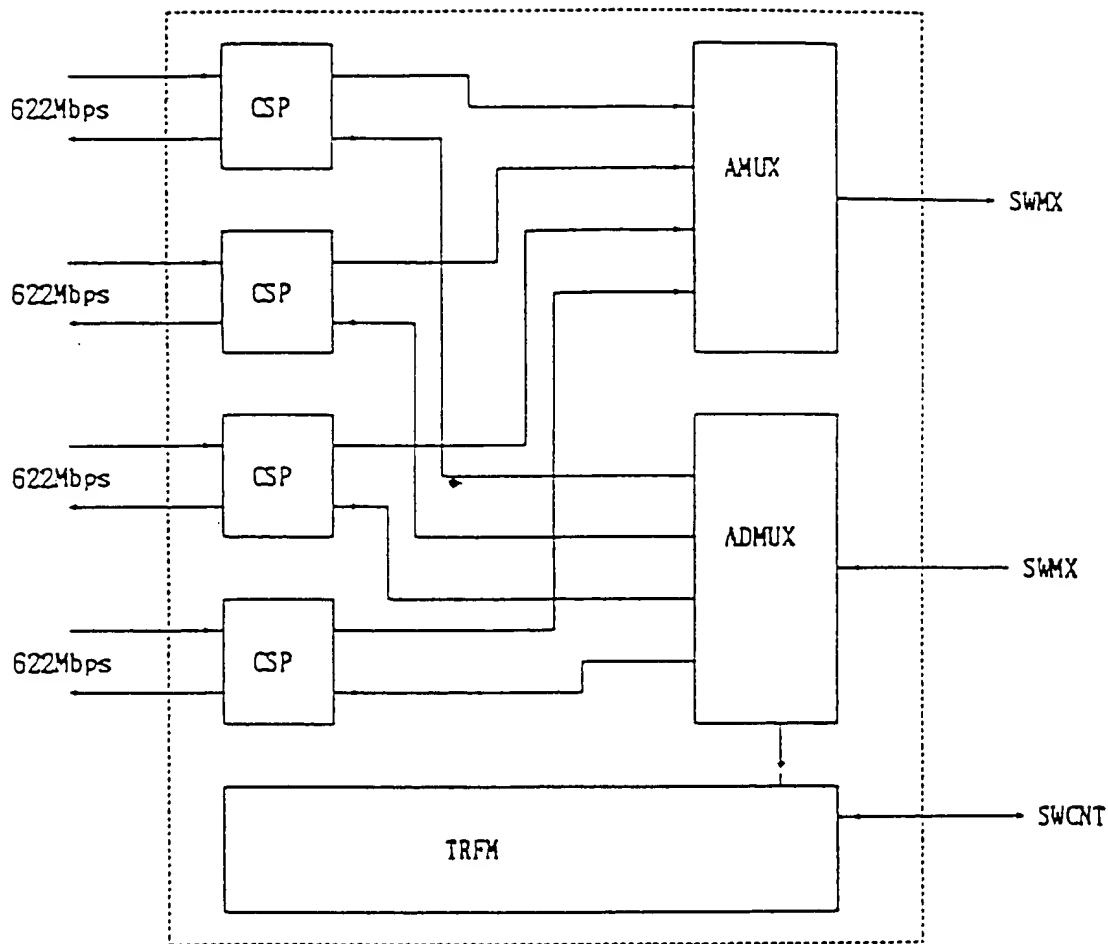
FIG. 179

SIGNAL NAME	SENDING/RECEIVING	LEVEL	MEANING OF SIGNAL
Dxx	BIDIRECTIONAL	TTL	PROCESSOR DATA BUS
Axx		TTL	PROCESSOR ADDRESS BUS
WR		TTL	WRITE REQUEST SIGNAL
RD		TTL	READ REQUEST SIGNAL
PKGCS	SENDING	TTL	PACKAGE SELECTION
RESET		TTL	POWER-ON, OR OF M-RST
ALM	RECEIVING	TTL	NG-OR OF FAULT MONITOR POINT IN EACH PACKAGE
BUSY		TTL	

FIG. 180

BLOCK NAME	FUNCTION
SWMDX	CELLS ARE MULTIPLEXED FROM 620 MBPS FULL ATM HIGHWAY TO 2.4 GBPS HIGHWAY IN SWITCH CELLS ARE DEMULTIPLEXED FROM 2.4 GBPS HIGHWAY IN SWITCH 620 MB S FULL ATM HIGHWAY TRAFFIC MEASUREMENT FUNCTION AND CONGESTION CONTROL FUNCTION
SWMX	4 × 4 SELF-ROUTING IN 2.4 GBPS HIGHWAY CONGESTION CONTROL FUNCTION
SWCNT	INTERFACE WITH DUPLEX CC FAULT MONITOR IN DEVICE
SWTIF	DISTRIBUTING ACT SIGNAL OF DUPLEX SYSTEM TO EACH TERMINAL DEVICE COMMON UNIT
SCLK	SELECTING SYSTEM OF CLK#0/1 GENERATING 155.52 MHZ FROM SELECTED 10.368 MSZ AND DISTRIBUTING IT TO EACH UNIT
POW	NECESSARY POWER SOURCE IS SUPPLIED IN DEVICE

FIG. 181



CSP : Cell Serial/Parallel Converter
 AMUX : ATM cell Multiplexer
 ADMUX : ATM cell Demultiplexer
 TRFM : Traffic Monitor

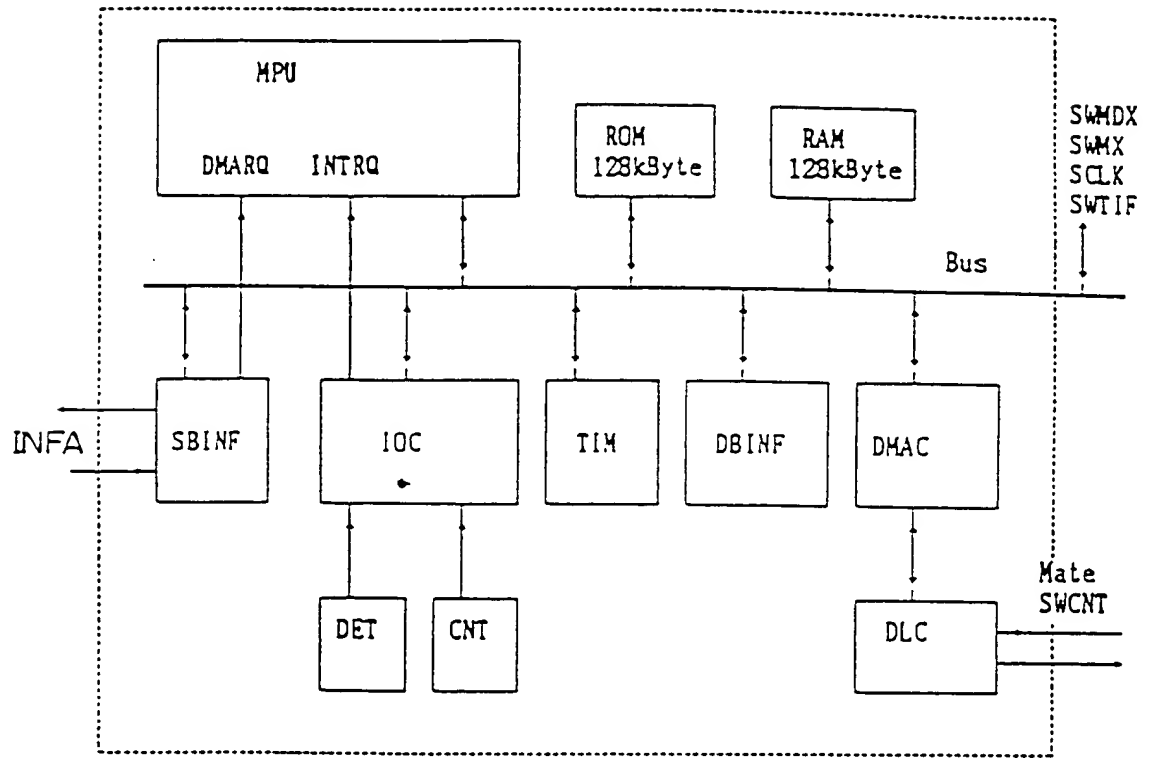
FIG. 182

BLOCK NAME	FUNCTION
CSP	<ul style="list-style-type: none"> • CONVERSION FROM 622 MBPS HIGHWAY 16 PARALLEL (TTL) TO 8 PARALLEL (ECL) • CONVERSION FROM 622 MBPS HIGHWAY 8 PARALLEL (ECL) TO 16 PARALLEL (TTL) • CHECKING PARITY IN INPUT HIGHWAY • GENERATING PARITY IN OUTPUT HIGHWAY
AMUX	<ul style="list-style-type: none"> • FOUR 622 MBPS HIGHWAYS ARE CELL-MULTIPLIED INTO 2.4 GBPS HIGHWAYS • CHECKING PARITY IN INPUT HIGHWAY • GENERATING PARITY IN OUTPUT HIGHWAY • GENERATING AND CHECKING PARITY OF INTERNAL BUFFER
ADMUX	<ul style="list-style-type: none"> • 2.4 GBPS HIGHWAY IS DEMULTIPLIED INTO FOUR 622 MBPS HIGHWAYS ACCORDING TO TAG INFORMATION IN CELL • CHECKING PARITY IN INPUT HIGHWAY (CELL IS DISCARDED, IF HEADER PARITY ERROR OCCURS) • GENERATING PARITY IN OUTPUT HIGHWAY • GENERATING AND CHECKING PARITY OF INTERNAL BUFFER • OUTPUTTING CELL DISCARD NOTIFICATION, VALID CELL PASSING NOTIFICATION, AND TRAFFIC MEASUREMENT HEADER INFORMATION • SERVICE CLASS IS CONTROLLED BY P BIT WHEN DMUX BUFFER USE EXCEEDS THRESHOLD. (REFER TO TRAFFIC CONTROL FOR DETAILS)
TRFM	<ul style="list-style-type: none"> • SETTING AND READING PARAMETER FROM PROCESSOR (COUNTING NUMBER OF CELLS ARRIVING AND DISCARDED AT EACH OUTPUT LINE ACCORDING TO TRAFFIC INFORMATION FROM ADMUX)

FIG. 183

BLOCK NAME	FUNCTION
SWCNT	<ul style="list-style-type: none">• CELL READ FROM ATMSW IS CONTROLLED.• ATMSW USE OF BUFFER IS MONITORED.• SERVICE CLASS IS CONTROLLED BY P BIT WHEN BUFFER USE EXCEEDS THRESHOLD.
ATMSW	2 × 2 SELF-ROUTING SWITCH OF 2.4 GBPS HIGHWAY
REG	RETIMING INPUT HIGHWAY FROM SWMDX AND DISTRIBUTING IT TO ATMSW
PRINF	SETTING AND READING PARAMETER FROM PROCESOR

FIG. 185

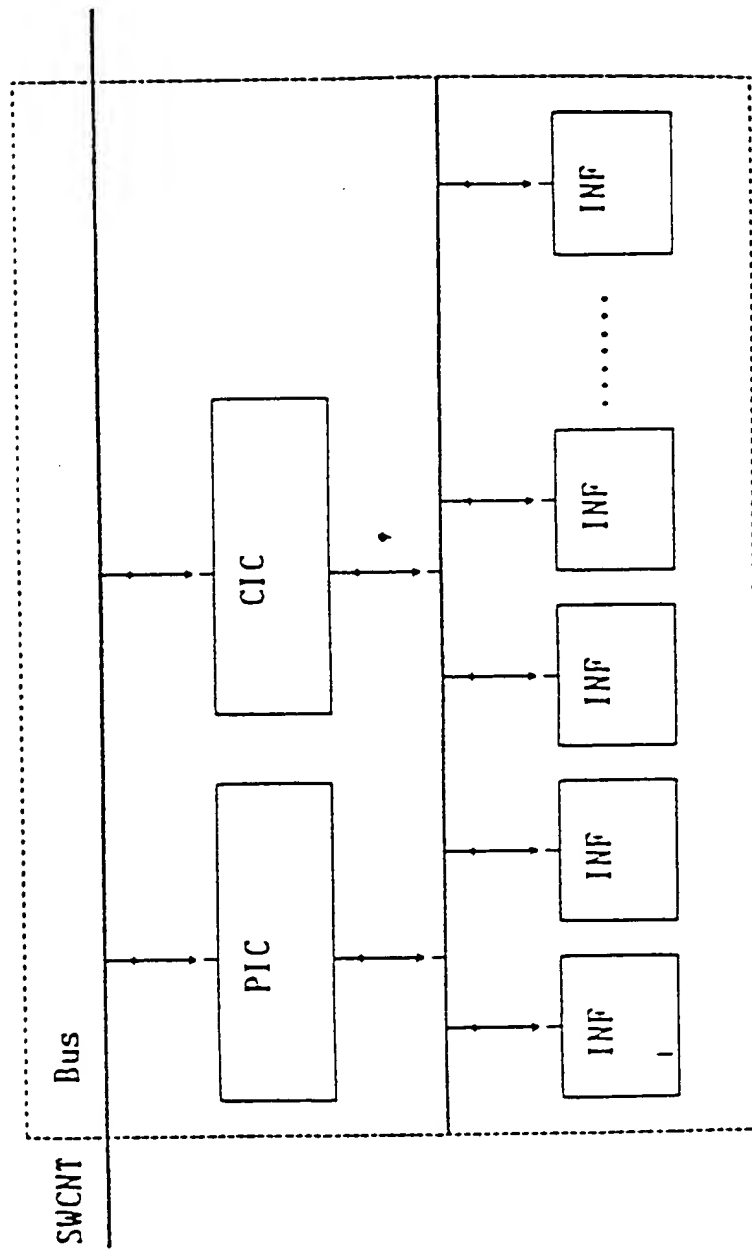


MPU : Micro-processor
 IOC : I/O Controller
 TIM : TIMER
 ROM : Read Only Memory
 RAM : Random Access Memory
 SBINF : Switch Bus Interfacer
 DLC : Data Link Controller
 DMAC : DMA controller
 DBINF : Debug Interfacer
 DET : Fault Detector
 CNT : Interrupt Controller

FIG. 186

BLOCK NAME	FUNCTION
MPU	SW UNIT CONTROL PROCESSOR
IOC	RECEIVING INTERRUPT REQUEST FROM I/O DEVICE AND CONTROLLING INTERRUPTION PROCESS
TIM	GENERATING FIRMWARE MONITOR TIMER AND DBINF COMMUNICATIONS CLOCK
ROM	STORING SW UNIT CONTROL PROGRAM
RAM	USED AS CONTROL PROCESSOR WORK AREA
SBINF	INTERFACING BETWEEN PIFA-SW BUS AND CONTROL PROCESSOR BUS. PERFORMING CC ACCESS PROCESS, DMA ACCESS PROCESS, AND MSCN PROCESS.
DLC	SERIAL COMMUNICATIONS CONTROLLER TO ESTABLISH COMMUNICATIONS WITH MATE SYSTEM
DMAC	DMA CONTROLLER FOR CONTROLLING DLC 4 CHANNEL
DBINF	DEBUGGING RS232C INTERFACE
DET	CONNECTING FAULT INFORMATION
CNT	CONTROLS VARIOUS INTERRUPTION INFORMATION

FIG. 187



PIC : Processor Interface Controller
 CIC : Communication Interface Controller
 INF : Lower Unit Interfacer

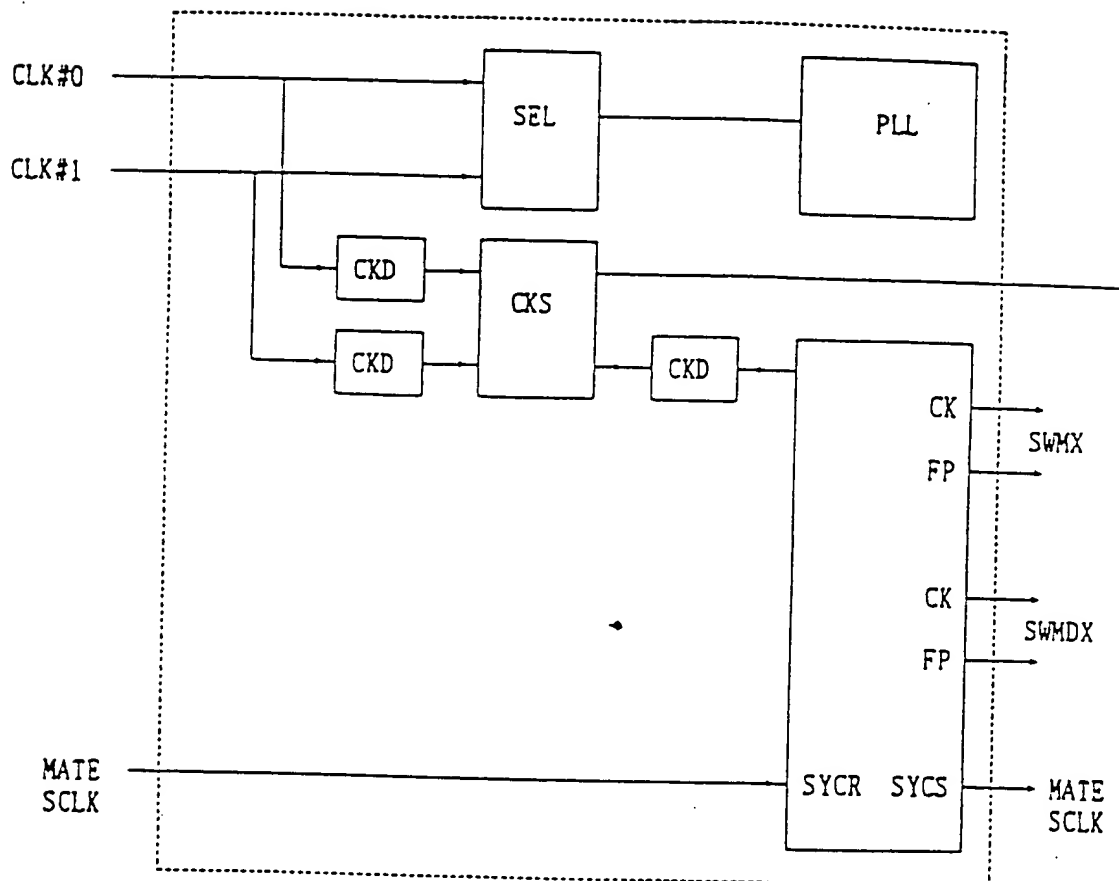
FIG. 188

BLOCK NAME	F U N C T I O N
P I C	CONTROLLING INTERFACE WITH SW UNIT CONTROL PROCESSOR (I80C186) SELECTING LINE, REPORTING INTERRUPTION OCCURRENCE, ETC.
C I C	CONTROLLING INTERFACE WITH SWCNT DLG
I N F	DETECTING COMMUNICATIONS CONTROL SIGNAL TO SW EXTENSION (NOT EXISTING) MONITORING PROCESSOR FAULT IN SW EXTENSION (NOT EXISTING)

F I G. 189

0927213 032699

00000-672250



CKD : Clock Down Detector
 CKS : Clock Select Controller
 SEL : Clock Selectore
 PLL : Phase Lock Loop
 TIM : Timing Generator

FIG. 190

BLOCK NAME	FUNCTION
CKD	DETECTING DISCONNECTION OF SYSTEM CLOCK FROM CLOCKS 0 AND 1 SYSTEMS DETECTING DISCONNECTION FROM OUTPUT CLOCK FROM PLL
CKS	SELECTING SYSTEM OF SYSTEM CLOCK (AUTONOMOUS SWITCH ACCORDING TO INFORMATION FROM CLKD) NOTIFYING SWCNT OF CLOCK FAULT AND SYSTEM SELECTION STATE
SEL	SELECTING AND OUTPUTTING CLOCK TO BE USED IN SRSW ACCORDING TO CONTROL SIGNAL OF CKS
PLL	GENERATING 155.5 MHZ FROM REFERENCE CLOCK 10.368 MHZ
TIM	GENERATING CLOCK/READ FRAME PULSE TO BE SUPPLIED TO SWMX AND SWMDX SYNCHRONIZING READ FRAME PULSE ACCORDING TO SYNCHRONIZATION SIGNAL FROM MATE SYSTEM AT INITIALIZATION

FIG. 191

SERVICE (CELL DISCARD CLASS)	CLP	P
Assured service (High priority)	0	0
Assured service (Low priority)	1	0
Non-assured service	1	1

FIG. 192

L: DISCARD NOTIFICATION SIGNAL
V: VALID CELL NOTIFICATION SIGNAL
H: CELL HEADER INFORMATION

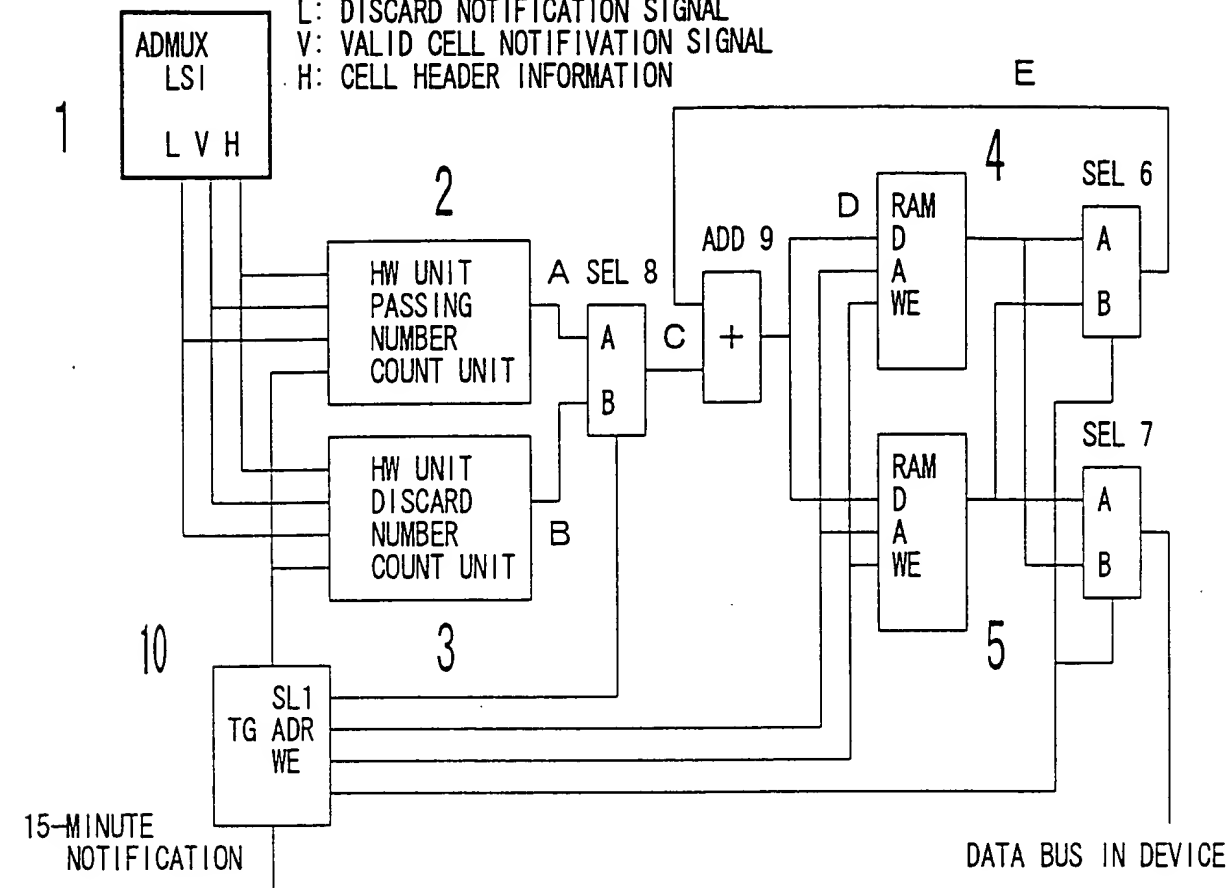
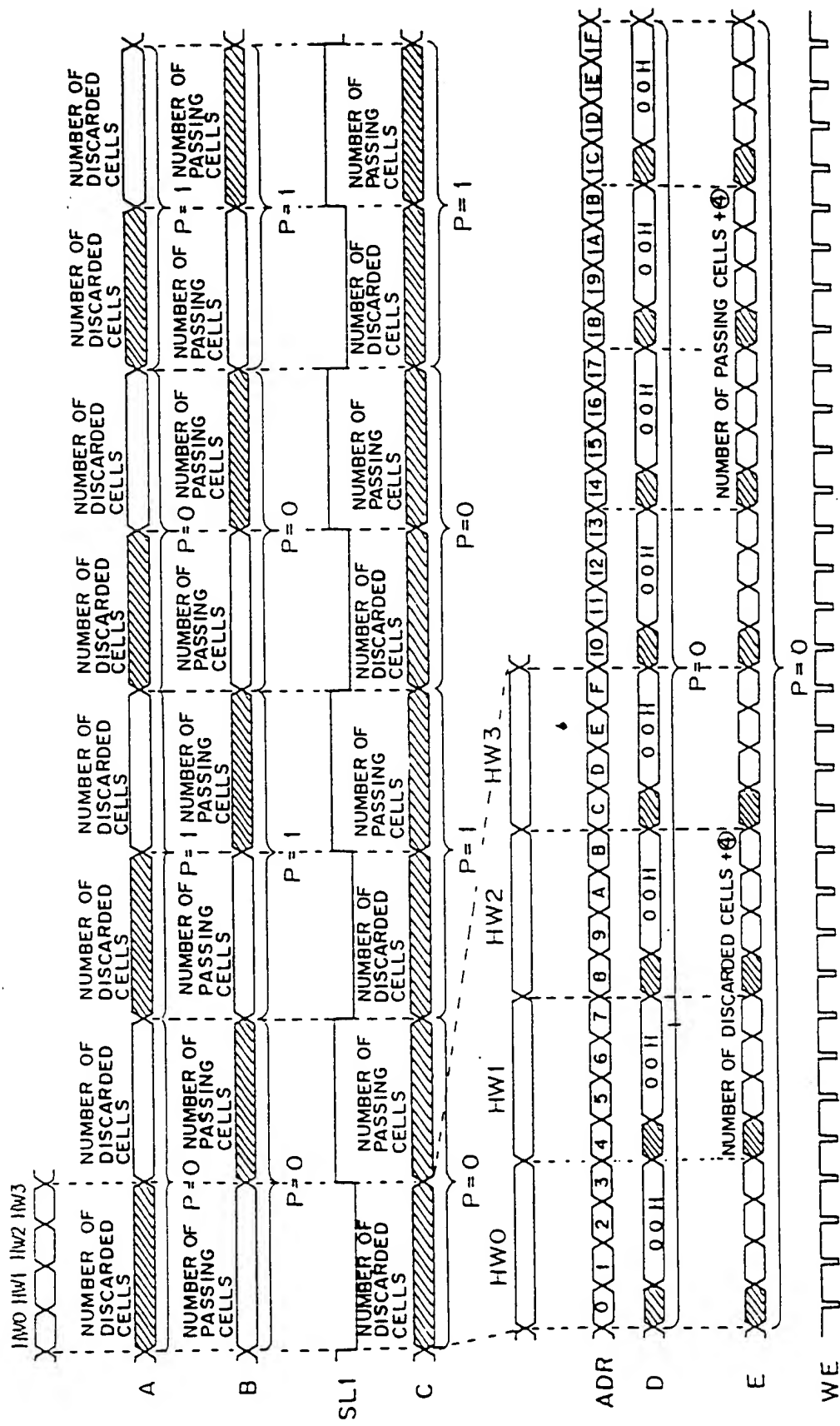
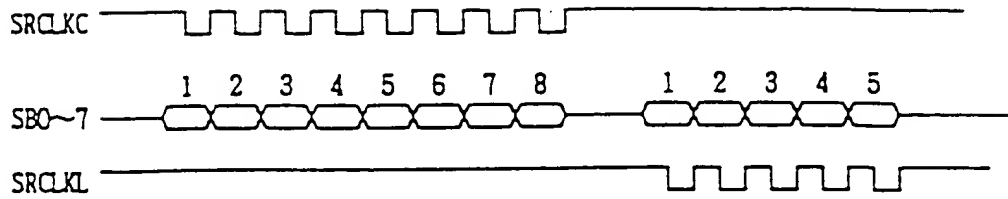


FIG. 193

[illegible]

(a)



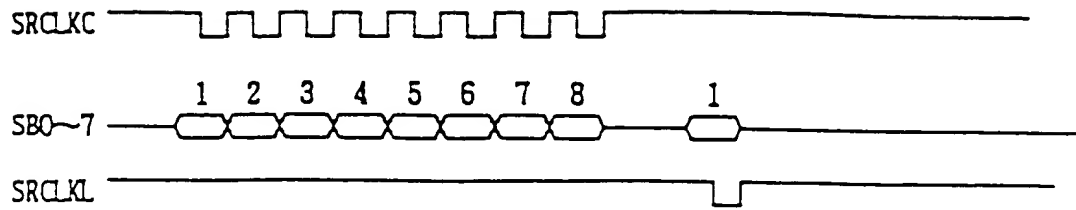
(b)

	1	2	3	4	5	6	7	8		1	2	3	4	5
SBO	(1)									(1)				
1											D	a	D	a
2	D.	23	15	07	D.	D.	D.	D.		D.	a	a	a	a
3	C.	16	08	00	C.	C.	C.	C.		C.	24	16	08	00
4											\	\	\	\
5											31	23	15	07
6														
SB7	(2)									(2)				
PTY	P	P	P	P	P	P	P	P		P	P	P	P	P
	ADDRESS									DATA				

(1) READ/WRITE READ:1 WRITE:0
 (2) ORDER/ANSWER ORDER:1 ANSWER:0

FIG. 195

(d)



(b)

	1	2	3	4	5	6	7	8	1
SBO	(1)								(1)
1									
2	D.	23	15	07	D.	D.	D.	D.	D.
3		16 ~	08 ~	00 ~					
4	C.	ADDRESS	ADDRESS	ADDRESS	C.	C.	C.	C.	C.
5									
6									
SB7	(2)								(2)
PTY	P	P	P	P	P	P	P	P	P
	ADDRESS								DATA

(1) READ/WRITE READ:1 WRITE:0
 (2) ORDER/ANSWER ORDER:1 ANSWER:0

FIG. 196

(a)

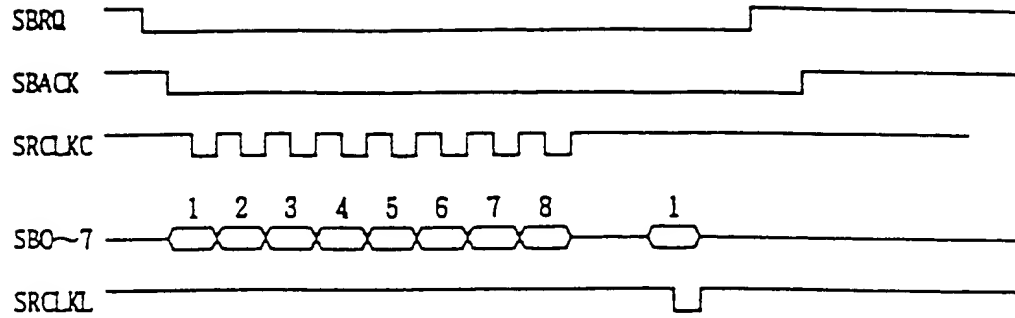
(b)

	1	2	3	4	5	6	7	8		1	2	3	4	5
SB0	(1)	Address	Address	Address						(1)	Data	Data	Data	Data
1		Address	Address	Address						(3)				
2	C.	Address	Address	Address	C.	C.	C.	C.		(4)				
3	D.	Address	Address	Address										
4		16	08	00	D.	D.	D.	D.			C.	24	16	08
5		S	S	S							D.	S	S	S
6		23	15	07								31	23	15
SB7	(2)									(2)				
PTY	P	P		P	P	P	P	P		P	P	P	P	P
	ADDRESS									DATA				

(1) READ/WRITE READ : 1 WRITE : 0
 (2) ORDER/ANSWER ORDER : 1 ANSWER : 0
 (3) ERROR1 ERROR EXISTING : 1 ERROR NOT EXSITING : 0
 (4) ERROR2 ERROR EXISTING : 1 ERROR NOT EXSITING : 0

FIG. 197

(a)



(b)

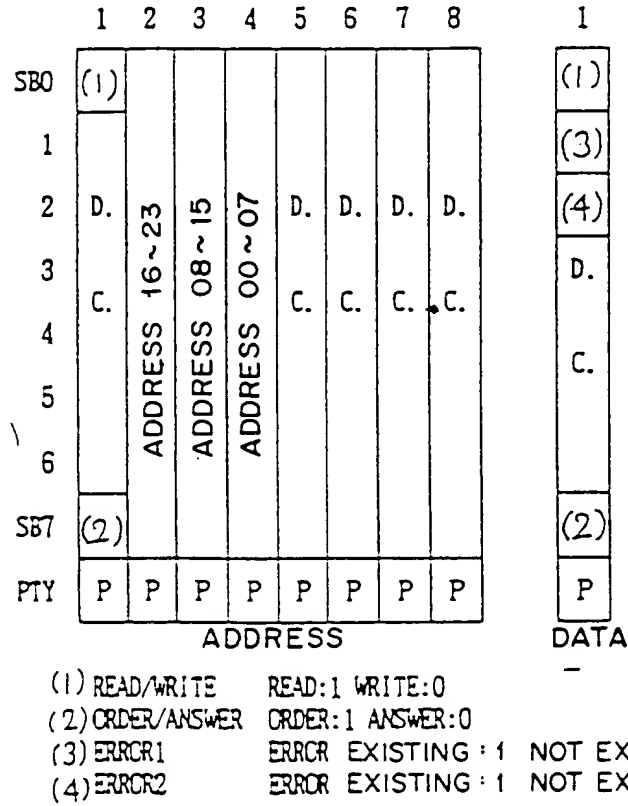


FIG. 198

ORDER TYPE	IN/OUT	ORDER	MSB		CONTENTS OF COMMANDS																						LSB				
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03
COMMAND ACTIVATION	OUT	0010	A	1	D.C.				(1)	D.C.				O	D.C.												ORDER				
			D	DC	NUMBER OF COMMANDS				COMMAND ADDRESS																						
RETRY INSTRUCTION	OUT	0100	A	1	D.C.				(1)	D.C.				O	D.C.												ORDER				
			D	D.C.																											
MSCN READ	IN	1000	A	1	D.C.				(1)	D.C.				O	D.C.												ORDER				
			D	MSCN READ DATA																											
WRITING TEST LOOPBACK DATA	OUT	0001	A	1	D.C.				(1)	D.C.				O	D.C.												ORDER				
			D	LOOPBACK DATA																											
READING TEST LOOPBACK DATA	IN	1001	A	1	D.C.				(1)	D.C.				O	D.C.												ORDER				
			D	LOOPBACK DATA																											

FIG. 199

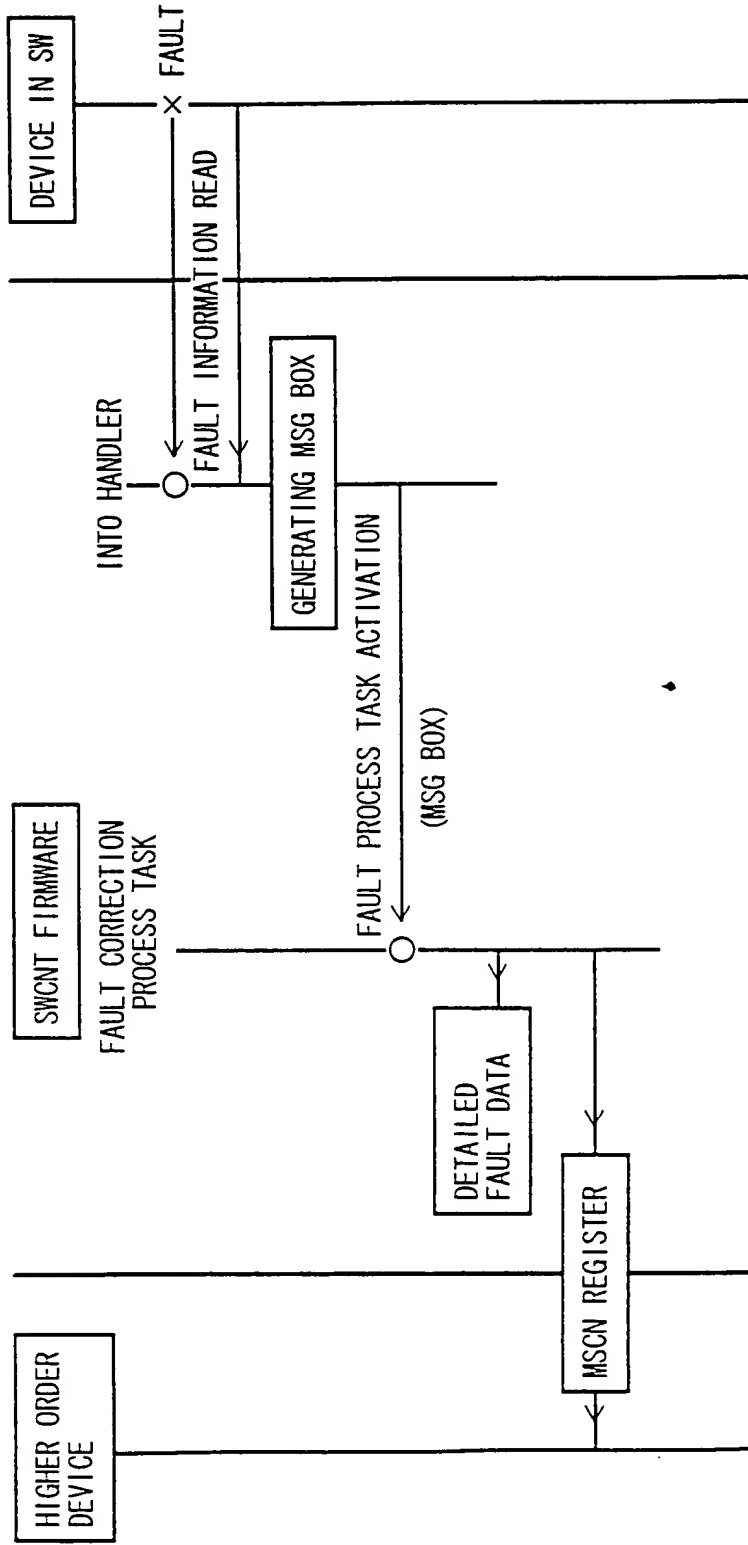


FIG. 200

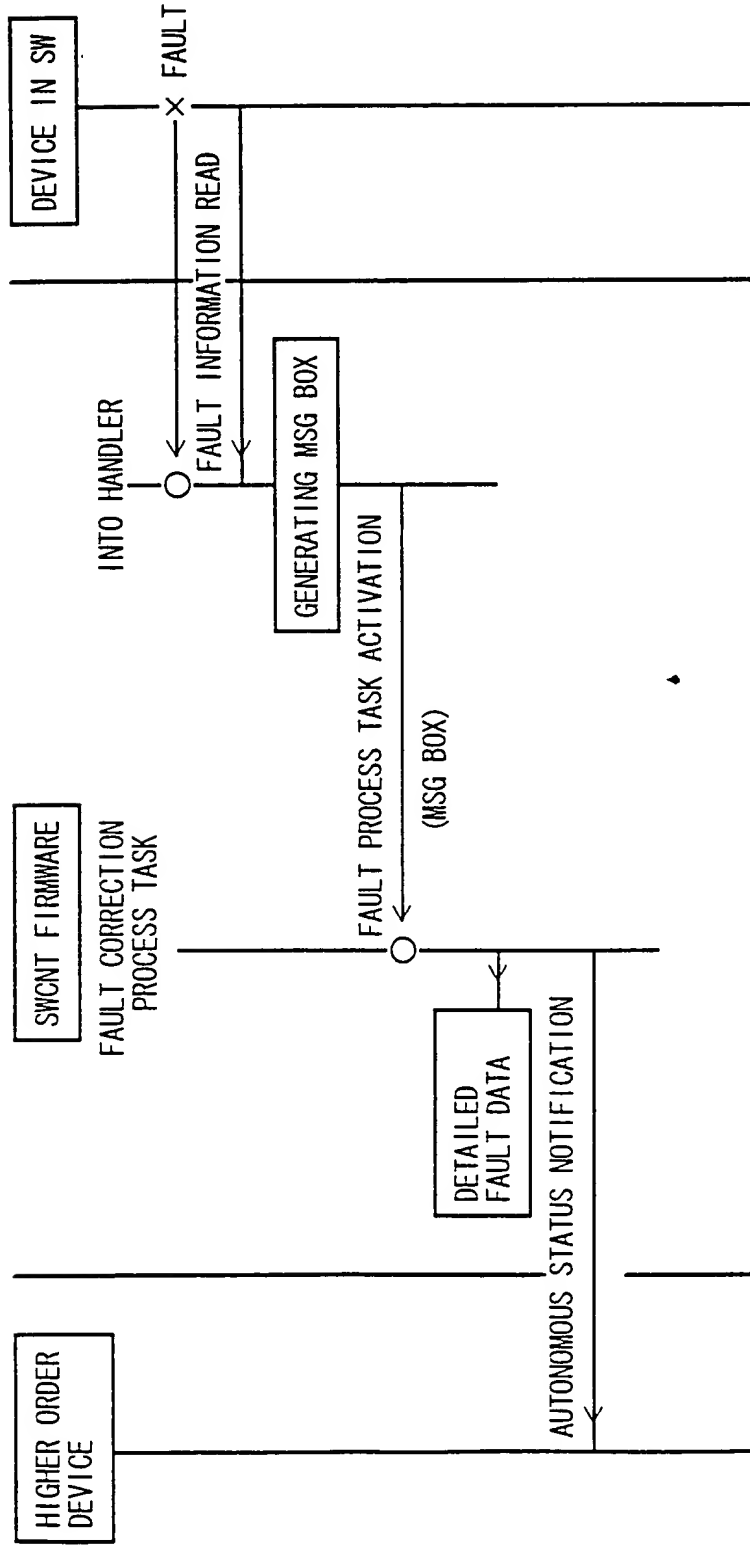


FIG. 201

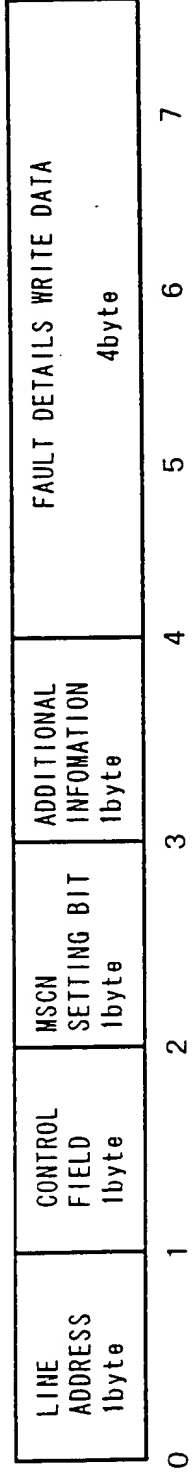


FIG. 202

		SCLK	SWMX - DOWN	SWMX - UP	16
		TWO SYSTEMS	INTRA-	INTER-	
		ONE SYSTEM	INTRA-	INTER-	
		IN P			

[illegible]

FIG. 203

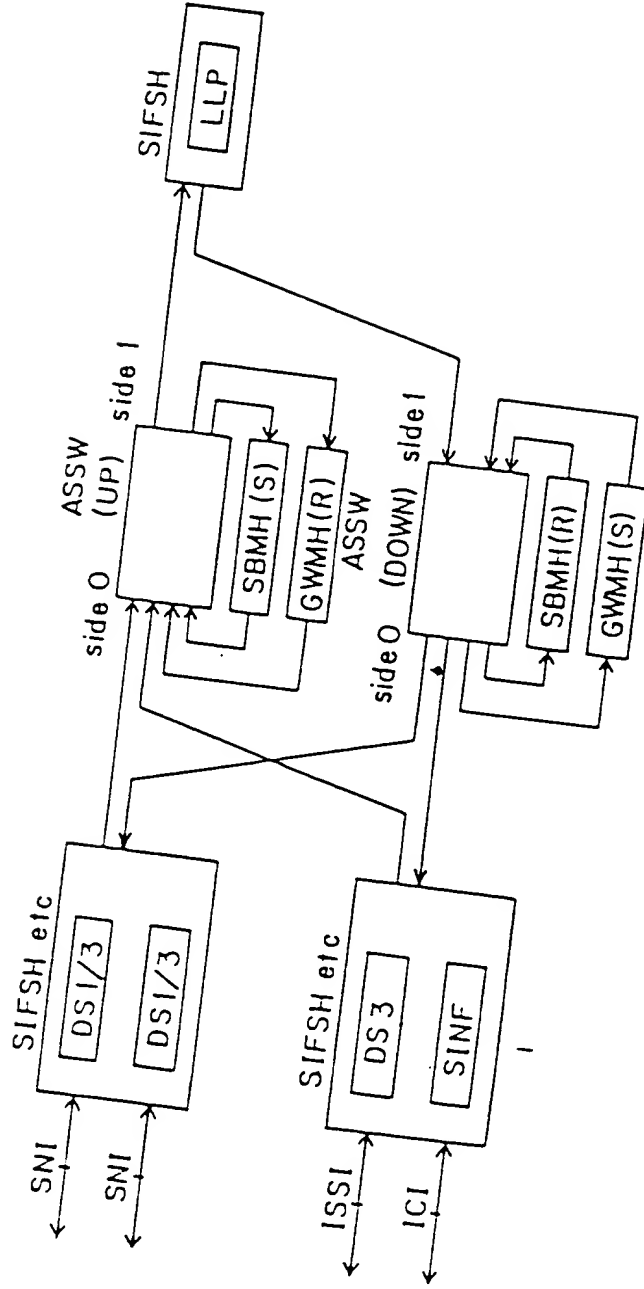


FIG. 204

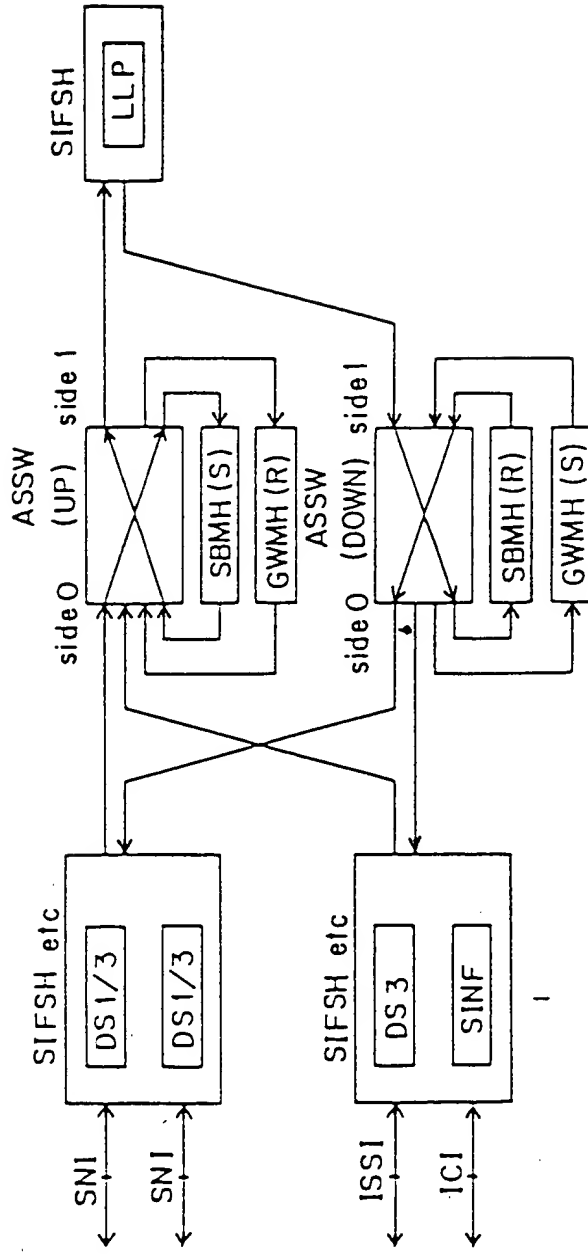


FIG. 205

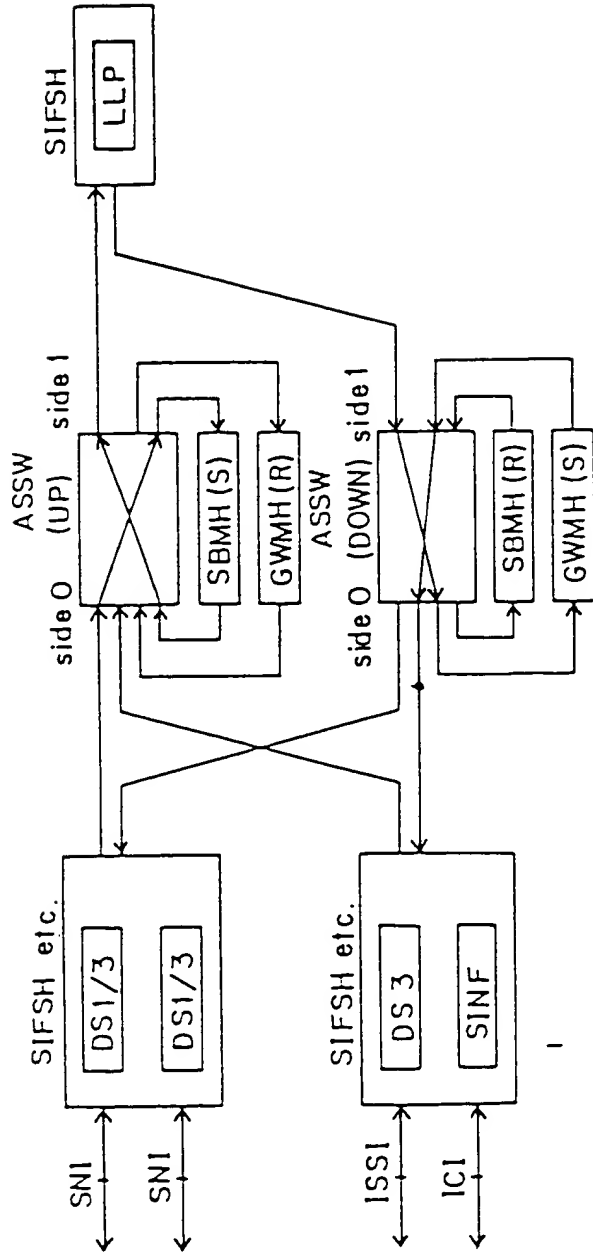


FIG. 206

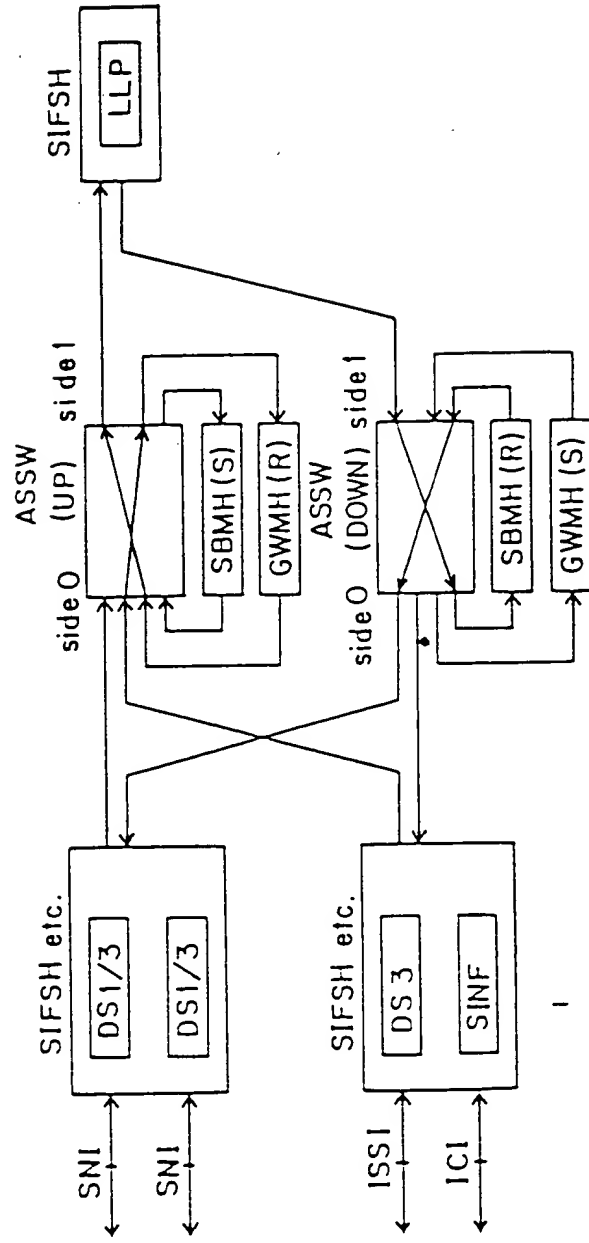


FIG. 207

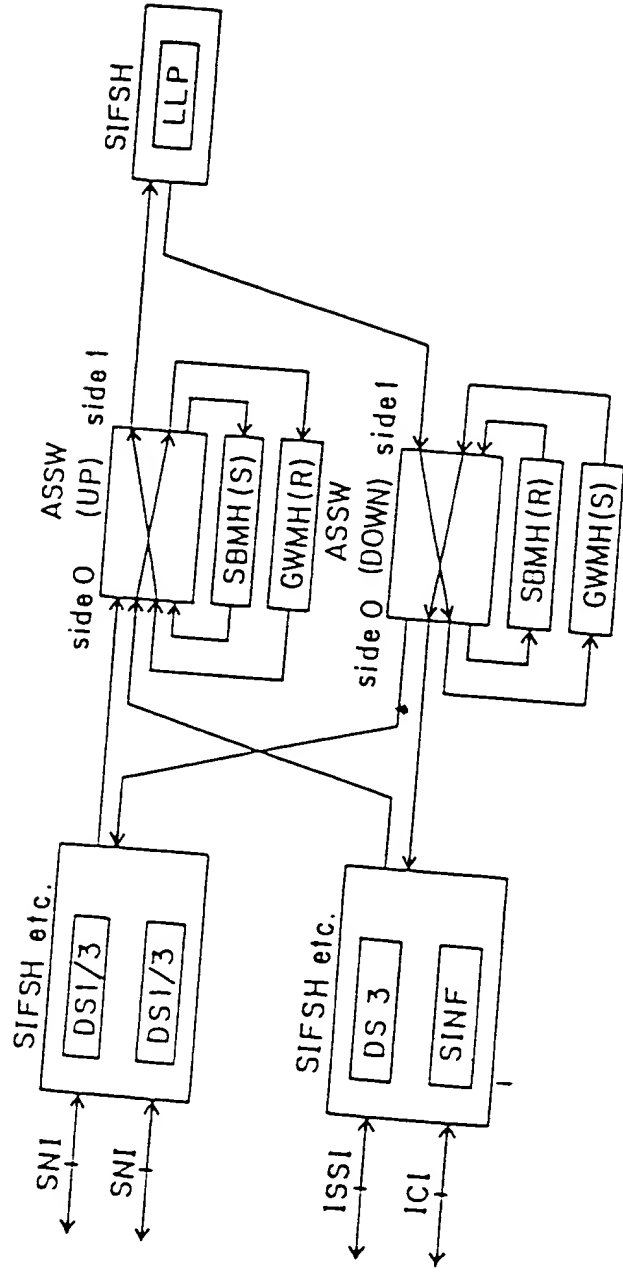


FIG. 208

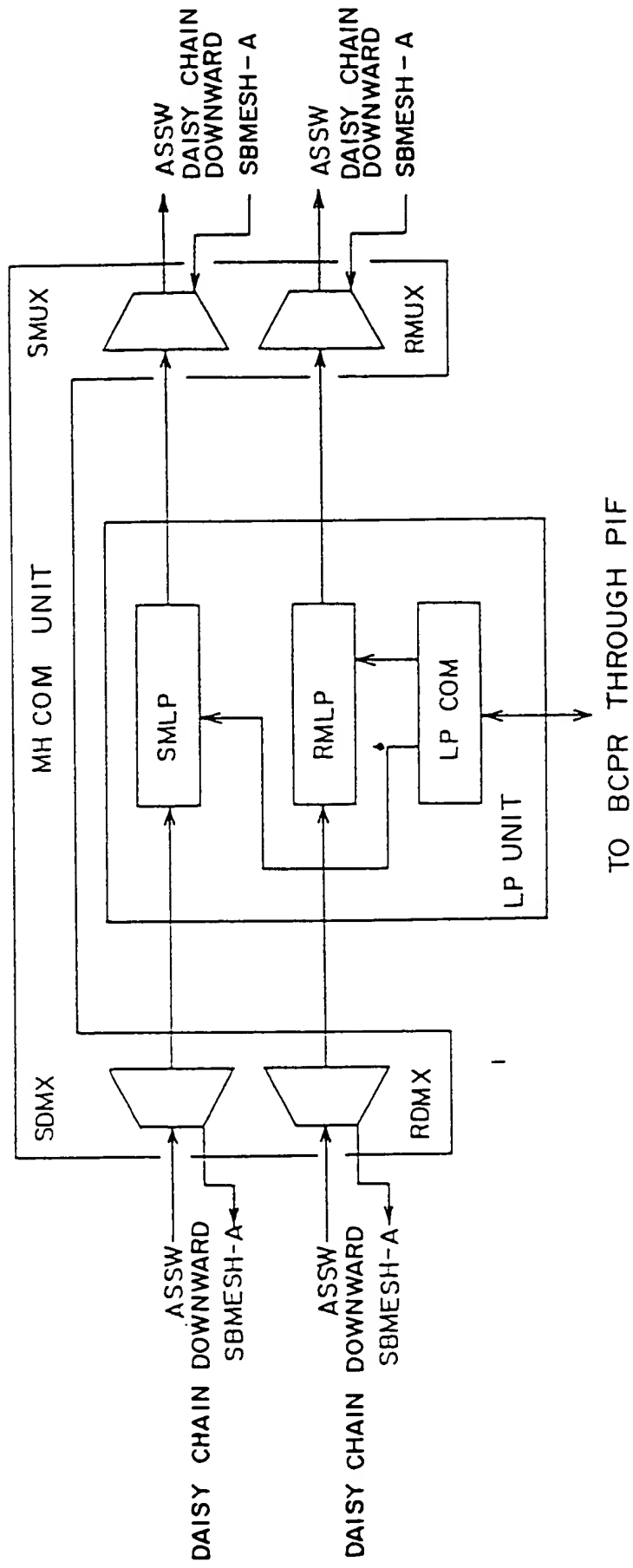


FIG. 209

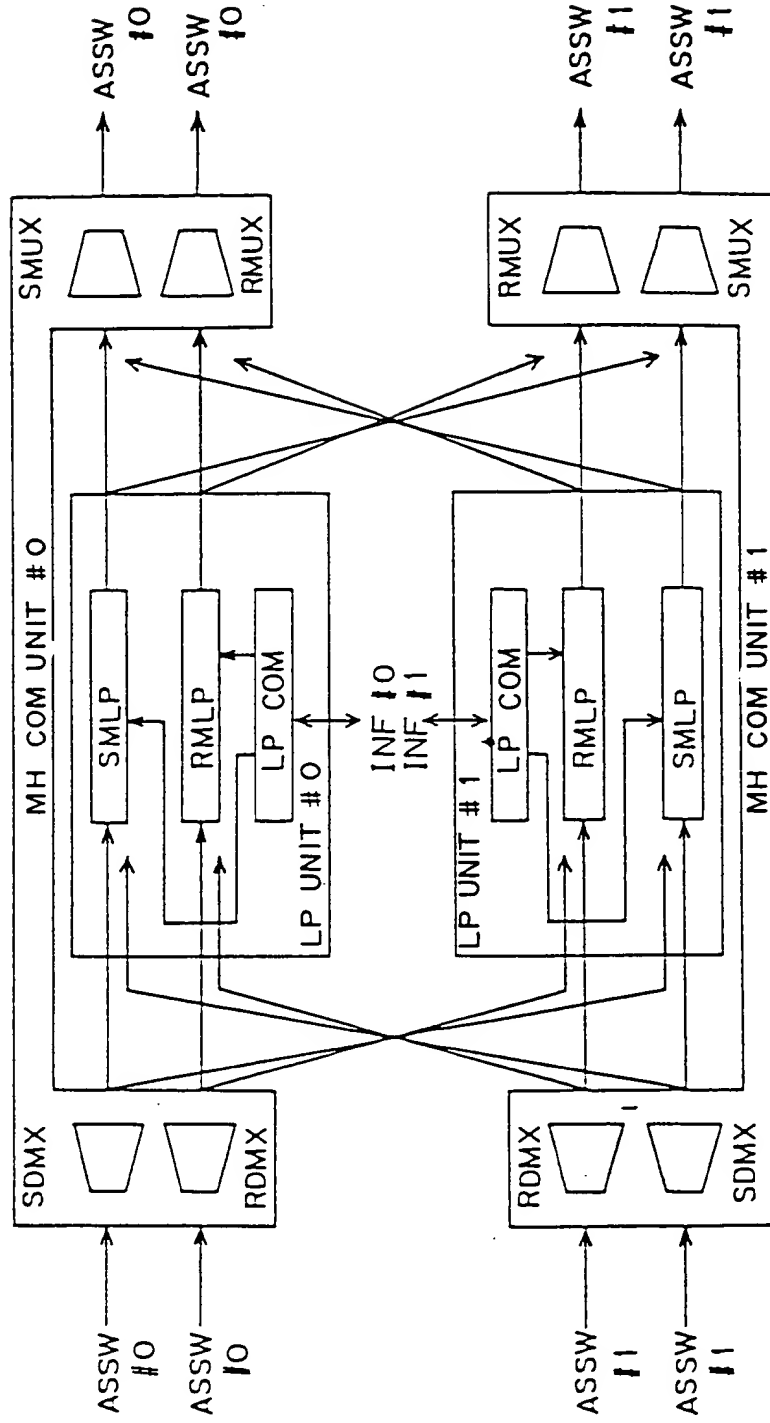


FIG. 210

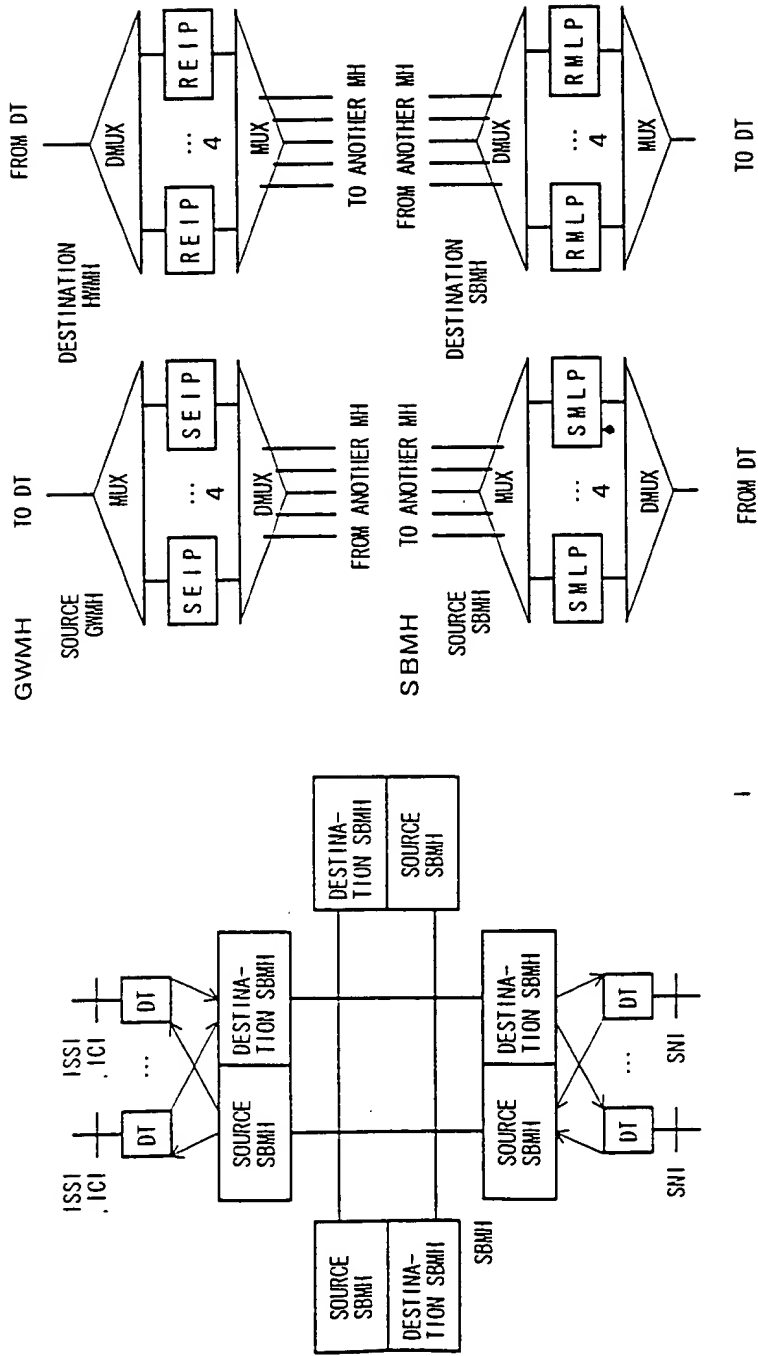
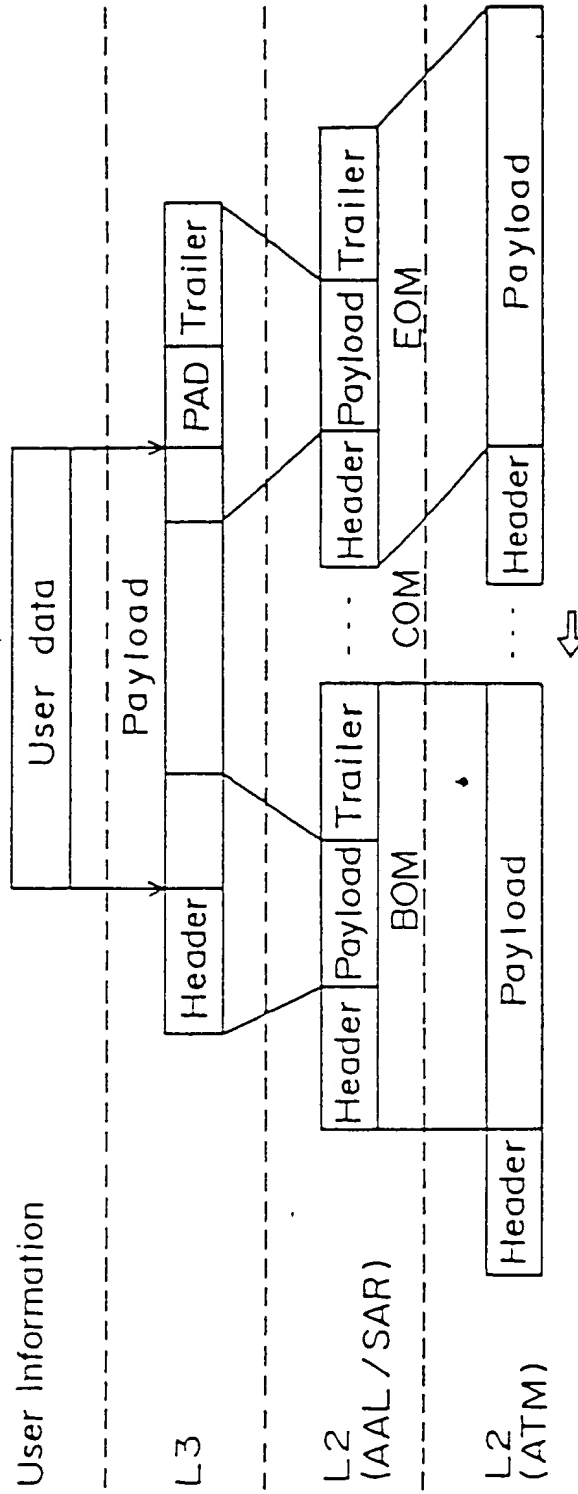


FIG. 211



BOM : Beginning of Message
 COM : Continuation of Message
 EOM : End of Message
 SAR : Segmentation and Re-assembly

FIG. 212

VCI/MID ALLOCATING SYSTEM BY CELL TYPE

	OUTPUT VCI DETERMINING SYSTEM	OUTPUT MID DETERMINING SYSTEM
S S M	DETERMINED BY DA FULL ANALYSIS	ASSIGNING NON-USED MID
B O M		
C O M	RETRIEVING ROUTING MEMORY BY INPUT VCI/MID	
E O M		

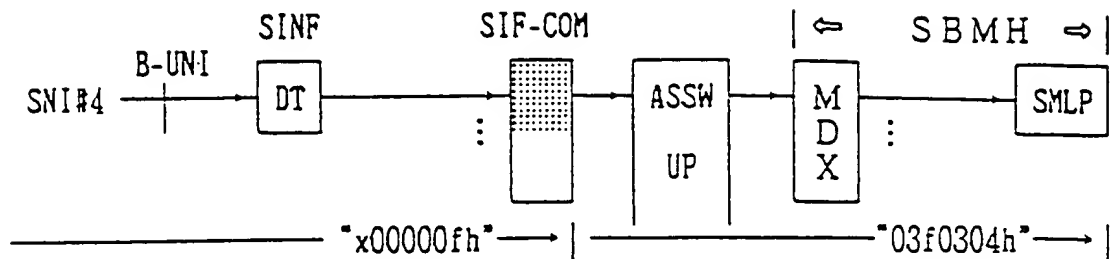
F I G . 2 1 4

Approved for Release

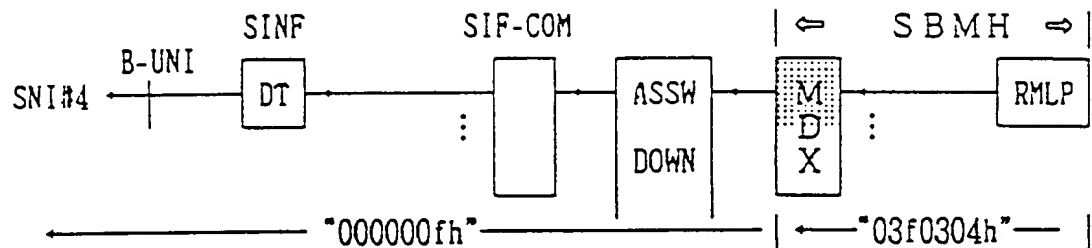
SNI No	VPI (hex)	VCI (hex)
SNI# 0	03f	0300
SNI# 1	03f	0301
⋮	⋮	⋮
SNI#31	03f	031f

FIG. 216

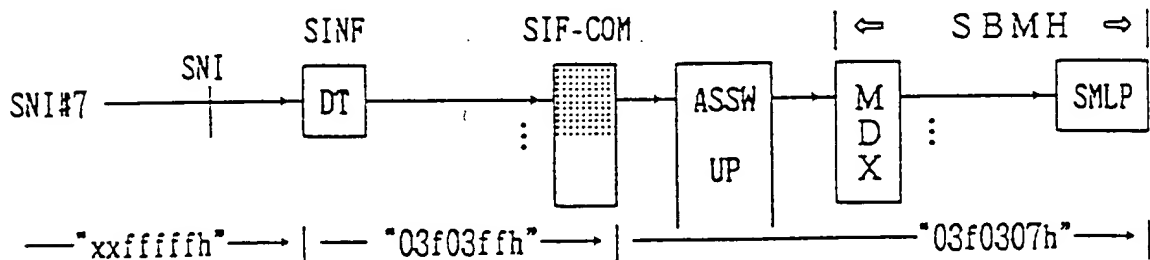
- FROM B-UNI TO SMLP (UPWARD)



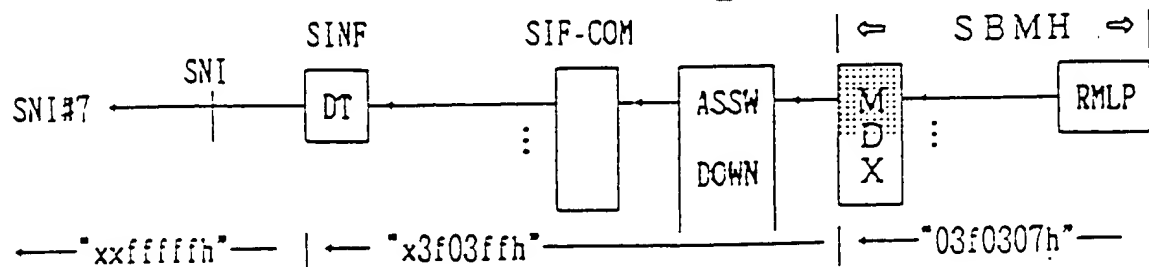
- FROM RMLP TO B-UNI (DOWNWARD)



- FROM SNI TO SMLP (UPWARD)



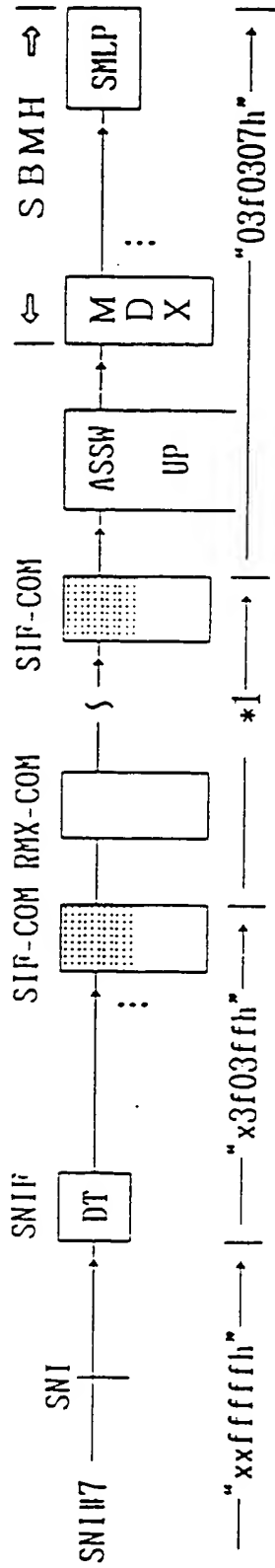
- FROM RMLP TO SNI (DOWNWARD)



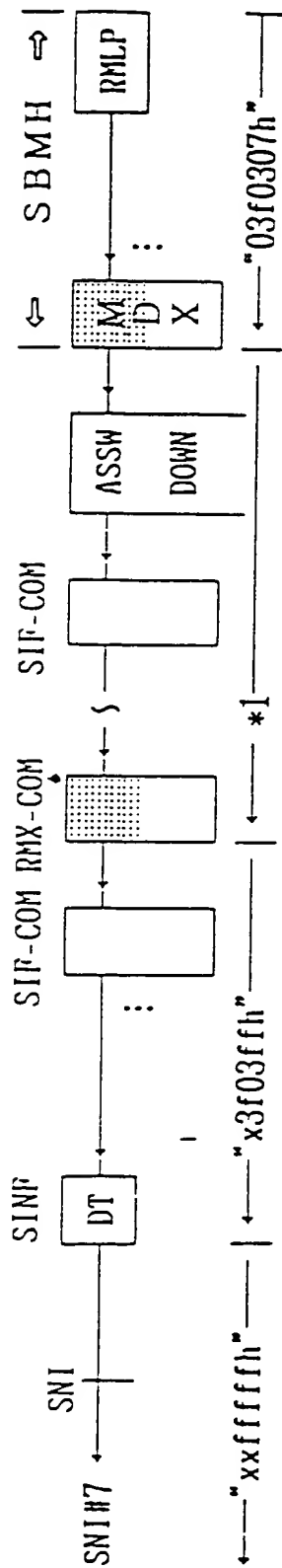
INDICATES POSITION OF VCC

FIG. 217

• FROM SNI (IN BRLC) TO SMLP (UPWARD)



• FROM RMLP TO SNI (IN BRLC) (DOWNWARD)



INDICATES POSITION OF VCC

FIG. 218

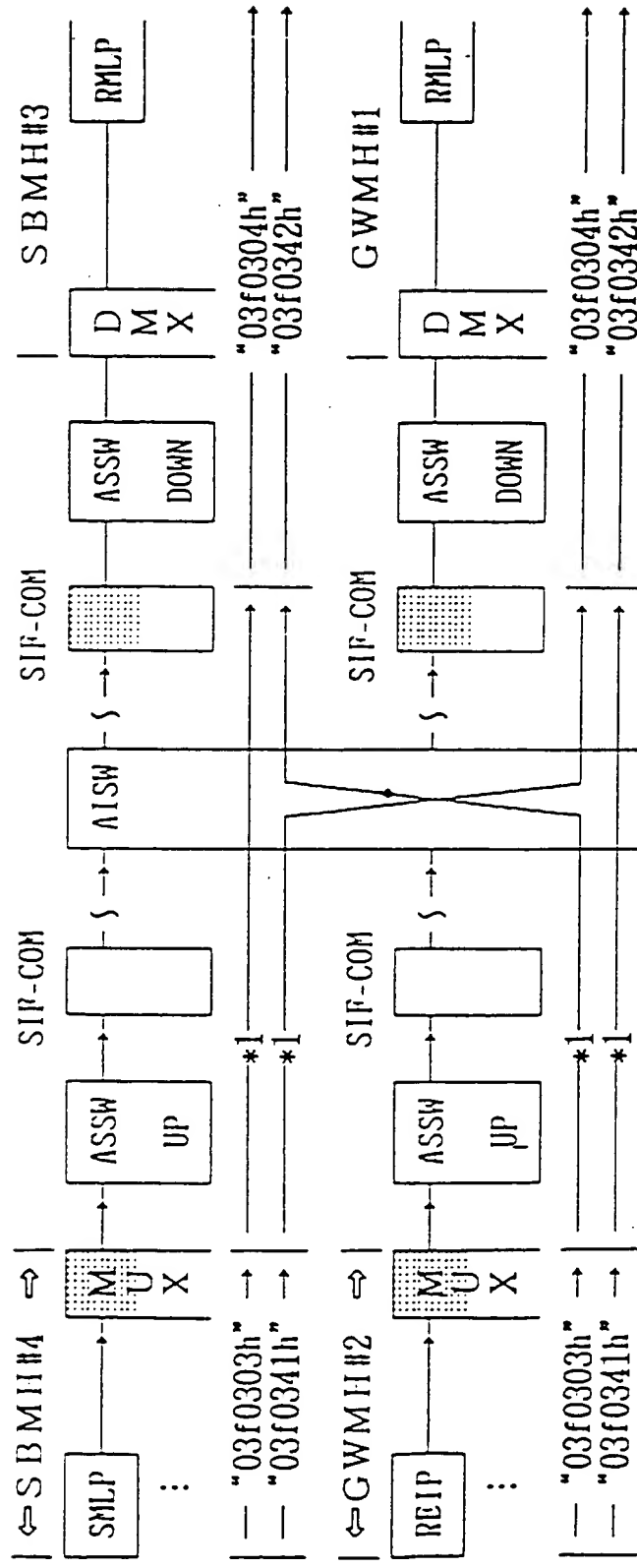
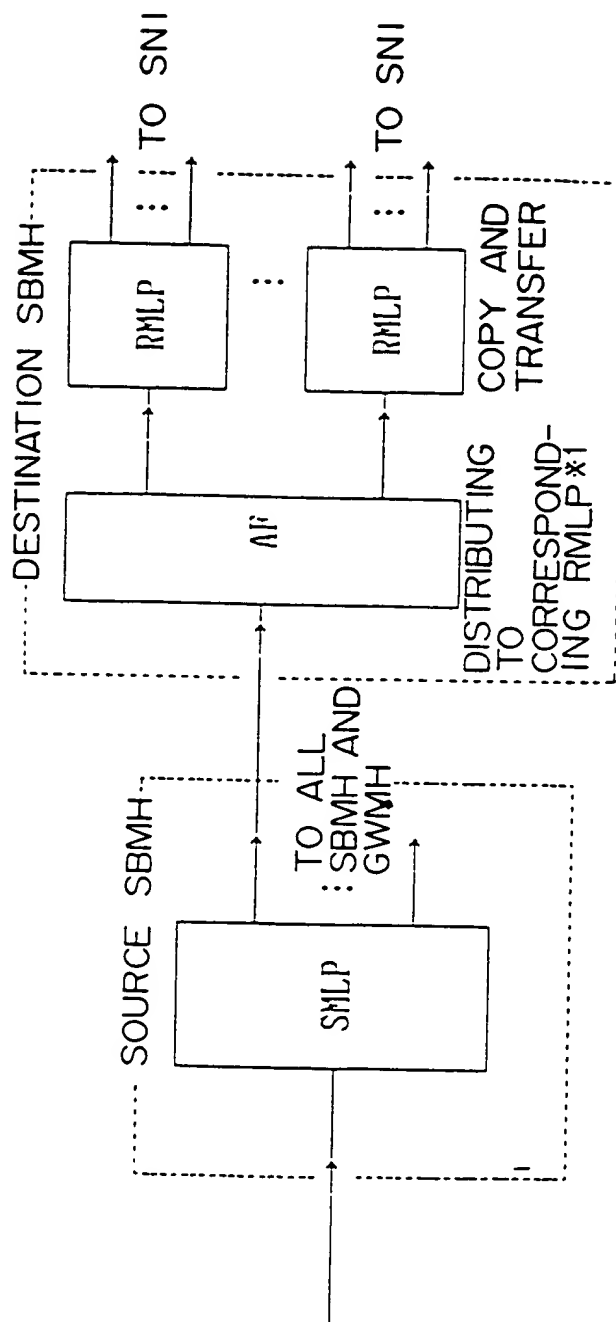


FIG. 220

SMLP	RANGE OF MID (hex)
SMLP#0	000 ~ 0ff
SMLP#1	100 ~ 1ff
SMLP#2	200 ~ 2ff
SMLP#3	300 ~ 3ff

FIG. 221



*1: DISCARDED IF THERE IS NO SNI TO ACCOMMODATE
CORRESPONDING GA IN DESTINATION SBMH

FIG. 222

	DETERMIN- ATION	DETERMIN- ATION AREA	PROCESS EXAMPLES
S M L P	SOURCE SNI	INPUT VCI	Screening, Traffic Measure, Etc.
	L3 PDU	INPUT VCI/MID	SN Check, Routing, Etc.
R M L P	DESTINA- TION SNI	OUTPUT VCI	Screening, Traffic Measure, Etc.
	L3 PDU	OUTPUT VCI/MID	Routing Egress Restriction, Etc.

FIG. 223

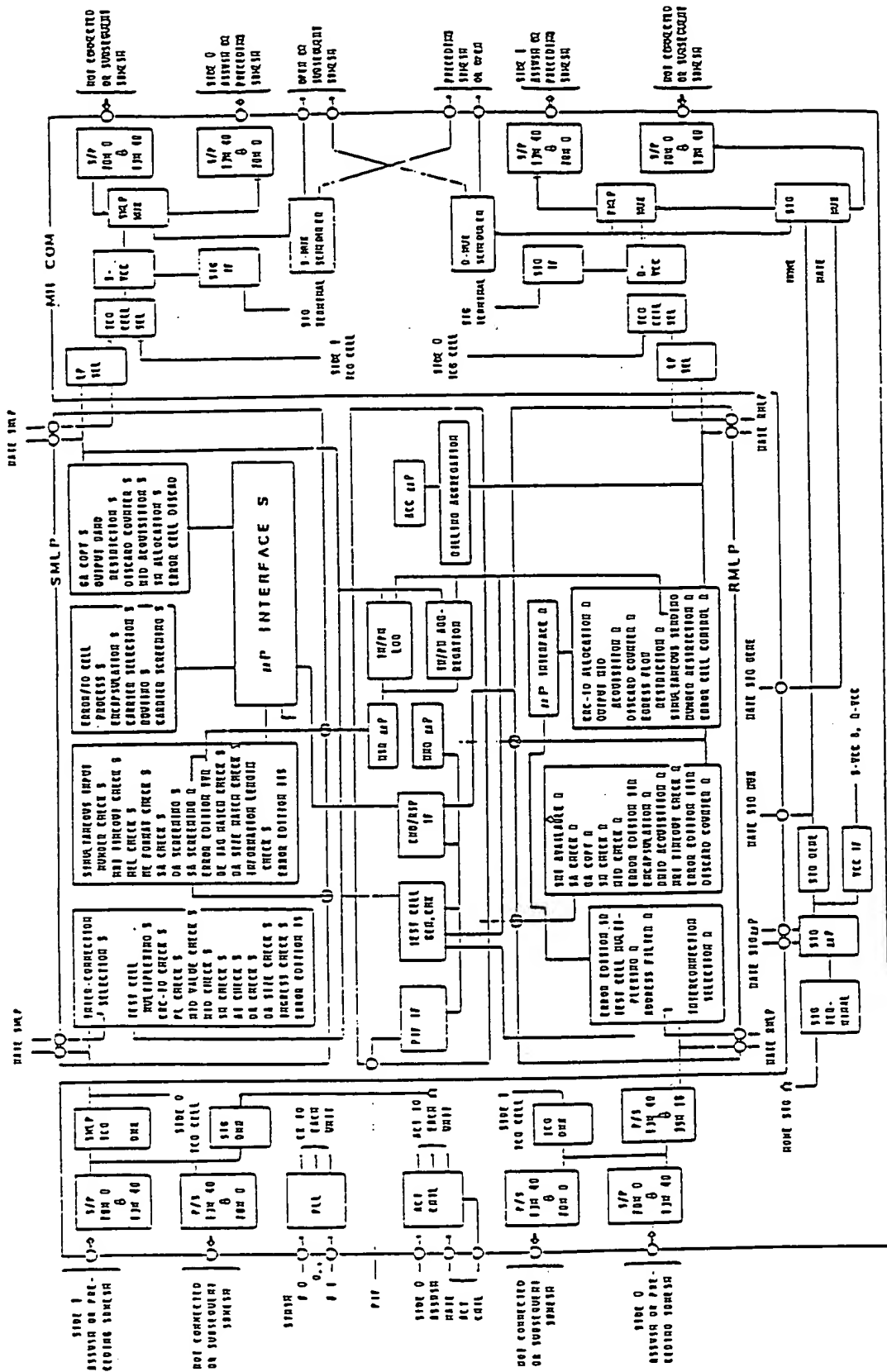
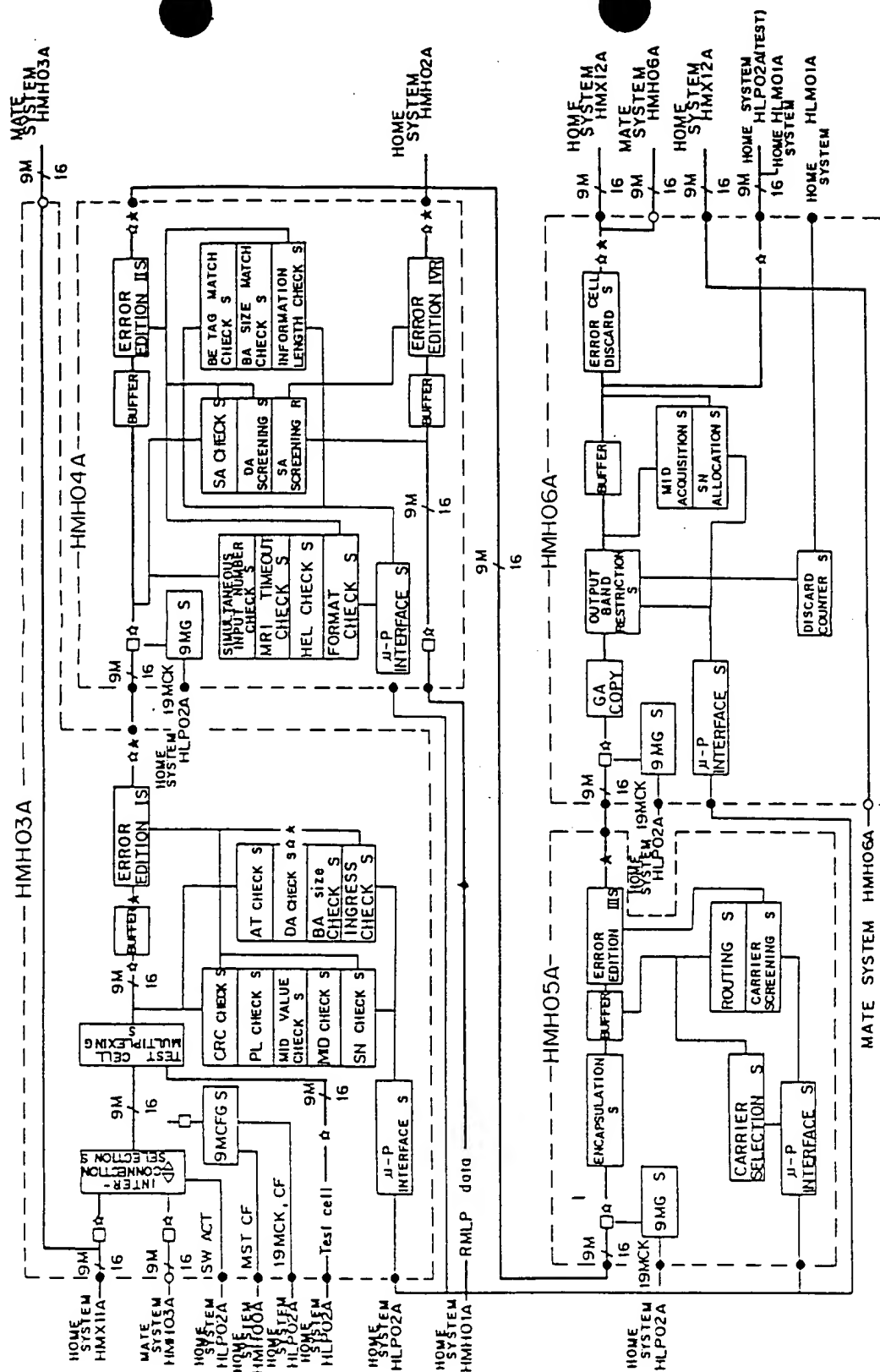


FIG. 224

○ : FRONT CABLE ● : B.W.B. — : CONTROL LINE — : DATA HIGHWAY
 ✕ : parity checker ★ : parity generator
 □ : DETECTING DISCONNECTION OF CLOCK AND CELL FRAME
 ◁▷ : CLOCK SWITCHING POINT
 : BLOCK REQUIRING μ-P INTERFACE



ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PNCB
			SUB	ME	CC	MS	
01	INTER-CONNECTION SELECTION S	SELECTING MDX ACT SYSTEM DATA ACCORDING TO SWITCH SYSTEM INFORMATION. LOSING TCG CELL.	○	—	—	—	HMH 03A
02	TEST CELL MULTIPLEXING	MULTIPLEXING TEST CELL WHEN LINE IS IDLE. PRIORITIZING TEST CELL DURING DIAGNOSTICS.	○	○	—	—	
03	CRC-10 CHECK S	CRC DIVING CELL PAYLOAD CHECKING FOR ERRORS.	○	×	—	—	
04	PL LENGTH CHECK S	CHECKING WHETHER OR NOT PAYLOAD LENGTH INDICATES PREDETERMINED VALUE.	○	×	○	—	
05	MID VALUE CHECK S	CHECKING WHETHER OR NOT MID VALUEE IS PREDETERMINED VALUE.	○	×	○	—	
06	MID CHECK S	CHECKING WHETHER VCI/MID IS NOT ACTIVE AT BOM, AND WHETHER VCI/MID IS ACTIVE AT COM AND EOM.	○	×	△	—	
07	SN CHECK S	INITIALIZING SN AT BOM AND SSM. AND CHECKING ORDER OF SN AT COM AND EOM	○	×	△	—	
08	AT CHECK S	CHECKING WHETHER OR NOT ADDRESS TYPE INDICATES PREDETERMINED VALUE.	○	×	○	—	
09	DA CHECK S	CHECKING WHETHER DA IS NOT IA ENTERED IN INPUT SNI.	○	×	○	—	
10	BAsize CHECK S	CHECKING WHETHER OR NOT BA SIZE INDICATES PREDETERMINED VALUE.	○	×	○	—	
11	INGRESS FLOW CHECK S	CHECKING WHETHER OF NOT SNI OF DS3 MEETS ACCESS CLASS OF CLASSES 1-4.	○	×	×	—	
12	ERROR EDITION I	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG.	○	×	○	—	
13	SIMULTANEOUS INPUT NUMBER CHECK S	LIMITING NUMBER OF MID SIMULTANEOUSLY INPUT FROM 1 SNI TO 1 OR 16.	○	×	○	○	HMH 04A
14	MRI TIMEOUT CHECK S	CHECKING TIME FROM BOM TO EOM IN 1 L3 PDU UNITS.	○	×	○	○	
15	HEL CHECK S	CHECKING WHETHER OR NOT HEADER EXTENSION LENGTH INDICATES PREDETERMINED VALUE.	○	×	—	×	
16	HE FORMAT CHECK S	CHECKING FORMAT OF HEADER EXTENSION.	○	×	—	×	

SUB : SNI LOOPBACK TEST CELL ME : INTER-MH PVC TEST CELL CC : CRC-10-ERROR CELL MS : MASTER ERROR CELL
 ○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS × : NOT OBJECT OF PROCESS
 — : NO CELL PASSES OR NO RELATED CELLS △ : CHECKING BUT NO WRITING TO MEMORY.

FIG. 226

ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	ME	CC	MS	
17	SA CHECK S	CHECKING WHETHER SA IS AN IA ENTERED IN INPUT SNI.	○	×	—	○	HMH 04A
18	DA SCREENING	RECEPTION IS LIMITED AT DA IN INPUT SNI UNITS. SHARED WITH TABLE OF RMLP SA SCREENING R.	○	×	—	○	
19	BE tag MATCH CHECK S	CHECKING WHETHER OR NOT BE TAG OF SIP L3 HEADER MATCHES BE TAG OF TRAILER.	○	×	—	○	
20	BA size MATCH CHECK S	CHECKING WHETHER OR NOT BA SIZE OF SIP L3 HEADER MATCHES BE LENGTH OF TRAILER.	○	×	—	○	
21	INFORMATION LENGTH CHECK S	CHECKING WHETHER OR NOT ACTUAL LENGTH OF L3 PDU MATCHES LENGTH OF SIP L3 TRAILER.	○	×	—	○	
22	ERROR EDITION II	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG.	○	×	—	○	HMH 05A
23	ENCAPSULATION S	CHANGING SIP INTO FORMAT OF INTER-MH INF. PDU: ADDING ISSI-L3 DTPDU HEADER AND CGV HEADER TO NEW BOM.	○	○	—	○	
24	CARRIER SELECTION S	SETTING SIP L3 HEADER CARRIER OR CARRIER ENTERED IN SNI UNITS IN CARRIER AREA IN ISSI L3 DTPDU HEADER.	○	○	—	○	
25	ROUTING S	SPECIFYING, FROM DA, MH(SBMH/GVMH) ACCOMMODATING DESTINATION SNI.	○	○	—	○	
26	CARRIER SCREENING S	LIMITING SENDING OF CARRIER.	○	○	—	○	HMH 06A
27	GA COPY S	OUTPUT CELL INPUT AT GA TO EACH SUBSCRIBER.	○	○	—	○	
28	OUTPUT BAND RESTRICTION S	LIMITING OUTPUT BAND (PEAK RATE) FOR EACH OUTPUT MH.	○	○	—	○	
29	DISCARD COUNT S	COUNTING NUMBER OF L2 AND L3 MESSAGES DISCARDED BY OUTPUT BAND RESTRICTION AND REPORTING IT TO PM OF LP-COM.	○	○	—	○	
30	MID ACQUISITION S	ASSIGNING OUTPUT MID TO OUTPUT MH UNIT.	○	○	—	×	
31	SN ALLOCATION S	ASSIGNING SEQUENCE NUMBER (SN).	○	○	—	○	
32	ERROR CELL DISCARD S	MASTER ERROR (MS) OF ERROR FLAG DISCARDS NG CELLS.	○	○	—	○	

SUB : SNI LOOPBACK TEST CELL ME : INTER-MH PVC TEST CELL CC : CRC-10 ERROR CELL MS : MASTER ERROR CELL
 ○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS × : NOT OBJECT OF PROCESS
 — : NO CELL PASSES OR NO RELATED CELLS

FIG. 227

ITEM	BLOCK NAME	CONTENTS	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	ME	CC	MS	
3 3	μ -P INTERFACE S	INTERFACING WITH MHG μ -P OF HLP01A	—	—	—	—	COMMON TO PWCB
3 4	9MG S	GENERATING CLOCK BASED ON 19M CLOCK RECEIVED FROM HLP02A AND CELL FRAME	—	—	—	—	
3 5	9MCEG S	GENERATING 9M CLOCK BASED ON 19M CLOCK RECEIVED FROM HLP02A AND CELL FRAME, AND REFERENCE CELL FRAME BASED ON SNLP.	—	—	—	—	HMH 03A

SUB : LOOPBACK TEST CELL ME : INTER-NH PVC TEST CELL CC : ERROR CELL MS : MASTER ERROR CELL
 O : APPLIED FOR PROCESS OBJECT OR DURING PROCESS x : NOT OBJECT OF PROCESS — : NO CELL PASSES OR NO RELATED CELLS

FIG. 228

[illegible]

FIG. 229

E F BLOCK NAME	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 MA	E1 MA	E2 SH	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	PV C
DA CHECK S (B/S)	OH	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	M
BA SIZE CHECK S (B/S)	OH	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	—	—	M
INGRESS FLOW CHECK S (B/S)	OH	O	—	—	—	—	—	—	—	—	—	O	ON	—	—	—	—	—	—	—	—	—	—	—	M
SIMULTANEOUS INPUT NUMBER CHECK S (E)	OH O	O	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	—	M
SIMULTANEOUS INPUT NUMBER CHECK S (C)	OH O	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M
WRI TIME OUT S (E)	OH O	O	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	—	M
HEL CHECK S (B/S)	OH O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	—	—	M
HE FORMAT CHECK S - 1ST (B/S)	OH O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	↓	ON	—	—	—	—	—	—	—	M
HE FORMAT CHECK S - 2ND (B/S)	OH O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	—	M
SA CHECK A (B/S)	OH —	—	—	—	—	—	—	I	—	—	—	—	—	—	—	—	—	—	ON	—	—	—	—	—	

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG.
 'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK.
 'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.
 '—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.

FIG. 230

BLOCK NAME	E F	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 IM	E1 MA	E2 MA	E1 SN	E2 SN	E1 DT	E2 DT	E1 DA	E2 DA	E1 BA	E2 BA	E1 AC	E2 AC	E1 EN	E2 EN	E1 MT	E2 MT	E1 HE	E2 HE	E1 VE	E2 VE	E1 CS	E2 CS	E1 SA	E2 SA	E1 DA	E2 DA	E1 BE	E2 BE	E1 LE	E2 LE	E1 IL	E2 IL	E1 EB	E2 EB	E1 PV	E2 PV								
DA SCREENING S (B/S)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M						
BE TAG MATCH S (E)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M						
BA SIZE MATCH CHECK S (E)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M						
INFORMATION LENGTH CHECK S (S/C/E)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M						
ENCAPSULATION S (C/E)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M						
*1 WHEN L2-PDU WHOSE 'EIMS' IS ON IS RECEIVED AT BOW AND COM HAVING SAME RMID VALUE, SUBSEQUENTLY RECEIVED COM AND EOW HAVE 'EIMS' SET 'ON'.																																																			
CARRIER SELECTION S (ISSIB)		ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M					
ROUTING S		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M					
CARRIER SCREENING (ISSIB)		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M					
GA COPY S (C/E)		*2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	M					
*2 BOW WHOSE 'EFMS' INDICATES NG (ON) IS NOT COPIED, BUT ORIGINAL CELL IS SET MHID AND TRANSMITTED IF COM AND EOW ARE FIRST NG CELL, THEY ARE COPIED.																																																			

'ON' : EF WHICH IS SET ON WHEN CHECK RESULT INDICATES NG. '—' : CHECK IS MADE REGARDLESS OF OK/NG OF EF WITH THIS MARK.
 'O' : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK. 'M' : NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 231

BLOCK NAME	EF	E1 MS	E1 RM	E2 PL	E2 IM	E1 IM	E2 MA	E1 MA	E2 SN	E2 DT	E2 ST	E2 DA	E2 BA	E2 AC	E2 EM	E2 MT	E2 HE	E2 VE	E2 CS	E2 SA	E2 DA	E2 BE	E2 LE	E2 IL	E2 EB	E2 C
OUTPUT BAND CONTROL S		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NID ACQUISITION S		O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SN ASSIGNMENT S		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ERROR CELL DISCARD S		x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

OH : EF WHICH IS SET ON WHEN CGECK RESULT INDICATES NG.
 O : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES OK.
 x : CHECK IS MADE ONLY WHEN EF WITH THIS MARK INDICATES NG.

FIG. 232

DATA INTERFACE OF SWLP AND LPCOM

DATA INTERFERENCE OF UNIT IN UNIT TEST CELL RECEIVING UNIT INTERFACE (TRANSMITTED FROM SAME INTERFACE)

[illegible]

	SNI ID (INPUT VC1) 4bit	PRECEDING CELL					
00	SIP ST	INPUT MID				SNI ID (INPUT VC1)	
01	TRIAL CP	VPI	OUTPUT VCI (DESTINATION MH ID)				PT
02		BC TRIAL					CLP
03	ST	SN	OUTPUT MID (USED AS RUID IN PROCESS)				
04	RSV		BE tag				
05	BA size						
06	DA						
07	TS04 THROUGH TS25 DEPEND ON EACH SEGMENT TYPE						
08	REFER TO CHAPTER 10						
09							
10	SA						
11							
12							
13	CLB						
14	HLP		PL	00\$		HEL3	
15	Brdg						
16		3					0
17		1					
18							
19							
20							
21							
22							
23							
24	RSV		BE tag				
25	Length						
26	PL Len.	CRC					

Error = L

88

WT MRI time out

CC	Payload CRC Violation
1	0
2	0
3	0
4	0
5	0
6	0
7	0
8	0
9	0
10	0
11	0
12	0
13	0
14	0
15	0
16	0
17	0
18	0
19	0
20	0
21	0
22	0
23	0
24	0
25	0
26	0
27	0
28	0
29	0
30	0
31	0
32	0
33	0
34	0
35	0
36	0
37	0
38	0
39	0
40	0
41	0
42	0
43	0
44	0
45	0
46	0
47	0
48	0
49	0
50	0
51	0
52	0
53	0
54	0
55	0
56	0
57	0
58	0
59	0
60	0
61	0
62	0
63	0
64	0
65	0
66	0
67	0
68	0
69	0
70	0
71	0
72	0
73	0
74	0
75	0
76	0
77	0
78	0
79	0
80	0
81	0
82	0
83	0
84	0
85	0
86	0
87	0
88	0
89	0
90	0
91	0
92	0
93	0
94	0
95	0
96	0
97	0
98	0
99	0
100	0
101	0
102	0
103	0
104	0
105	0
106	0
107	0
108	0
109	0
110	0
111	0
112	0
113	0
114	0
115	0
116	0
117	0
118	0
119	0
120	0
121	0
122	0
123	0
124	0
125	0
126	0
127	0
128	0
129	0
130	0
131	0
132	0
133	0
134	0
135	0
136	0
137	0
138	0
139	0
140	0
141	0
142	0
143	0
144	0
145	0
146	0
147	0
148	0
149	0
150	0
151	0
152	0
153	0
154	0
155	0
156	0
157	0
158	0
159	0
160	0
161	0
162	0
163	0
164	0
165	0
166	0
167	0
168	0
169	0
170	0
171	0
172	0
173	0
174	0
175	0
176	0
177	0
178	0
179	0
180	0
181	0

PL	Payload Length Error
1	0
2	0
3	0
4	0
5	0
6	0
7	0
8	0
9	0
10	0
11	0
12	0
13	0
14	0
15	0
16	0
17	0
18	0
19	0
20	0
21	0
22	0
23	0
24	0
25	0
26	0
27	0
28	0
29	0
30	0
31	0
32	0
33	0
34	0
35	0
36	0
37	0
38	0
39	0
40	0
41	0
42	0
43	0
44	0
45	0
46	0
47	0
48	0
49	0
50	0
51	0
52	0
53	0
54	0
55	0
56	0
57	0
58	0
59	0
60	0
61	0
62	0
63	0
64	0
65	0
66	0
67	0
68	0
69	0
70	0
71	0
72	0
73	0
74	0
75	0
76	0
77	0
78	0
79	0
80	0
81	0
82	0
83	0
84	0
85	0
86	0
87	0
88	0
89	0
90	0
91	0
92	0
93	0
94	0
95	0
96	0
97	0
98	0
99	0
100	0

80W/SSW With Invalid UID

WA	WID Currently Active/EOM with Unapproved WID

SN	Invalid Sequence Number
----	-------------------------

ST	Invalid SA Type

DT	Invalid DA Type
----	-----------------

	Invalid SUDS Address Type
AT	

DA	Individual DA Assigned to Org. SHI

DF	DA Field Format Error
1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	1
9	1
10	1
11	1
12	1
13	1
14	1
15	1
16	1
17	1
18	1
19	1
20	1
21	1
22	1
23	1
24	1
25	1
26	1
27	1
28	1
29	1
30	1
31	1
32	1
33	1
34	1
35	1
36	1
37	1
38	1
39	1
40	1
41	1
42	1
43	1
44	1
45	1
46	1
47	1
48	1
49	1
50	1
51	1
52	1
53	1
54	1
55	1
56	1
57	1
58	1
59	1
60	1
61	1
62	1
63	1
64	1
65	1
66	1
67	1
68	1
69	1
70	1
71	1
72	1
73	1
74	1
75	1
76	1
77	1
78	1
79	1
80	1
81	1
82	1
83	1
84	1
85	1
86	1
87	1
88	1
89	1
90	1
91	1
92	1
93	1
94	1
95	1
96	1
97	1
98	1
99	1
100	1

SF	SA Field Format Error
1	1
2	1
3	1
4	1
5	1
6	1
7	1
8	1
9	1
10	1
11	1
12	1
13	1
14	1
15	1
16	1
17	1
18	1
19	1
20	1
21	1
22	1
23	1
24	1
25	1
26	1
27	1
28	1
29	1
30	1
31	1
32	1
33	1
34	1
35	1
36	1
37	1
38	1
39	1
40	1
41	1
42	1
43	1
44	1
45	1
46	1
47	1
48	1
49	1
50	1
51	1
52	1
53	1
54	1
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57	1
58	1
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62	1
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64	1
65	1
66	1
67	1
68	1
69	1
70	1
71	1
72	1
73	1
74	1
75	1
76	1
77	1
78	1
79	1
80	1
81	1
82	1
83	1
84	1
85	1
86	1
87	1
88	1
89	1
90	1
91	1
92	1
93	1
94	1
95	1
96	1
97	1
98	1
99	1
100	1

BA	Invalid BAsize Field Value
----	----------------------------

AC	Access Class Violation

HE	Invalid HE Length Field Value
00000000	00000000
00000001	00000001
00000002	00000002
00000003	00000003
00000004	00000004
00000005	00000005
00000006	00000006
00000007	00000007
00000008	00000008
00000009	00000009
0000000A	0000000A
0000000B	0000000B
0000000C	0000000C
0000000D	0000000D
0000000E	0000000E
0000000F	0000000F
00000010	00000010
00000011	00000011
00000012	00000012
00000013	00000013
00000014	00000014
00000015	00000015
00000016	00000016
00000017	00000017
00000018	00000018
00000019	00000019
0000001A	0000001A
0000001B	0000001B
0000001C	0000001C
0000001D	0000001D
0000001E	0000001E
0000001F	0000001F
00000020	00000020
00000021	00000021
00000022	00000022
00000023	00000023
00000024	00000024
00000025	00000025
00000026	00000026
00000027	00000027
00000028	00000028
00000029	00000029
0000002A	0000002A
0000002B	0000002B
0000002C	0000002C
0000002D	0000002D
0000002E	0000002E
0000002F	0000002F
00000030	00000030
00000031	00000031
00000032	00000032
00000033	00000033
00000034	00000034
00000035	00000035
00000036	00000036
00000037	00000037
00000038	00000038
00000039	00000039
0000003A	0000003A
0000003B	0000003B
0000003C	0000003C
0000003D	0000003D
0000003E	0000003E
0000003F	0000003F
00000040	00000040
00000041	00000041
00000042	00000042
00000043	00000043
00000044	00000044
00000045	00000045
00000046	00000046
00000047	00000047
00000048	00000048
00000049	00000049
0000004A	0000004A
0000004B	0000004B
0000004C	0000004C
0000004D	0000004D
0000004E	0000004E
0000004F	0000004F
00000050	00000050
00000051	00000051
00000052	00000052
00000053	00000053
00000054	00000054
00000055	00000055
00000056	00000056
00000057	00000057
00000058	00000058
00000059	00000059
0000005A	0000005A
0000005B	0000005B
0000005C	0000005C
0000005D	0000005D
0000005E	0000005E
0000005F	0000005F
00000060	00000060
00000061	00000061
00000062	00000062
00000063	00000063
00000064	00000064
00000065	00000065
00000066	00000066
00000067	00000067
00000068	00000068
00000069	00000069
0000006A	0000006A
0000006B	0000006B
0000006C	0000006C
0000006D	0000006D
0000006E	0000006E
0000006F	0000006F
00000070	00000070
00000071	00000071
00000072	00000072
00000073	00000073

CS	Invalid HE Carrier Selection
----	------------------------------

VE	Invalid HE Version
----	--------------------

EW	Exceed Max. Number of CDU

SA	SA not Assigned to Org. SHI
----	-----------------------------

DS	DA Screening Violation
----	------------------------

BE	BETag Mismatch
----	----------------

IL	Incorrect Length
----	------------------

LE	Base Size Field not equal Length Field
----	--

UN	WID Assigned Error (UNIQUE SPECIFICATION)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32
33	33
34	34
35	35
36	36
37	37
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89	89
90	90
91	91
92	92
93	93
94	94
95	95
96	96
97	97
98	98
99	99
100	100

EB	End-User Blocking (UNIQUE SPECIFICATION)

10

1

「

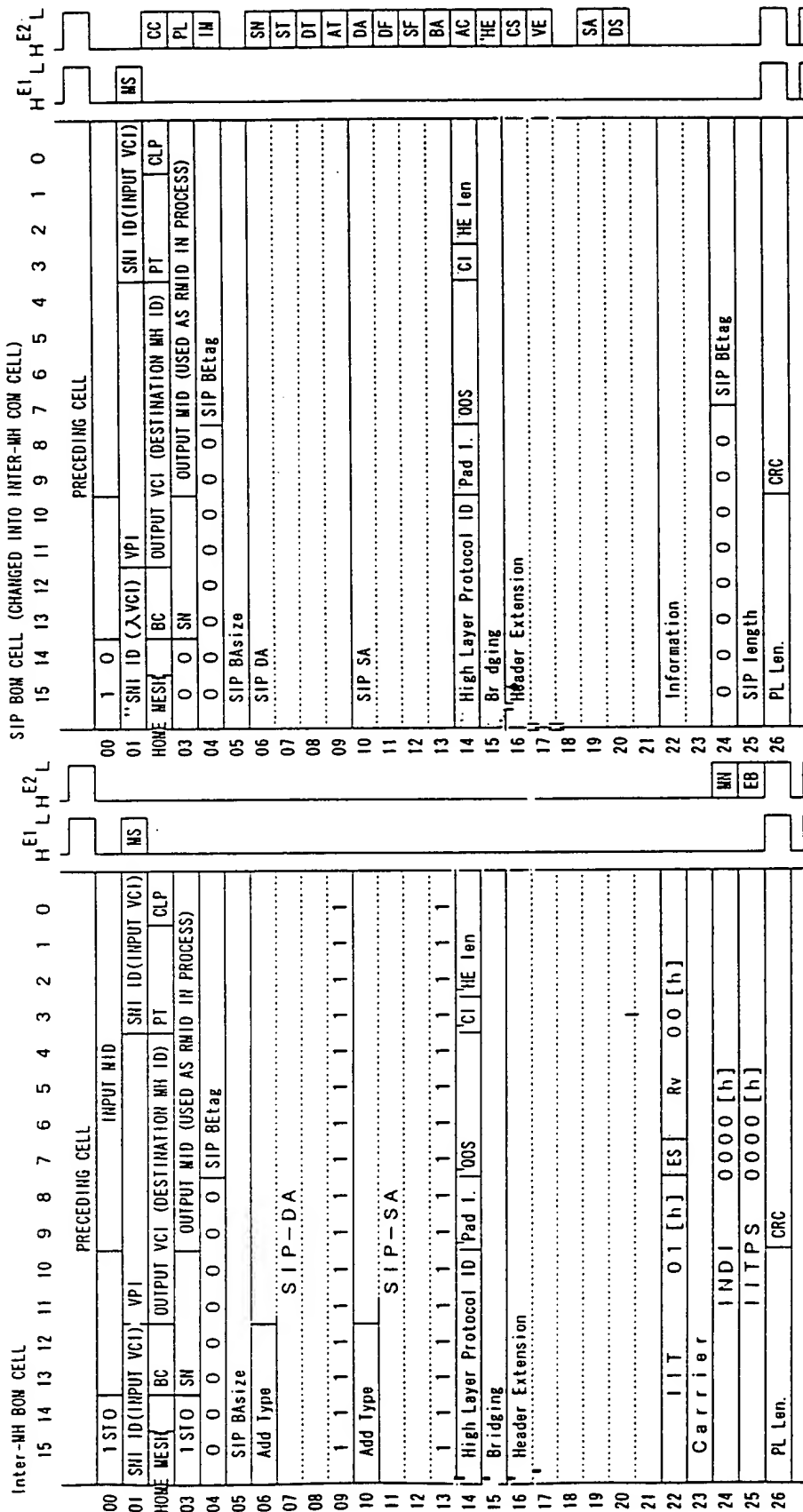
AREA CHANGED IN SENDING PROCESS UNIT

NOTE: FOR USE IN INTERNAL PROCESS IN EF1 EXCEPT MS

3
3
2
- 6
F

SIP ST : ST OF SIP FORMAT IS ENTERED. (ASSIGNED IN ERROR EDITION 1).
 BC : INDICATES WHERE TO BROADCAST TO. (ASSIGNED IN ROUTING PROCESS UNIT).
 DESTINATION MH ID : INDICATES OUTPUT VCI (DESTINATION MH ID).
 TRIAL : INDICATES WHETHER OR NOT IT IS PVC TEST CELL (INTERMESH/SNI LOOPBACK).
 TEST CELL IS 1. (ASSIGNED BEFORE CRC-10 CHECK PROCESS UNIT BETWEEN MESHS.
 ASSIGNED AT ROUTING PROCESS UNIT AT SNI LOOPBACK)
 SNI ID : 8-BIT LSB OF VCI INPUT FROM MDX. INDICATES SOURCE SNI ID.
 15-12 IS 4-BIT MSB (1-BIT MSB IS TEST BIT), AND 3-0 IS 4-BIT LSB (MOVED IN
 ERROR EDITION 1).
 HOME MESH : INDICATES WHETHER OR NOT IT IS LOOPBACK CELL TO HOME MESH (ASSIGNED IN DA
 CHECK PROCESS UNIT. LOOPBACK CELL TO HOME MESH DOES NOT REQUIRE RETRIEVAL
 OF ROUTE INFORMATION IN ROUTING PROCESS UNIT).
 OUTPUT VCI : DESTINATION MH ID. 1-BIT MSB OF TEST CELL IS 1.
 PT : PAYLOAD TYPE (NOT CHANGED IN PROCESS UNIT).
 CLP : CELL LOSS PRIORITY (NOT CHANGED IN PROCESS UNIT).
 ST : SEGMENT TYPE OF INTER-MH (REASSIGNMENT FROM SIP IN ENCAPSULATION PROCESS UNIT).
 SN : SEQUENCE NUMBER (REASSIGNMENT IN SN ASSIGNING UNIT).
 MID : MESSAGE IDENTIFIER 1. RMID FROM VCI* AND MID IS ENTERED IN SIMULTANEOUS INPUT
 NUMBER CHECK UNIT.
 2. OUTPUT MID IS ENTERED IN MID ACQUIRING UNIT.
 SAR PL : SAR PAYLOAD,
 PL : PL OF SIP IS INPUT.
 CRC : REASSIGNED IN CRC-10 ASSIGNING UNIT.
 CP : 0 FOR ORIGINAL CELL, AND 1 FOR COPIED CELL.

FIG. 234



SINCE ERROR CELL IS NOT ENCAPSULATED, NO ERROR FLAG OTHER THAN E2UN AND E2EB IS SET.

F | G. 235

The diagram illustrates the bit-level structure of two SIP-related cells: SIP CON CELL and SIP COM CELL. Each cell is 26 octets long, with bit positions 0 through 25 indicated for each octet.

SIP CON CELL Structure:

- Octet 0:** O (bit 0), 1 (bit 1), SIP PL Length (bits 2-3), INPUT MID (bits 4-5), SIP ID (INPUT VCI) (bits 6-7), SNH ID (INPUT VCI) (bits 8-9), PT (bit 10), CLP (bit 11).
- Octet 1:** HOME MESH (bits 0-1), BC (bit 2), OUTPUT VCI (DESTINATION MH ID) (bits 3-4), PT (bit 5), CLP (bit 6).
- Octet 2:** O (bit 0), SN (bit 1), OUTPUT MID (USED AS RHID IN PROCESS) (bits 2-3).
- Octet 3:** Information (bits 0-3).
- Octet 4:** Information (bits 0-3).
- Octet 5:** Information (bits 0-3).
- Octet 6:** SN (bits 0-3).
- Octet 7:** Information (bits 0-3).
- Octet 8:** Information (bits 0-3).
- Octet 9:** Information (bits 0-3).
- Octet 10:** Information (bits 0-3).
- Octet 11:** Information (bits 0-3).
- Octet 12:** Information (bits 0-3).
- Octet 13:** Information (bits 0-3).
- Octet 14:** Information (bits 0-3).
- Octet 15:** Information (bits 0-3).
- Octet 16:** Information (bits 0-3).
- Octet 17:** Information (bits 0-3).
- Octet 18:** Information (bits 0-3).
- Octet 19:** Information (bits 0-3).
- Octet 20:** Reserve (bits 0-3), SIP Bctag (bits 4-5).
- Octet 21:** SIP length (bits 0-3).
- Octet 22:** SIP length (bits 0-3).
- Octet 23:** SIP length (bits 0-3).
- Octet 24:** SIP length (bits 0-3).
- Octet 25:** PL (bits 0-3), CRC (bits 4-5).

SIP COM CELL Structure:

- Octet 0:** O (bit 0), 1 (bit 1), SIP PL Length (bits 2-3), INPUT MID (bits 4-5), SIP ID (INPUT VCI) (bits 6-7), SNH ID (INPUT VCI) (bits 8-9), PT (bit 10), CLP (bit 11).
- Octet 1:** HOME MESH (bits 0-1), BC (bit 2), OUTPUT VCI (DESTINATION MH ID) (bits 3-4), PT (bit 5), CLP (bit 6).
- Octet 2:** O (bit 0), SN (bit 1), OUTPUT MID (USED AS RHID IN PROCESS) (bits 2-3).
- Octet 3:** Information (bits 0-3).
- Octet 4:** Information (bits 0-3).
- Octet 5:** Information (bits 0-3).
- Octet 6:** SN (bits 0-3).
- Octet 7:** Information (bits 0-3).
- Octet 8:** Information (bits 0-3).
- Octet 9:** Information (bits 0-3).
- Octet 10:** Information (bits 0-3).
- Octet 11:** Information (bits 0-3).
- Octet 12:** Information (bits 0-3).
- Octet 13:** Information (bits 0-3).
- Octet 14:** Information (bits 0-3).
- Octet 15:** Information (bits 0-3).
- Octet 16:** Information (bits 0-3).
- Octet 17:** Information (bits 0-3).
- Octet 18:** Information (bits 0-3).
- Octet 19:** Information (bits 0-3).
- Octet 20:** Reserve (bits 0-3), SIP Bctag (bits 4-5).
- Octet 21:** SIP length (bits 0-3).
- Octet 22:** SIP length (bits 0-3).
- Octet 23:** SIP length (bits 0-3).
- Octet 24:** SIP length (bits 0-3).
- Octet 25:** PL (bits 0-3), CRC (bits 4-5).

FIG. 236

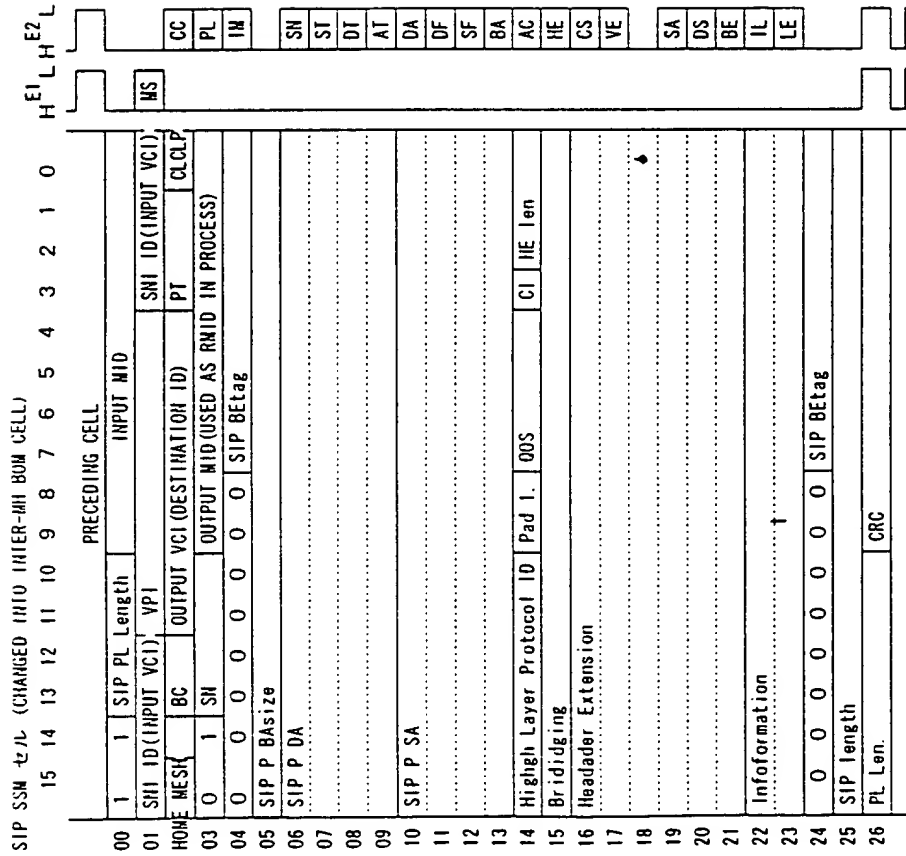


FIG. 237

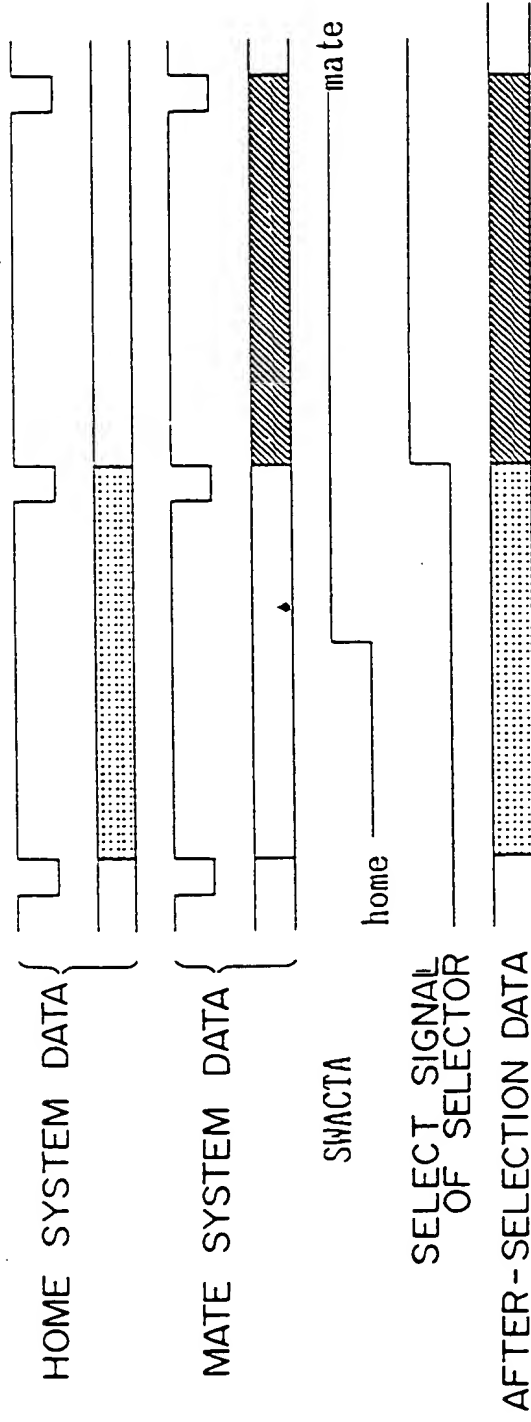


FIG. 238

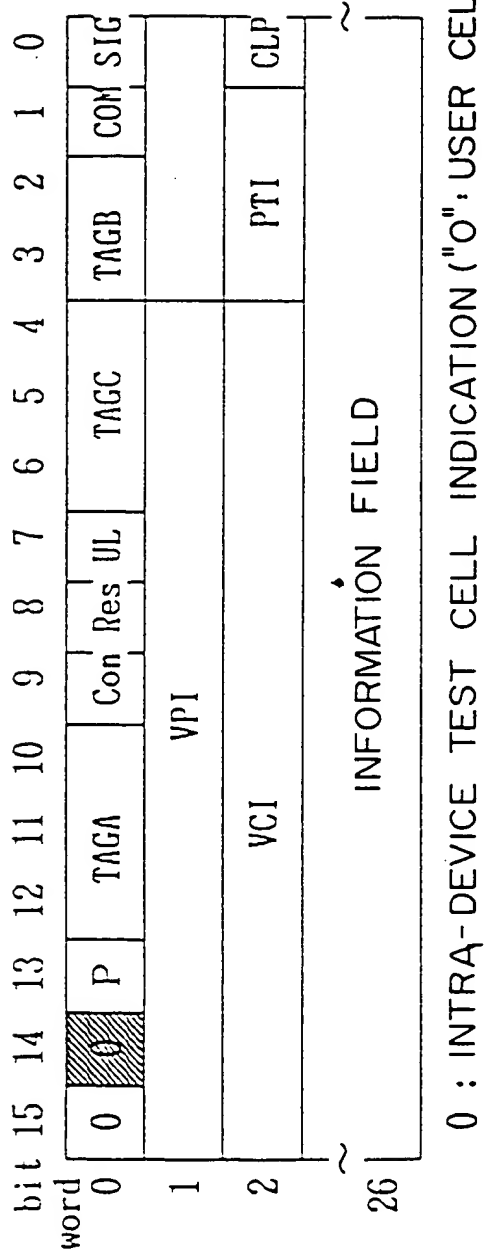


FIG. 239

INPUT			OUTPUT		
LP UNIT STATUS	LINE CELL ENB	TEST CELL ENB	CELL ENB	CELL	TEST CELL FETCH TSOK
IN NORMAL OPERATION	ENB	DSB	ENB	LINE CELL	NG
	ENB	ENB	ENB	LINE CELL	NG
	DSB	ENB	ENB	TEST CELL	OK
	DSB	DSB	DSB	LINE CELL	NG
IN DIAGNOSTICS	DSB BY COMPULSORY MASK	ENB	ENB	TEST CELL	OK
		DSB	DSB	TEST CELL	NG

ENB : ENABLE (ENABLE CELL)
DSB : DISABLE (DISABLE CELL)

FIG. 240

INPUT	OUTPUT
RESIDUAL CELL PAYLOAD	EFCC
0	OFF
OTHER THAN 0	ON

FIG. 241

ST	ERROR CONDITION		
BOM	PL \neq 44 OCTET	————	PL IS NOT MULTIPLE OF 4 OCTETS.
COM	PL \neq 44 OCTET	————	PL IS NOT MULTIPLE OF 4 OCTETS.
EOM	4 OCTET > PL	4 OCTET < PL	PL IS NOT MULTIPLE OF 4 OCTETS.
SSM	28 OCTET > PL	44 OCTET < PL	PL IS NOT MULTIPLE OF 4 OCTETS.

F I G . 2 4 2

66360-012420

INPUT		OUTPUT		
ST	MID CHECK	EF1-MA	EF2-MA	MID CHECK
BOM	not ACT	OFF	OFF	ACT
BOM	ACT	OFF	ON	ACT
COM	ACT	OFF	OFF	ACT
COM	not ACT	ON	OFF	not ACT
EOM	ACT	OFF	OFF	not ACT
EOM	not ACT	OFF	ON	not ACT

*1 : ERROR FLAG(EF2MA) IS SET,
BUT MASTER ERROR FLAG(EF1MS) IS NOT SET.

MID CHECK (PRESENT)

(RAM)
1bit

VCI+MID
(32k)

Act.

NOTE : 32k=32SNI x1k(MID 10bit)
SN CHECK S AND RAM ARE USED IN COMBINATION

FIG. 244

I INPUT			OUTPUT	
ST	CELL SN	SN CHECK	EFSN	SN CHECK
BOM, SSM	SN	D. C.	OFF	SN+1
COM, EOM	SN	SN	OFF	SN+1
COM, EOM	SN	≠SN	ON	SN+1

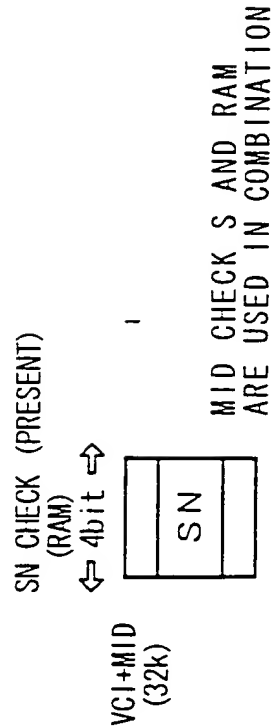


FIG. 245

ST		ERROR CONDITION (ADDRESS TYPE 4BIT)	EFDT	EFST
BOM SSM	DA	VALUE OTHER THAN 1100 OR 1110	ON	OFF
	SA	VALUE OTHER THAN 1100	OFF	ON

FIG. 246

INPUT			OUTPUT
S T	DA CHECK	MATCHING ADDRESS *1	E F S A
BOM, SSM	No Match	D. C.	*2
BOM, SSM	Match	≠SNI#	*3
BOM, SSM	Match	=SNI#	
COM, EOM	D. C.	D. C.	ACT

*1 : MATCHING ADDRESS MSB 4bit
*2 : ROUTE RETRIEVAL IS REQUIRED IN ROUTING UNIT
*3 : ROUTE RETRIEVAL IS REQUIRED IN ROUTING UNIT

DA CHECK (PRESENT)

(CAMLSI)

⇐ 64bit ⇒

SNI#+ADD#
(256)

DA

NOTE : 512 = 32SNI × 8ADDRESS/SNI

FIG. 247

669660-672260

ST	ERROR CONDITION
BOM, SSM	BASIZE<320CTETS, BASIZE >92224CTETS

FIG. 248

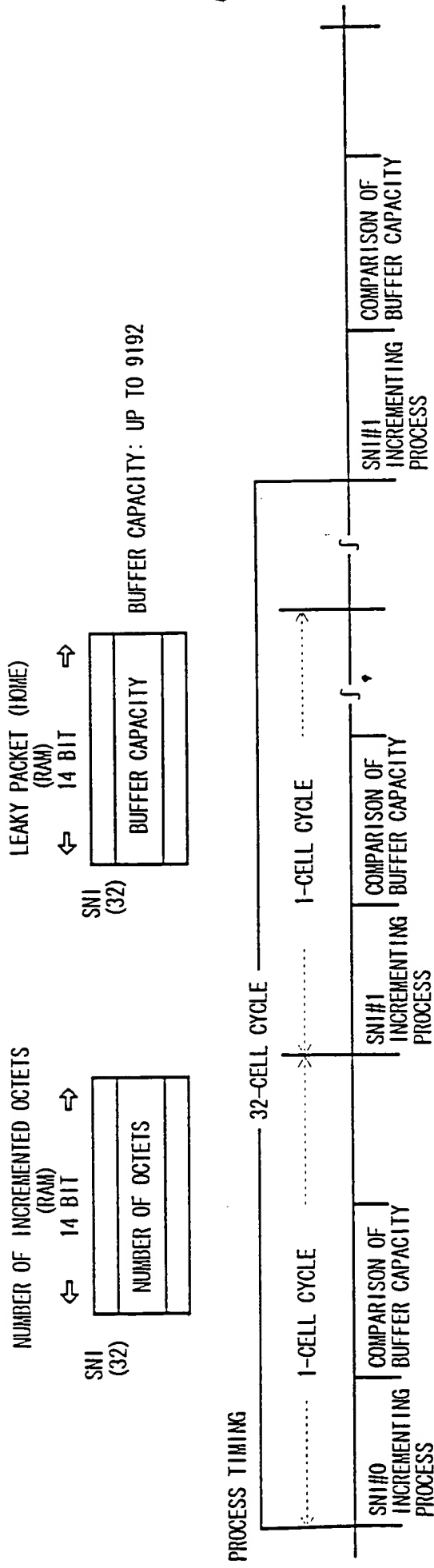


FIG. 249

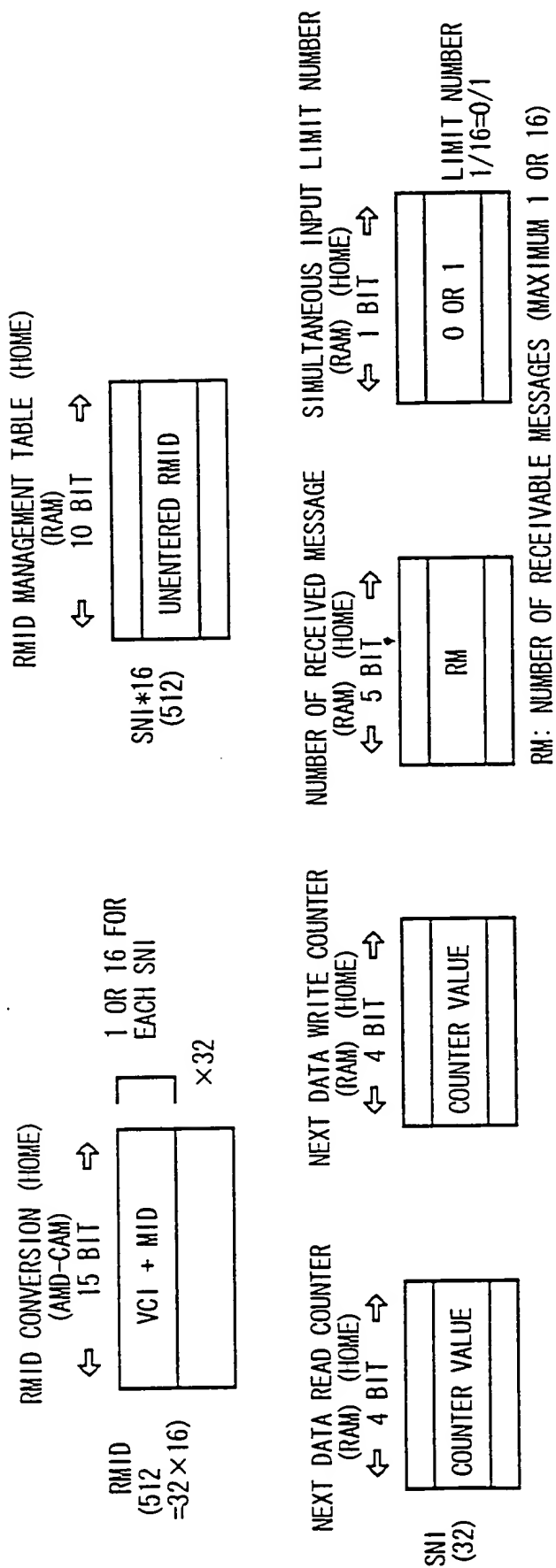


FIG. 250

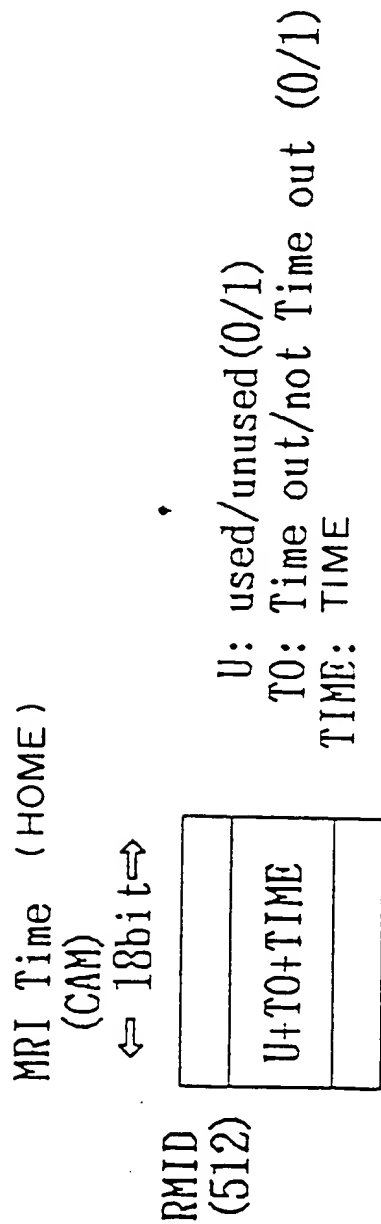


FIG. 251

READ AND WRITE DATA TO RMID CONVERSION CAM AND MRI CAM

INPUT	CAM TYPE	RMID CONVERSION		MRMR I		OUTPUT ERROR FLAG	RMID CONVERSION		MRI
		MATCHING DATA	RESULT	MATCHING DATA	RESULT		WRITE DATA	WRITE DATA	
FOR EACH CELL FRAME (FOR IDLE CELL)				0+1+PRESENT TIME	MATCHING	EFMT+1	ALL 1	ALL 1	ALL 1
FOR EACH CELL FRAME (FOR BOM, COM, EOM, AND SSM)				0+1+PRESENT TIME	MATCHING	—	—	—	0+1+TO TIME
FOR EACH CELL FRAME (FOR ALL CELLS)				0+1+PRESENT TIME	NON-MATCHING	—	—	—	—
IDLE CELL (WHEN MRI MATCHING FOR CELL FRAME)				NO MATCHING OPERATION		REFER TO ABOVE LISTED "FOR CELL FRAME (FOR IDLE CELL)"			
IDLE CELL (WHEN MRI NON-MATCHING FOR CELL FRAME)				1+0+ ALL 1	MATCHING	EFMT+1	ALL 1	ALL 1	ALL 1
IDLE CELL (WHEN MRI NON-MATCHING FOR CELL FRAME)				1+0+ ALL 1	NON-MATCHING	—	—	—	—
FOR EACH CELL FRAME +) BOM						—	VCI+MID	—	0+1+TO TIME
FOR EACH CELL FRAME +) COM		VCI+MID	MATCHING			—	—	—	—
FOR EACH CELL FRAME +) COM		VCI+MID	NON-MATCHING			EIRM	—	—	—
FOR EACH CELL FRAME +) EOM		VCI+MID	MATCHING			—	ALL 1	ALL 1	ALL 1
FOR EACH CELL FRAME +) EOM		VCI+MID	NON-MATCHING			EIRM	—	—	—
SSM	1	D. C.							

* 1 : EOM (TIME OUT) CELL GENERATION

FIG. 252

66920-27220



FIG. 255

TABLE RMID RMID ACQUISITION UNIT, SIMULTANEOUS INPUT LIMIT, MRI T.O. SET/RELEASE PROCESS

INPUT			RMID ACQUISITION CHECK	SIMULTANEOUS INPUT LIMIT CHECK	OUTPUT			RMID	MRI T.O.	RECEIVED CELL NUMBER	READ POIN- TER	WRITE POIN- TER	REMARKS
CELL	MS	RM			MS	RM	EM						
SSM	x	x	ACQUIRED	—	x	x	x	IMPOSSIBLE	—	—	—	—	RELEASING RMID
			NOT-ACQUIRED	OK	x	x	x	NEW RMID	—	—	+1	+1	
				NG	o	o	o	ALL 1	—	—	—	—	
	o	x	ACQUIRED	—	o	x	x	IMPOSSIBLE	—	—	—	—	
			NOT-ACQUIRED	—		o	x	ALL 1	—	—	—	—	
	o	o	—	—	o	o	x	ALL 1	—	—	—	—	
BOM	x	x	ACQUIRED	—	x	x	x	ACQUIRED RMID	RESETTING	—	—	—	
			NOT-ACQUIRED	OK	x	x	x	NEW RMID	SETTING	+1	+1	—	
				NG	o	o	o	ALL 1	—	—	—	—	
	o	x	ACQUIRED	—	o	x	x	ACQUIRED RMID	CLEAR	-1	—	+1	RELEASING RMID
			NOT-ACQUIRED	—		o	x	ALL 1	—	—	—	—	
	o	o	—	—	o	o	x	ALL 1	—	—	—	—	
COM	x	x	ACQUIRED	—	x	x	x	ACQUIRED RMID	—	—	—	—	
			NOT-ACQUIRED	—	o	o	x	ALL 1	—	—	—	—	
	o	x	ACQUIRED	—	o	x	x	ACQUIRED RMID	CLEAR	-1	—	+1	RELEASING RMID
			NOT-ACQUIRED	—		o	x	ALL 1	—	—	—	—	
	o	o	—	—	o	o	x	ALL 1	—	—	—	—	
EOM	x	x	ACQUIRED	—	x	x	x	ACQUIRED RMID	CLEAR	-1	—	+1	RELEASING RMID
			NOT-ACQUIRED	—	o	o	x	ALL 1	—	—	—	—	
	o	x	ACQUIRED	—	o	x	x	ACQUIRED RMID	CLEAR	-1	—	+1	RELEASING RMID
			NOT-ACQUIRED	—		o	x	ALL 1	—	—	—	—	
	o	o	—	—	o	o	x	ALL 1	—	—	—	—	
T.O.	—	—	ACQUIRED	—	o	x	x	ACQUIRED RMID	CLEAR	-1	—	+1	RELEASING RMID
PVC	—	—	—	—	x	x	x	INPUT MID	—	—	—	—	NO ACTION

o : ERROR ON.

x : ERROR OFF.

— : NO OBJECT OF PROCESS

FIG. 256

INPUT			OUTPUT
ST	SA CHECK	MATCHING ADDRESS *1	EF SA
BOM, SSM	No	D. C.	ON
COM, EOM	Match	≠SNI#	ON
COM, EOM	Match	=SNI#	OFF
COM, EOM	D. C.	D. C.	OFF

*1 : MATCHING ADDRESS MSB 4 bit

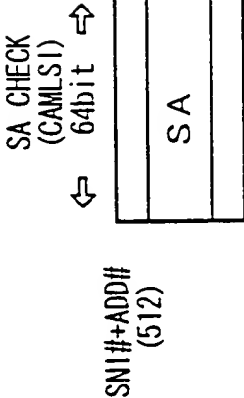


FIG. 258

INPUT				OUTPUT	
ST(SIP)	BEtag (H)	BEtag CHECK	BEtag (T)	EFBE	BEtag CHECK
BOM	BEtag H	D. C.	D. C.	OFF	BE tag H
COM	D. C.	D. C.	D. C.	OFF	—
EOM	D. C.	BEtag	= BEtag	OFF	D. C.
EOM	D. C.	BEtag	≠ BEtag	ON	D. C.
SSM	BEtag H	D. C.	= BEtagH	OFF	D. C.
SSM	BEtag H	D. C.	≠ BEtagH	ON	D. C.

H : Header
T : Trailer

BE tag MATCH (HOME)
(RAM)

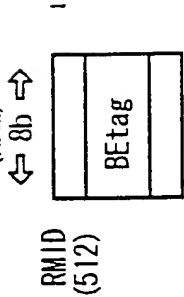


FIG. 260

I N P U T				O U T P U T	
ST (SIP)	BASIZE	BASIZE CHECK	LENGTH	EFBE	BASIZE CHECK
BOM	BASIZE	D. C.	D. C.	OFF	BASIZE
COM	D. C.	D. C.	D. C.	OFF	—
EOM	D. C.	BASIZE	= LENGTH	OFF	D. C.
EOM	D. C.	BASIZE	≠ LENGTH	ON	D. C.
SSM	BASIZE	D. C.	= LENGTH	OFF	D. C.
SSM	BASIZE	D. C.	≠ LENGTH	ON	D. C.

BASIZE MATCH (HOME)
(RAM)

⇐ 16 BIT ⇨

RMID
(1K)

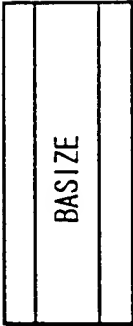
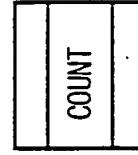


FIG. 261

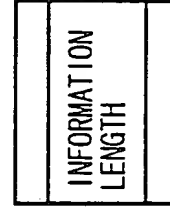
I N P U T						O U T P U T (2)		
ST	BASIZE	PAD LENGTH	CELL COUNT	PL LENGTH	INFORMATION LENGTH PL LENGTH OF EOM	CELL COUNT	EFIL	INFORMATION LENGTH
BOM	BASIZE	PAD	D. C.	D. C.	D. C.	INITIAL VALUE	OFF	PL LENGTH OF EOM
COM	D. C.	D. C.	≠ 0	D. C.	D. C.	DOWN	OFF	—
COM	D. C.	D. C.	= 0	D. C.	D. C.	D. C.	ON	—
EOM	D. C.	D. C.	≠ 0	D. C.	D. C.	D. C.	ON	—
EOM	D. C.	D. C.	= 0	PL	≠ PL	D. C.	ON	D. C.
EOM	D. C.	D. C.	= 0	PL	= PL	D. C.	OFF	D. C.
SSM	BASIZE	PAD	D. C.	PL	≠ PL	D. C.	ON	D. C.
SSM	BASIZE	PAD	D. C.	PL	= PL	D. C.	OFF	D. C.

CELL COUNT (RAM) 8 BIT

RMID (512)



PAYLOAD LENGTH OF EOM (HOME) (RAM) ⇐ 6 BIT ⇒



(≤ 44 OCTET)

FIG. 262

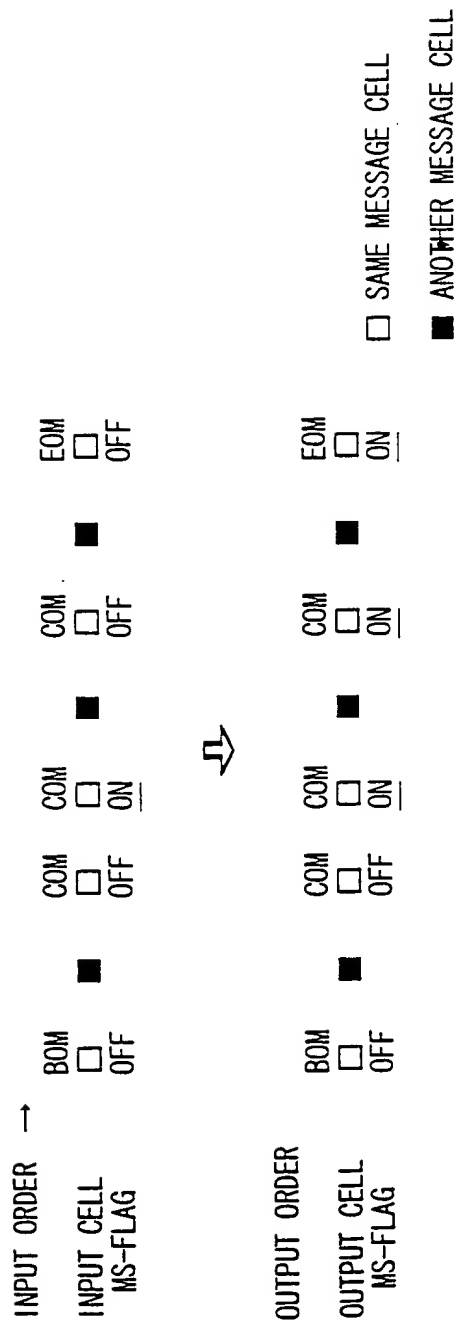
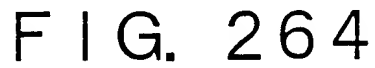


FIG. 263

- [illegible]



○ PROCESS FOR ERRONEOUS MEMORY
ERROR (HOME)
2bit (RAM)

TRIAL BIT+VCI+MID (32k)	MS+DM
----------------------------	-------

MS(Mster) : 1 IF MASTER ERROR FLAG OF CELL IS SET
DM(Discard Message) : IDENTIFIER INDICATING WHETHER
OR NOT EOM HAS ARRIVED (1 AT ARRIVA)

- ERROR MEMORY MATRIX

ITEM	INPUT CELL ST	read data		write data		OUTPUT CELL PROCESS
		MS	DM	MS	DM	
①	BOM (NORMAL CELL)	D.C.	D.C.	0	0	NO (INPUT THROUGH)
②	BOM (ERROR CELL)	D.C.	D.C.	1	0	NO (INPUT THROUGH)
③	COM (NORMAL CELL)	0	0	0	0	NO (INPUT THROUGH)
④	COM (NORMAL CELL)	1	0	1	0	SETTING MASTER ERROR FLAG
⑤	COM (NORMAL CELL)	D.C.	1	1	1	SETTING MASTER ERROR FLAG
⑥	COM (ERROR CELL)	D.C.	0	1	0	NO (INPUT THROUGH)
⑦	COM (ERROR CELL)	D.C.	1	1	1	NO (INPUT THROUGH)
⑧	EOM	0	0	0	1	NO (INPUT THROUGH)
⑨	EOM	1	0	1	1	SETTING MASTER ERROR FLAG
⑩	EOM	D.C.	1	D.C.	11	INVALID CELL

INPUT		OUTPUT (CELL DATA, ETC.)					
ST	ASSIGNING HEADER	IST	STC	SN	MID	PL	CRC
BOM	GENERATING BOM	---	BOM	COPY	COPY	COPY	COPY
	ARRIVAL OF BOM	BOM	COM	---	---	---	---
	COM	COM	COM	---	---	---	---
	EOM	EOM	EOM	---	---	---	---
	GENERATING BOM	---	BOM	COPY	COPY*	COPY	COPY
	ARRIVAL OF SSM	SSM	EOM	---	---	---	---

FIG. 266

○ ISSI HEADER TO BE ASSIGNED TO INTER-MH INF BOM

NAME	INFORMATION LENGTH	LEVEL	ACTION	PROCESS POSITION
RV (RESERVE)	1 cot	L 2	D. C (COPY ARRIVING BOM)	(22) ENCAPSULATION
Btag	1 cot	L 2	D. C (COPY ARRIVING BOM)	(22) ENCAPSULATION
Bsize	2 cot	L 2	D. C (COPY ARRIVING BOM)	(22) ENCAPSULATION
DA (Destination Address)	8 cot	L 3	D. C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
SA (Source Address)	8 cot	L 3	D. C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
D. C	17 cot	L 3	D. C. (COPY ARRIVING BOM)	(22) ENCAPSULATION
IIT	1 cot	L 3	SETTING 01 _H	(23) CARRIER SELECTION
ES (Explicit Selection)	1 cot	L 3	SETTING 0 OR 1	(23) CARRIER SELECTION
Rv (reserve)	7 cot	L 3	SETTING ALL 0	(23) CARRIER SELECTION
C (Carrier)	2 cot	L 3	ASSIGNING CARRIER INFORMATION	(23) CARRIER SELECTION
INID	2 cot	L 3	SETTING ALL 0	(23) CARRIER SELECTION
IITPS	2 cot	L 3	SETTING ALL 0	(23) CARRIER SELECTION

FIG. 267

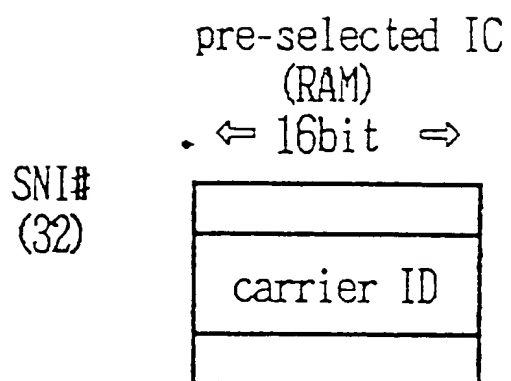


FIG. 269

AT INDICATES GA	CAM MATCHING			DETERMI- NATION	ACTION	BC (BROADCAST IDENTIFIER)		ISSI CARRIER AREA
	INTRA-STATION TABLE	INTRA-STATION NUMBER TABLE	EXTERNAL NUMBER TABLE			MSB	LSB	
○	D. C.	D. C.	D. C.	GA	BROADCAST TO ALL MH	1	1	ASSIGNING CARRIER
×	MATCHING	D. C.	D. C.	INTRA- STATION	ASSIGNING SBMH SPECIFIED VCI	0	0	CLEARING CARRIER
×	NON-MATCHING	MATCHING	NON-MATCHING	INTRA- STATION	BROADCAST TO ALL SBMH	0	1	CLEARING CARRIER
×	NON-MATCHING	NON-MATCHING	MATCHING	EXTERNAL	ASSIGNING GWMH SPECIFIED VCI	0	0	CLEARING CARRIER
×	NON-MATCHING	NON-MATCHING	NON-MATCHING	DETERMINATION IMPOSSIBLE	BROADCAST TO ALL GWMH	1	0	ASSIGNING CARRIER

FIG. 270

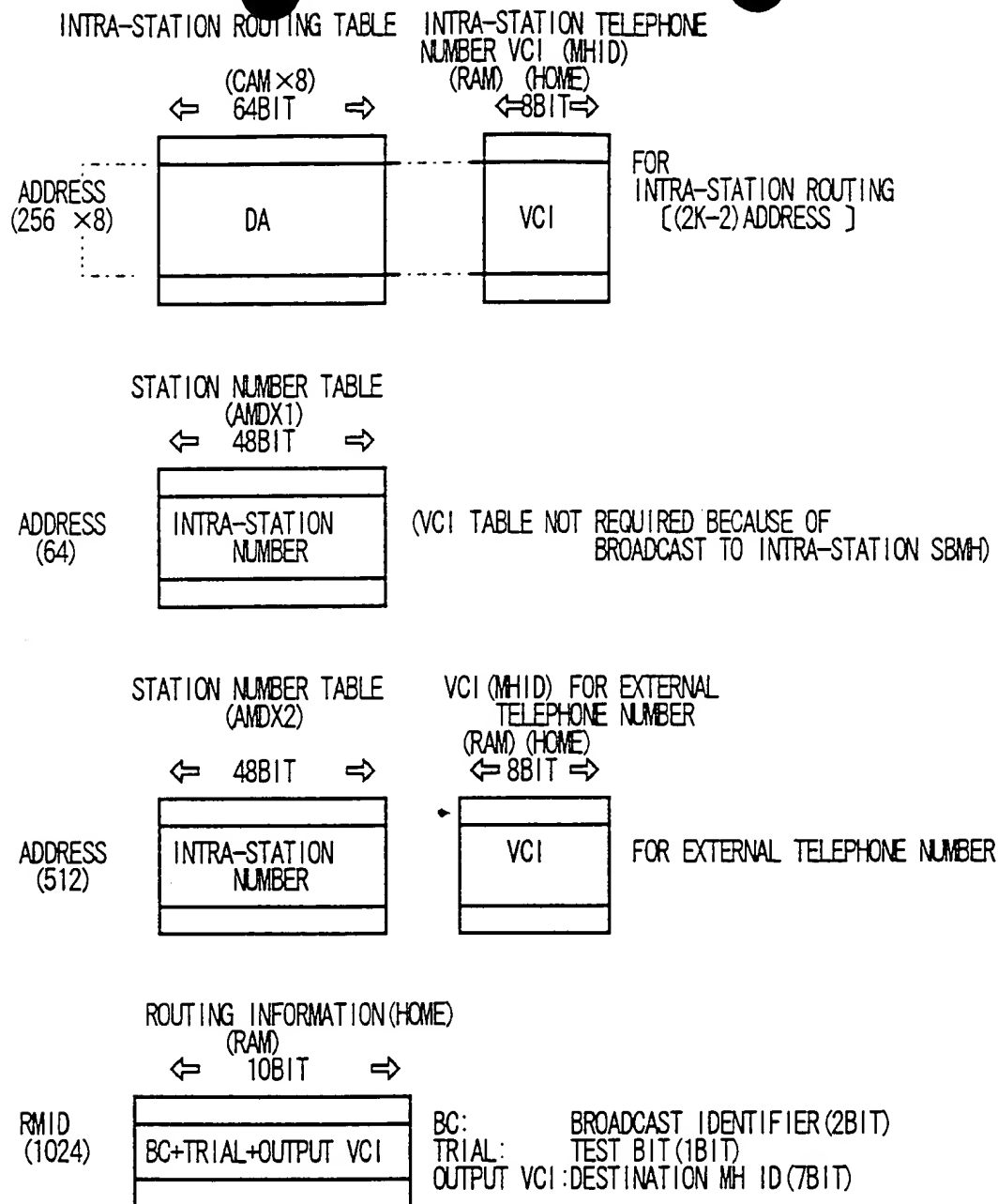


FIG. 271

CARRIER SCREENING
(CAM)
↔ 16bit ↔

CARRIER

SNI#*SCADD#
(512)

NOTE : Ik = (32SNI) x 16

CARRIER AREA STATE

ROUTING METHOD	CARRIER AREA	REMARKS
BROADCAST TO ALL MH	ASSIGNING CARRIER	CELL NOT USING ICI REQUIRES MASKING IN GWMH
ASSIGNING SBMH SPECIFIED VCI	CLEARING CARRIER	MASKING CARRIER AREA WITH 'INTRA-STATION' DETERMINED
BROADCAST TO ALL SBMH	CLEARING CARRIER	MASKING CARRIER AREA WITH 'INTRA-STATION' DETERMINED
ASSIGNING GWMH SPECIFIED VCI	CLEARING CARRIER	MASKING CARRIER AREA WITH 'LATA' DETERMINED
BROADCAST TO GWMH	ASSIGNING CARRIER	CELL NOT USING ICI REQUIRES MASKING IN GWMH

FIG. 272

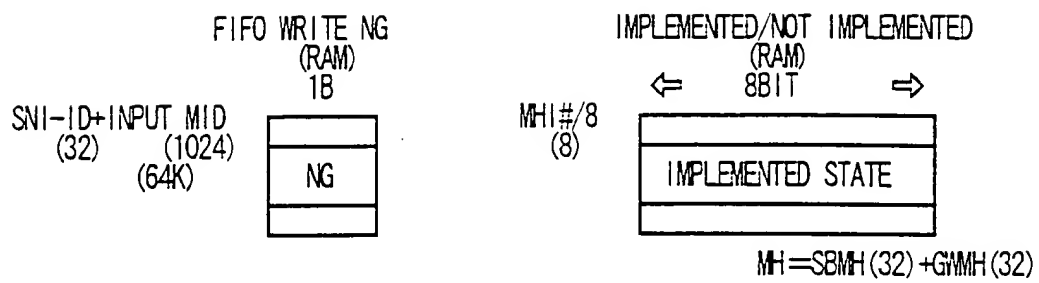
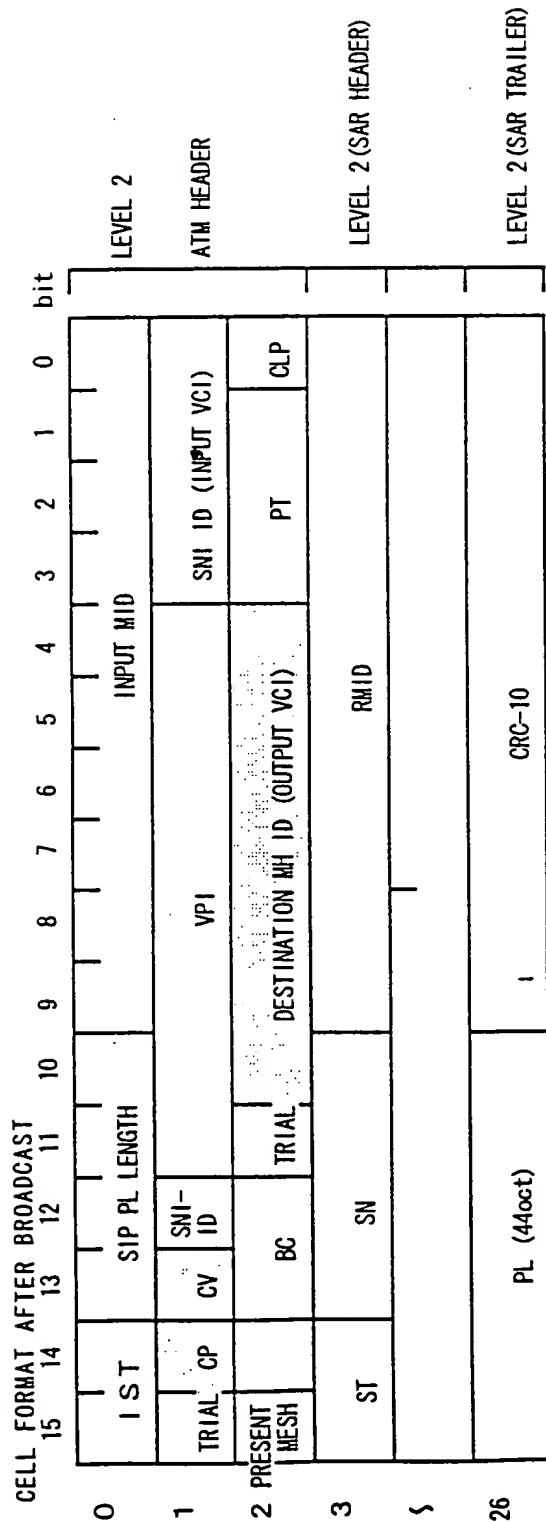


FIG. 274

669360-672260



 : CHANGED PORTIONS IN GA COPY UNIT

FIG. 275

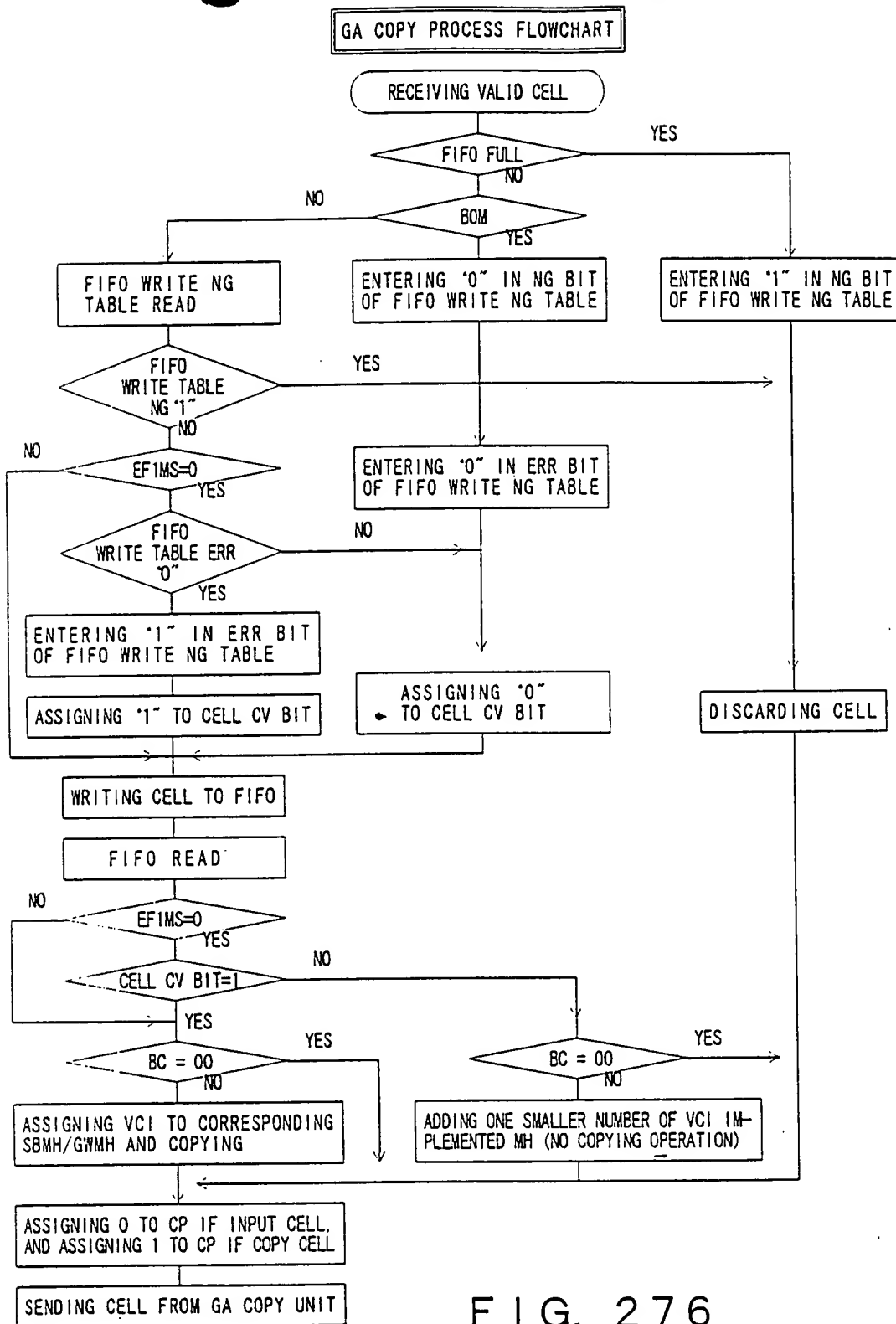


FIG. 276

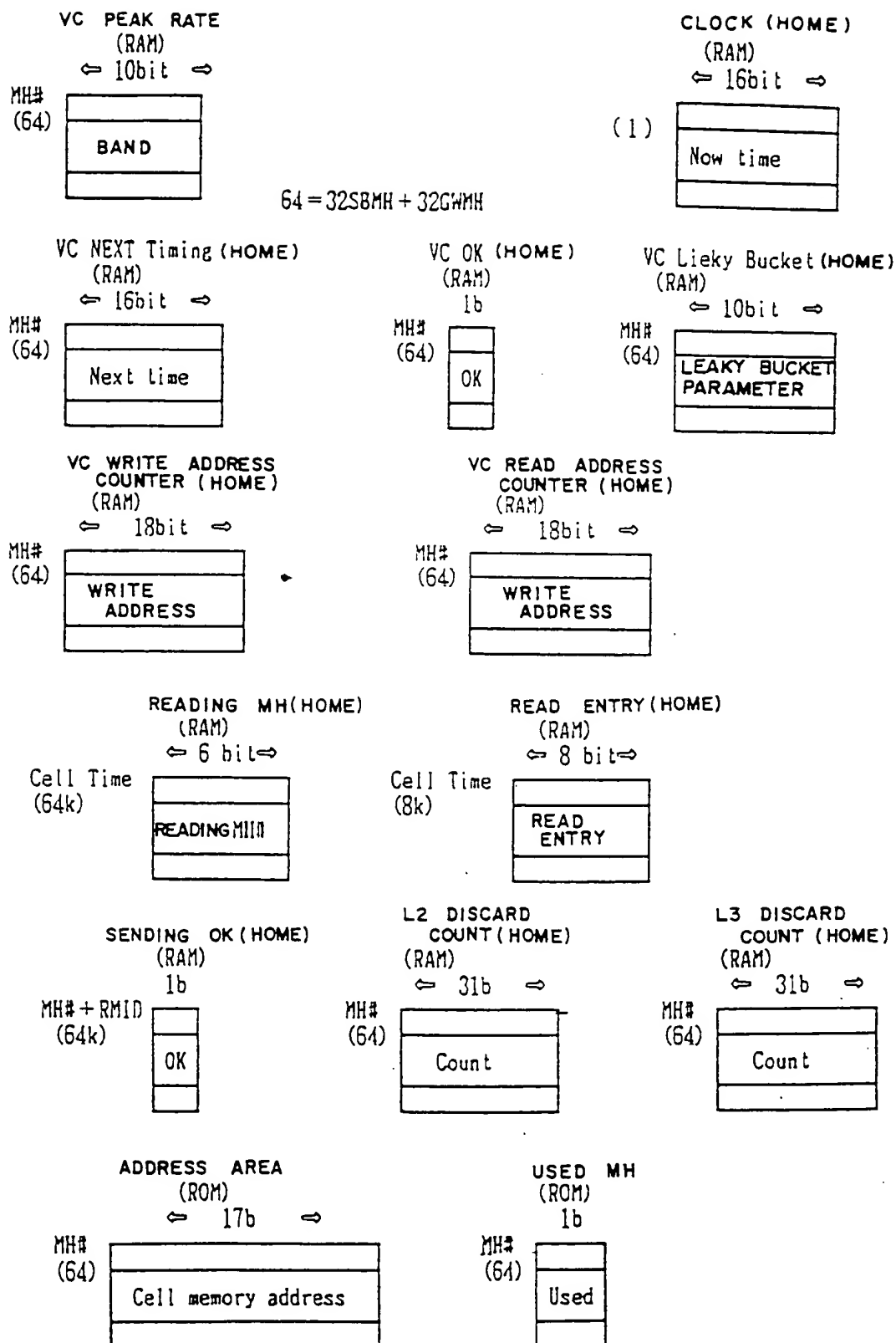


FIG. 277

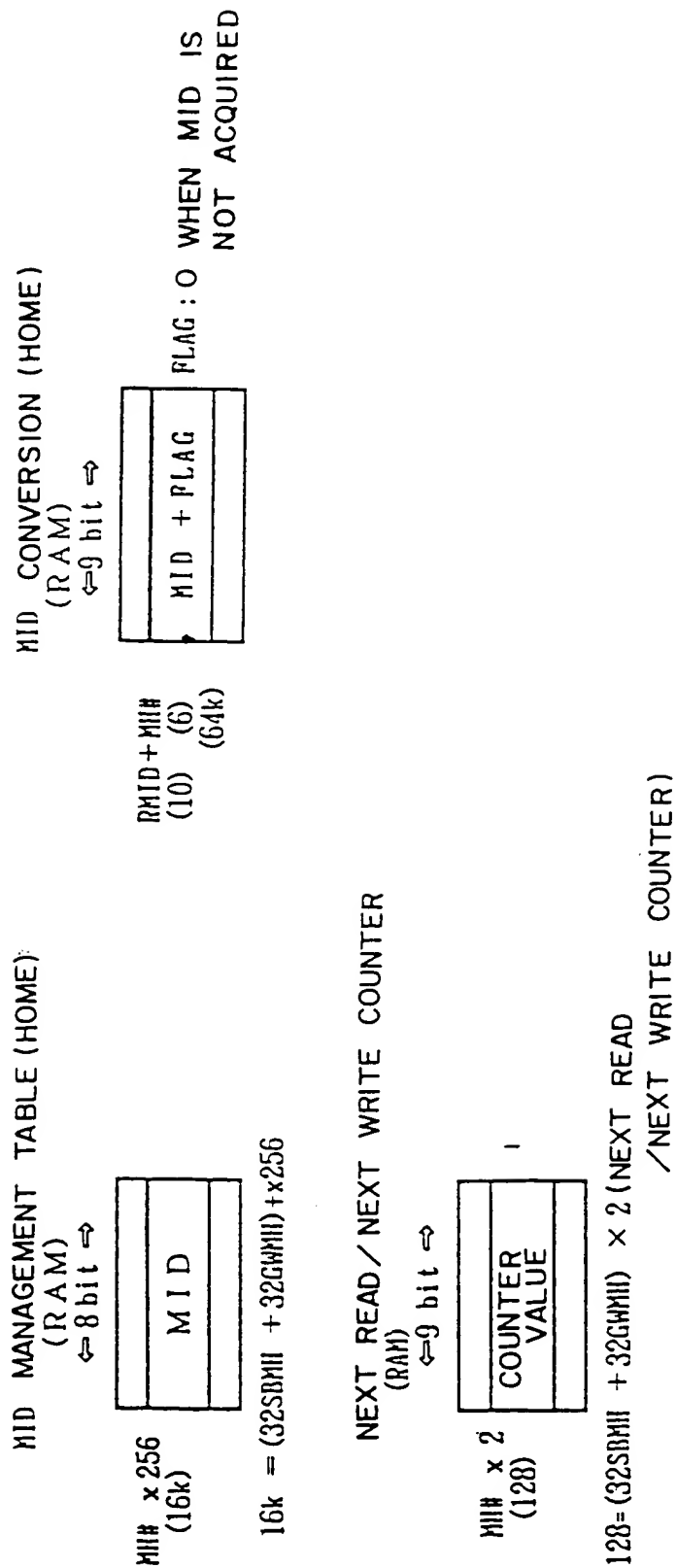


FIG. 278

00000-00000

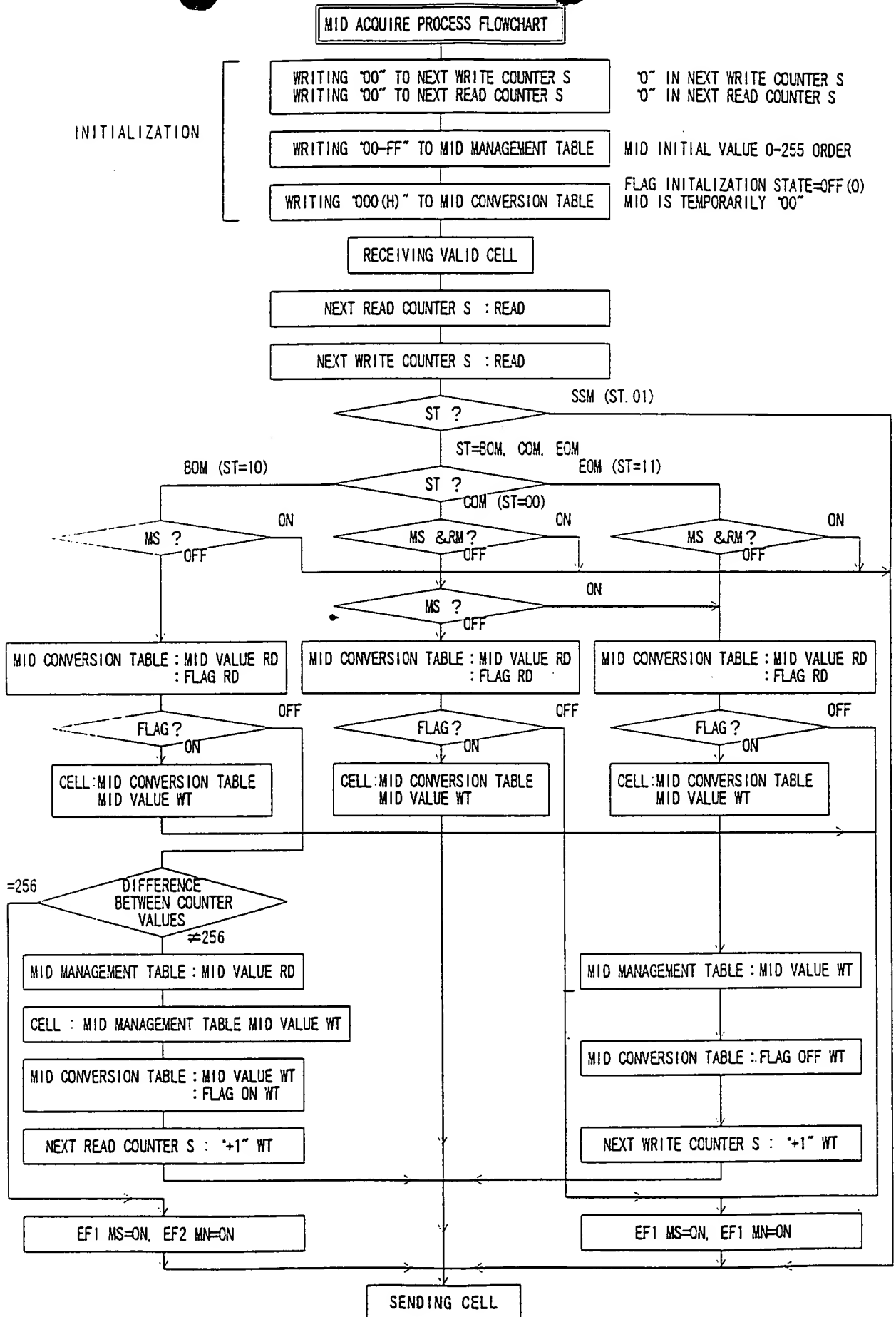


FIG. 279

SMLP TABLE (1/2)

PKG NAME	FUNCTION NAME	TABLE NAME	TYPE	HARDWARE ACCESS	SIZE (ADDRESS X BIT WIDTH)	PKG No	ADDRESS	DATA	REMARKS
1W103A	(9) DA CHECK S	① DA CHECK S	CANLSI	READ	256×64	03	00000 ~ 000FF	00~63	CAN LSI X 1
	(6) MID CHECK S	① MID CHECK S	RAM	READ/WRITE	32K×1		80000 ~ 8FFFF	04	MB81C84A X2 (ODD PARITY)
	(7) SN CHECK S	① SN CHECK S	RAM	READ/WRITE	32K×4			00~03	
	(10) INGRESS FLOW CHECK S	① LEAKY BUCKET S	RAM	READ/WRITE	32×14		90000 ~ 900FF	00~13	MB81C79A X2 (EVEN PARITY)
		② INCREMENTED OCTET NUMBER	RAM	READ	32×14		90020 ~ 9003F		
1W104A	(15) SA CHECK S	① SA CHECK	CANLSI	READ	256×64	04	00000 ~ 000FF	00~63	CAN LSI X 1
	(16) DA SCREENING S	① DS SCREENING	CANLSI	READ	1K×64		00100 ~ 004FF	00~63	CAN LSI X 4
	(12) SIMULTANEOUS INPUT NUMBER CHECK S	① RHID CONVERSION S	ANDCAH	READ/WRITE	512×15		60000 ~ 601FF	00~14	AM99C10A X2
		② HRT TIME S	ANDCAH	READ/WRITE	512×18		60200 ~ 603FF	00~17	AM99C10A X2
		③ SIMULTANEOUS INPUT LIMIT NUMBER	RAM	READ	32×1		80000 ~ 8001F	00	MB81C79A (ODD PARITY)
		④ RHID ASSIGNING MANAGEMENT	RAM	READ/WRITE	512×13		90000 ~ 901FF	00~12	MB81C79A (ODD PARITY)
		⑤ RHID MANAGEMENT S	RAM	READ/WRITE	512×13		90200 ~ 903FF		
	(16) DA SCREENING S	② SC ATTRIBUTE	RAM	READ	32×2		A0000 ~ A001F	00~02	MB81C79A (EVEN PARITY)
	(18) BA SIZE MATCHING CHECK S	① BA SIZE VALUE S	RAM	READ/WRITE	512×16		80000 ~ 801FF	00~15	MB81C79A X2 (EVEN PARITY)
	(19) INFORMATION LENGTH CHECK S	① DOWN CNT VALUE S	RAM	READ/WRITE	512×16		80200 ~ 803FF		
1W105A	(19) BE TAG MATCHING S	② BE TAG MATCHING S	RAM	READ/WRITE	512×16	05	80400 ~ 805FF		
	(25) ROUTING S	① INTRA-STATION ROUTING TABLE S	CANLSI	READ	2K×64		00000 ~ 007FF	00~63	CAN-LSI X8
		② INTRA-STATION NUMBER TABLE S	ANDCAH	READ	64×48		60000 ~ 6003F	00~47	AM99C10A (MAX ADDRESS 256)
		③ EXTERNAL STATION NUMBER TABLE S	ANDCAH	READ	512×48		60100 ~ 602FF	00~47	AM99C10A X2
	(26) CARRIER SCREENING S	① CARRIER SCREENING S	ANDCAH	READ	512×16		60300 ~ 604FF	00~47	AM99C10A X2
	(22) ERROR EDITION IIS	① ERROR & DISCARD MEMORY S	RAM	READ/WRITE	64K×2		80000 ~ 8FFFF	00~01	MB81C79A (EVEN PARITY)
	(24) CARRIER SELECTION S	① CARRIER SELECTION TABLE S	RAM	READ	32×16		90000 ~ 9001F	00~15	MB81C79A X2 (EVEN PARITY)
	(25) ROUTING S	④ INTRA-STATION PHONE NUMBER VC1 S	RAM	READ	2K×8		A0000 ~ A01FF	00~07	MB81C79A (EVEN PARITY)
		⑤ EXTERNAL STATION PHONE NUMBER VC1 S	RAM	READ	512×8		80000 ~ 801FF	00~07	MB81C79A (EVEN PARITY)
		⑦ RATING INFORMATION	RAM	READ/WRITE	512×10		C0000 ~ C01FF	00~09	MB81C79A (EVEN PARITY)
	(26) ENCAPSULATION S	CELL FIFO S	RAM	READ/WRITE	4K×18 (FOR 128CELL)		HWG NO FIRMWARE ACCESS		
		COPY MEMORY S	RAM	READ/WRITE	8K×18 (FOR 1 CELL)				

SMLP TABLE (2/2)

PKG NAME	FUNCTION NAME	TABLE NAME	TYPE	HARDWARE ACCESS	SIZE (ADDRESS × BIT WIDTH)	PKG No	ADDRESS	DATA	REMARKS
1MH06A	(28) OUTPUT BAND LIMIT S	⑥ READ ENTRY S	RAW	READ/WRITE	8k × 8	06	30000 ~ 31FFF	00 ~ 07	MB81C79A (EVEN PARITY)
		① VC WRITE ADDRESS COUNTER S	RAW	READ/WRITE	256 × 18		32000 ~ 320FF	00 ~ 17	VCSH-LSI (EVEN PARITY)
		② VC READ ADDRESS COUNTER S	RAW	READ/WRITE	256 × 18		32100 ~ 321FF	00 ~ 17	VCSH-LSI (EVEN PARITY)
		③ VO PEAK RATE S	RAW	READ	256 × 10		32300 ~ 323FF	00 ~ 09	VCSH-LSI (EVEN PARITY)
		④ VC NEXT TIMING S	RAW	READ/WRITE	256 × 16		32000 ~ 320FF	11 ~ 26	VCSH-LSI (EVEN PARITY)
		⑤ VC OK S	RAW	READ/WRITE	256 × 1			10	
		⑥ VC LIEKY BUCKET S	RAW	READ/WRITE	256 × 10			00 ~ 09	
		⑦ SHAPER CLOCK S	RAW	READ/WRITE	1 × 16		32800	00 ~ 15	VCSH-LSI
		⑩ SHAPER TRANSMISSION OK S	RAW	READ/WRITE	64k × 1		80000 ~ 8FFFF	00	MB81C84A (EVEN PARITY)
		⑪ L2 DISCARD COUNT S	D-RAM	READ/WRITE	4k × 16				IDT7024
		L3 DISCARD COUNT S	D-RAM	READ/WRITE					
		⑫ ENCAP. DISCARD COUNT S	D-RAM	READ/WRITE					
	(27) GA COPY S	CELL MEMORY S	RAW	READ/WRITE	(FOR 28k CELLS)	MSR μ-P DIRECTLY-CONNECTED MEMORY (LOGICAL DUPLEX CONFIGURATION)			
		① FIFO WRITE S	RAW	READ/WRITE	64k × 1		90000 ~ 9FFFF	00	TC5516645 × 3 (VC · SH PARITY CONTROL)
		② IMPLEMENTATION SB. GWH S	RAW	READ	8 × 8		A0000 ~ A0007	00 ~ 07	MB81C84A (ODD PARITY)
		CELL MEMORY S	RAW	READ/WRITE	16k × 18 (FOR 606 CELLS)				MB81C79A (EVEN PARITY)
	(30) MID ACQUISITION S	COPY MEMORY S	RAW	READ/WRITE	8k × 18 (FOR 1 CELL)	MNG NO FIRMWARE ACCESS			IDT7206 × 3 (PARITY ODD/EVEN MIXED)
		① NEXT R & NEXT W COUNTER S	RAW	READ/WRITE	128 × 9		B0000 ~ B007F	00 ~ 08	MB81C79A × 2 (USED IN COMBINATION WITH PARITY OF CELL FIFO S)
		② MID MANAGEMENT TABLE S	RAW	READ/WRITE	16k × 8		C0000 ~ C3FFF	00 ~ 07	TC5516645 (ODD PARITY)
		③ MID CONVERSION TABLE S	RAW	READ/WRITE	32k × 9		D0000 ~ D7FFF	00 ~ 08	TC5516645 (ODD PARITY)

FIG. 281

O : FRONT CABLE
 — : B.W.B.
 — : CONTROL LINE CLOK etc.
 — : DATA HIGHWAY
 □ : BLOCK REQUIRING μ-P INTERFACE
 ◇ : clock SWITCHING POINT

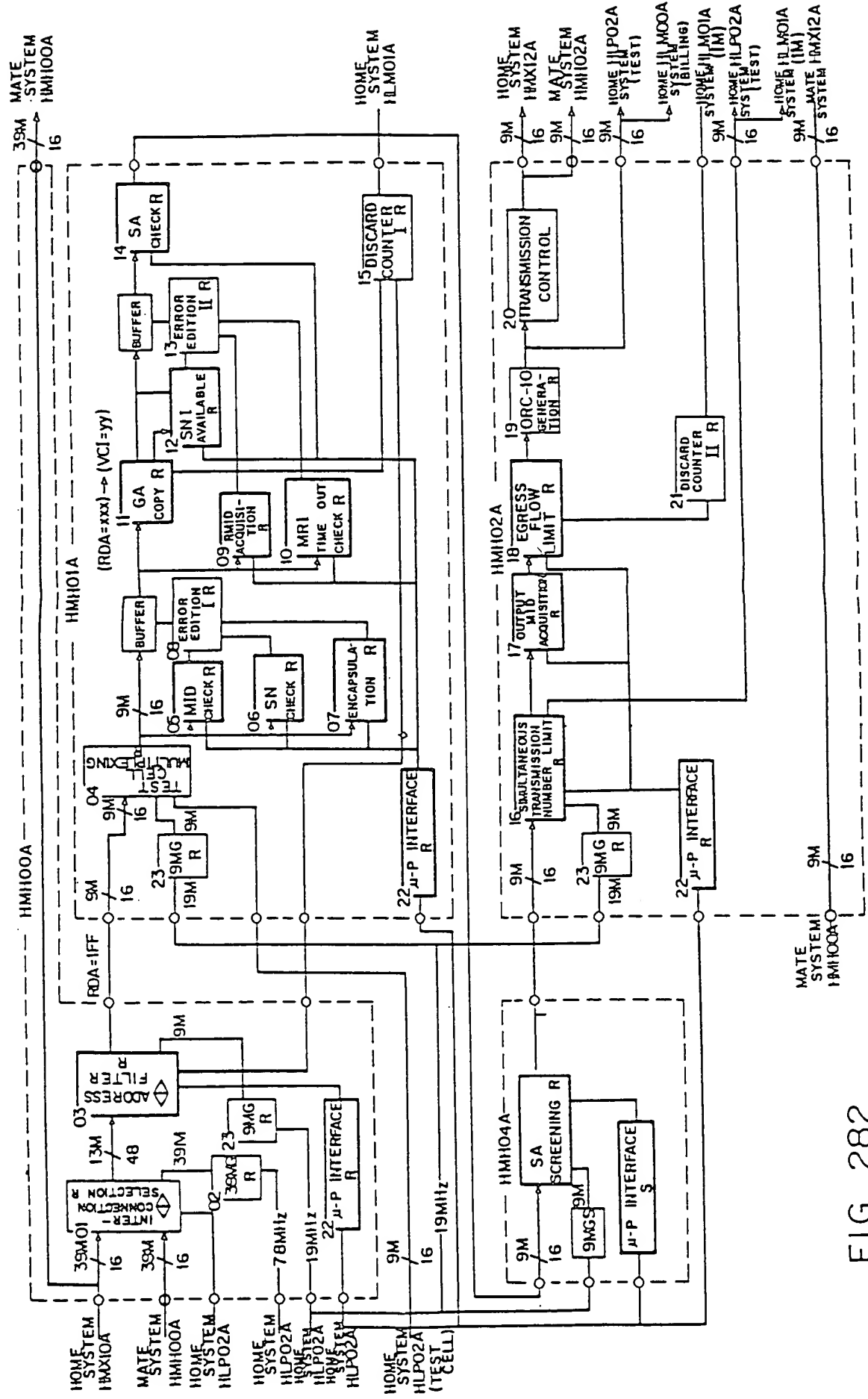


FIG. 282

ITEM	BLOCK NAME	C O N T E N T S () : RELATED ERROR FLAG	PROCESS FOR EACH OBJECT CELL				PWCB
			SUB	SPE	AL	ERR	
0 1	INTER-CONNECTION SELECTION R	SELECTING HDX ACT SYSTEM DATA ACCORDING TO SWITCH SYSTEM INFORMATION.	—	○	○	—	HMH 00A
0 2	39 MHZ R	RECEIVING 78MHZ CLOCK FROM HLPO2A AND GENERATING 39MHZ CLOCK USED IN RMLP UNIT AND CELL FRAME.	—	—	—	—	
0 3	ADDRESS FILTER R	SELECTING CELL TO BE PROCESSED BY RMLP FROM CELLS OF 622H DATA. BUFFERING SELECTED CELLS. AND PASSING THEM TO 150H PROCESSING UNIT. ALSO DISCARDING TCG CELLS.	—	○	○	—	
0 4	TEST CELL MULTIPLEXING R	MULTIPLEXING TEST CELL FOR SNI LOOPBACK TEST INPUT FROM HLPO2A WHEN LINE CONTAINS IDLE CELLS.	○	○	○	—	HMH 01A
0 5	WID CHECK R	CHECKING WHETHER VCI/BID IS NOT ACTIVE AT BOH. AND WHETHER VCI/BID IS ACTIVE AT COH AND EOH. [WS, HA, BC]	×	○	○	—	
0 6	SN CHECK R	INITIALIZING SN AT BOH AND SSH. AND CHECKING ORDER OF SN AT COH AND EOH [WS, SN]	×	○	○	—	
0 7	ENCAPSULATION R	RETRIEVING SIP FROM INTER-WH INF. PDU AND CHANGING ST (SEGMENT TYPE). [WS, SN]	○	○	○	—	
0 8	ERROR EDITION I R	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG. [WS, HA, BC, SN, EN]	○	○	○	○	
0 9	RWID ACQUISITION R	COMPRESSING VCI/BID FOR INTERNAL PROCESS. (VCI:8BIT, BID:10BIT) → (RWID:10BIT) [WS, WN, WD]	○	○	○	○	
1 0	WRI TIME OUT CHECK R	DETERMINING WRI TIMEOUT. (TIMEOUT VALUE: 177HS) TIMEOUT CELL IS TRANSMITTED WHEN TIMEOUT OCCURS. [WS, WT]	○	○	○		
1 1	GA COPY R	COPYING INPUT CELL IN WHICH DA IS INPUT BY GA AND OUTPUTTING IT TO EACH SUBSCRIBER. [WS, GA]	○	○	○	○	
1 2	SNI AVAILABLE R	DISCARDING CELL WHEN SNI INDICATES DT FAULT OR RECEPTION ERROR. [WS, DA]	○	×	○	○	
1 3	ERROR EDITION II R	ALLOCATING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG. [WS, WN, WD, WT, GA, DA]	○	○	○	○	
1 4	SA CHECK R	RETURNING LOOPBACK CELL IN RESPONSE TO GA MESSAGE. [WS, DO]	○	×	○	×	
1 5	DISCARD COUNTER I R	COUNTING DISCARDED CELLS GENERATED IN 600M-155M CONVERSION UNIT AND GA COPY UNIT, AND REPORTING IT TO HLM01A.	○	×	○	×	

SUB : SNI LOOPBACK TEST CELL SPE: INTER-WH PVC TEST CELL (SPECIAL DA) AL : INTER-WH PVC TEST CELL (ALLOCATED DA)
 ERR: ERROR CELL (MASTER ERROR FLAG ON) ○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS
 × : NOT OBJECT OF PROCESS — : NO CELL PASSES OR NO RELATED CELLS

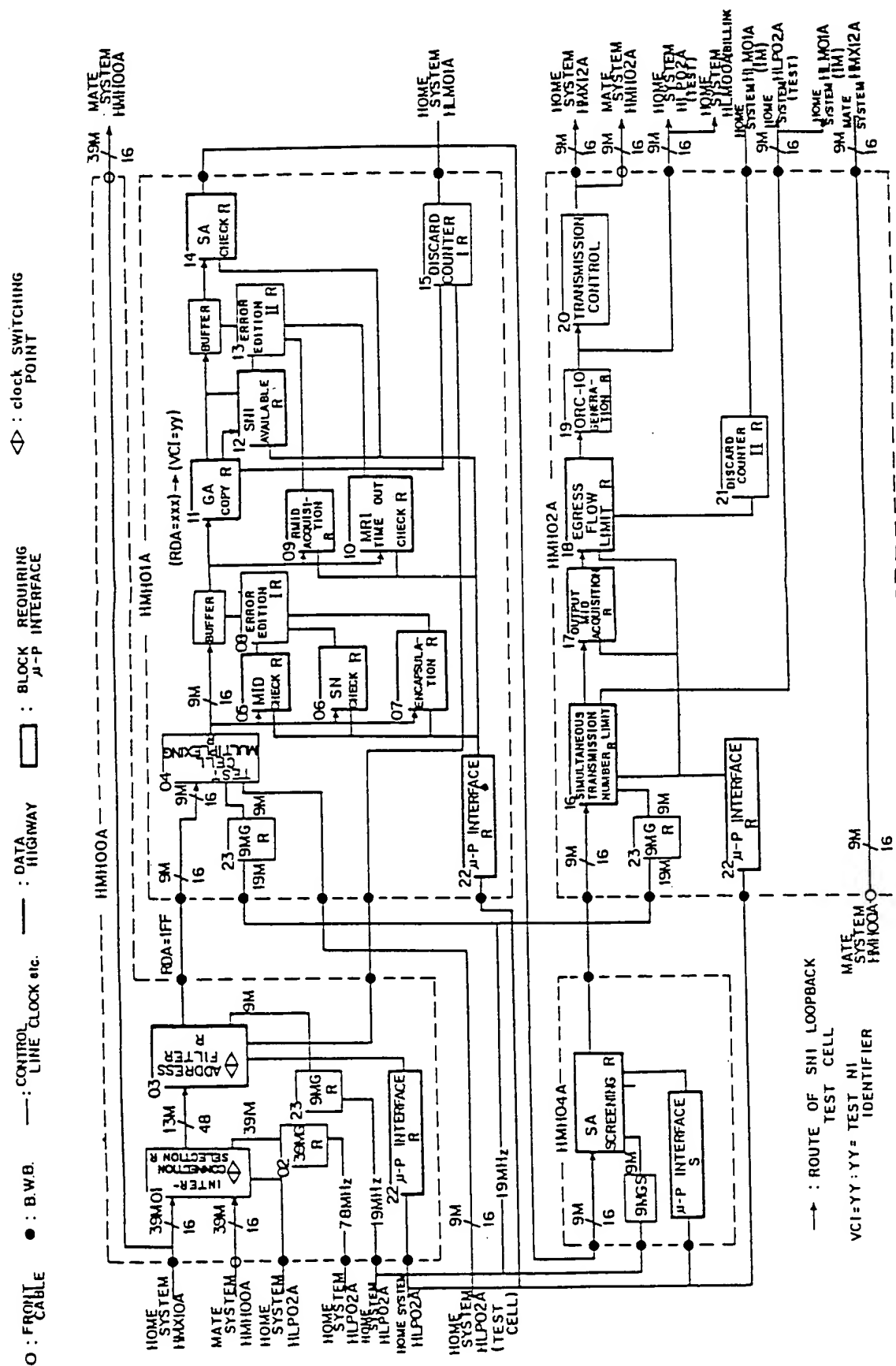
F I G. 2 8 3

ITEM	BLOCK NAME	C O N T E N T S [] : RELATED ERROR FLAG	PROCESS FOR EACH OBJECT CELL				PNCB
			SUB	SPE	ASS	ERR	
--	SA SCREENING R	LIMITING RECEPTION AT DESTINATION SNI. [MS, SS]	○	×	○	○	HMH 04A
1 6	SIMULTANEOUS TRANSMISSION NUMBER LIMIT	LIMITING NUMBER OF MESSAGES FOR EACH SNI. [MS, EM, ED]	○	×	○	○	HMH 02A
1 7	OUTPUT MID ACQUISITION R	CONVERTING FROM EMID (COMPRESSED MID) TO S OUTPUT MID.	○	—	○	—	
1 8	EGRESS FLOW LIMIT	LIMITING OUTPUT BAND (PEAK RATE) FOR EACH SNI.	○	—	○	—	
1 9	CRC-10 GENERATION R	GENERATING AND ASSIGNING CRC-10 OF CELL PAYLOAD.	○	—	○	—	
2 0	TRANSMISSION CONTROL R (DECAPUSLATION)	PREVENTING MHCOM FROM TRANSMITTING ENCAPSULATED BOM.	○	—	○	—	
2 1	DISCARD DOUNTER II R	COUNTING CELLS DISCARDED IN EGRESS FLOW LIMITING UNIT AND REPORTING IT TO HLM01A.	○	—	○	—	COMMON TO EACH PNCB
2 2	μ-P INTERFACE R	INTERFACING WITH MNG μ-P OF HLP02A (ACTUALLY USING SCTL2 LSI).	—	—	—	—	
2 3	9MG R	RECEIVING 10MHZ CLOCK FROM HLP02A AND GENERATING 9MHZ CLOCK TO BE USED IN RMLP.	—	—	—	—	

SUB : SNI LOOPBACK TEST CELL SPE: TEST USING INTER-MH SPECIAL DA ASS: LOOPBACK TEST INTER-MH ASSIGNED DA
ERR: ERROR CELL(MASTER ERROR FLAG ON) ○ : APPLIED FOR PROCESS OBJECT OR DURING PROCESS
× : NOT OBJECT OF PROCESS — : NO CELL PASSES OR NO RELATED CELLS

F I G. 2 8 4

66360" 672260

[illegible]

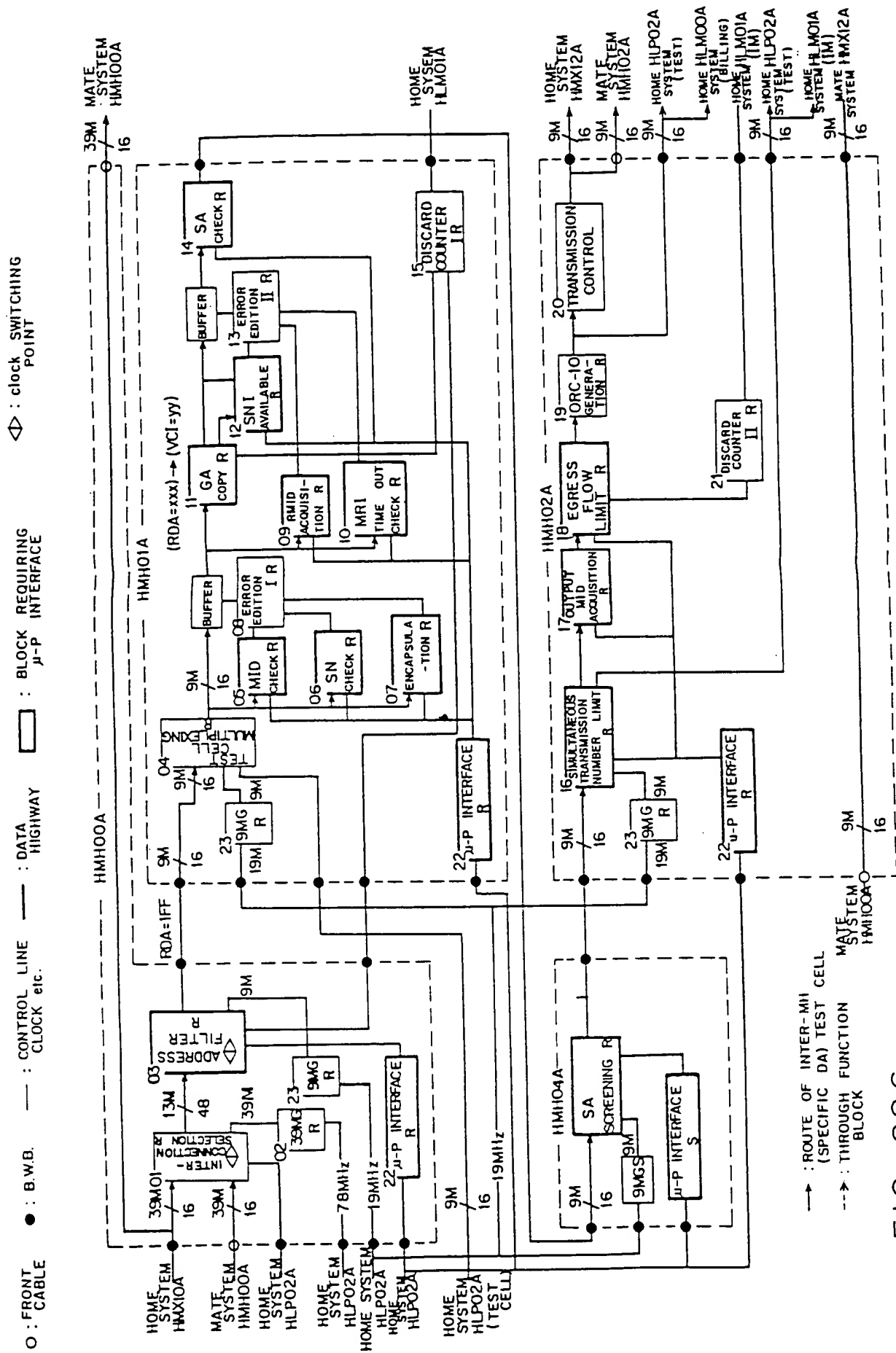


FIG. 286

FRONT
 O : CABLE
 ● : B.W.B.
 — : CONTROL LINE
 — : CLOCK etc.
 ☆ : parity checker
 ★ : parity generator (GENERATING PARITY FOR RAM, BUT OMITTED IN FIGURES)
 □ : DETECTING CLOCK CELL FRAME
 △ : OTHER POINT
 □ : BLOCK REQUIRING μ -P INTERFACE

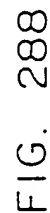


FIG. 289

BLOCK NAME	EF	E1 MS	E2 MA	E1 MC	E2 SN	E2 EN	E2 MN	E1 MD	E2 MT	E1 GA	E2 DA	E2 DO	E2 SS	E2 EM	E1 ED	PVC TEST		
																SUB	SPE	ASS
MID CHECK R (B/S) DM=0		ON	ON	-	-	-	-	-	-	-	-	-	-	-	-	x		
MID CHECK R (B/S) DM=1		-	ON	-	-	-	-	-	-	-	-	-	-	-	-	x		
MID CHECK R (C/E)		ON	-	ON	-	-	-	-	-	-	-	-	-	-	-	x		
SN CHECK R (C/E)		ON	-	-	ON	-	-	-	-	-	-	-	-	-	-	x		
ENCAPSULATION R (ISSIS)		ON	-	-	-	ON	-	-	-	-	-	-	-	-	-			
RMID ACQUISITION R (B/S)		ON	-	-	-	-	ON	-	-	-	-	-	-	-	-			
RMID ACQUISITION R (C/E)		ON	-	-	-	-	-	ON	-	-	-	-	-	-	-			
MRI TIMEOUT CHECK R (TO CELL)		ON	-	-	-	-	-	-	ON	-	-	-	-	-	-			
CELL ARRIVING AFTER TIMEOUT (C/E)		ON	-	-	-	-	-	ON	-	-	-	-	-	-	-			
GA COPY R		ON	-	-	-	-	-	-	-	ON	-	-	-	-	-			
IF IBOM ARRIVES BEFORE IEOM, MS AND GA IS SET ON (COPYING FOR RDA AFTER COPYING FOR RMID) IF MS IS SET ON IN ICOM (EFMD IS ALSO SET ON), CELL IS TRANSMITTED WITH VC1=E0 WHEN CELL WHOSE EIMS IS SET ON IS COPIED, FLAG AT EF2 IS MASKED AND E1GA IS SET ON (TO PREVENT DOUBLE COUNT)																		
SNI AVAILABLE R (B/S)		ON	-	-	-	-	-	-	-	ON	-	-	-	-	-		x	
SA CHECK R (B/S)		ON O	-	-	-	-	-	-	-	-	-	ON	-	-	-		x	
SA SCREENING R (B/S)		ON	-	-	-	-	-	-	-	-	-	-	ON	-	-		x	
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R (B)		ON	-	-	-	-	-	-	-	-	-	-	-	ON	-		x	
SIMULTANEOUS TRANSMISSION NUMBER LIMIT R (C/E)		ON	-	-	-	-	-	O	-	-	-	-	-	-	ON		x	

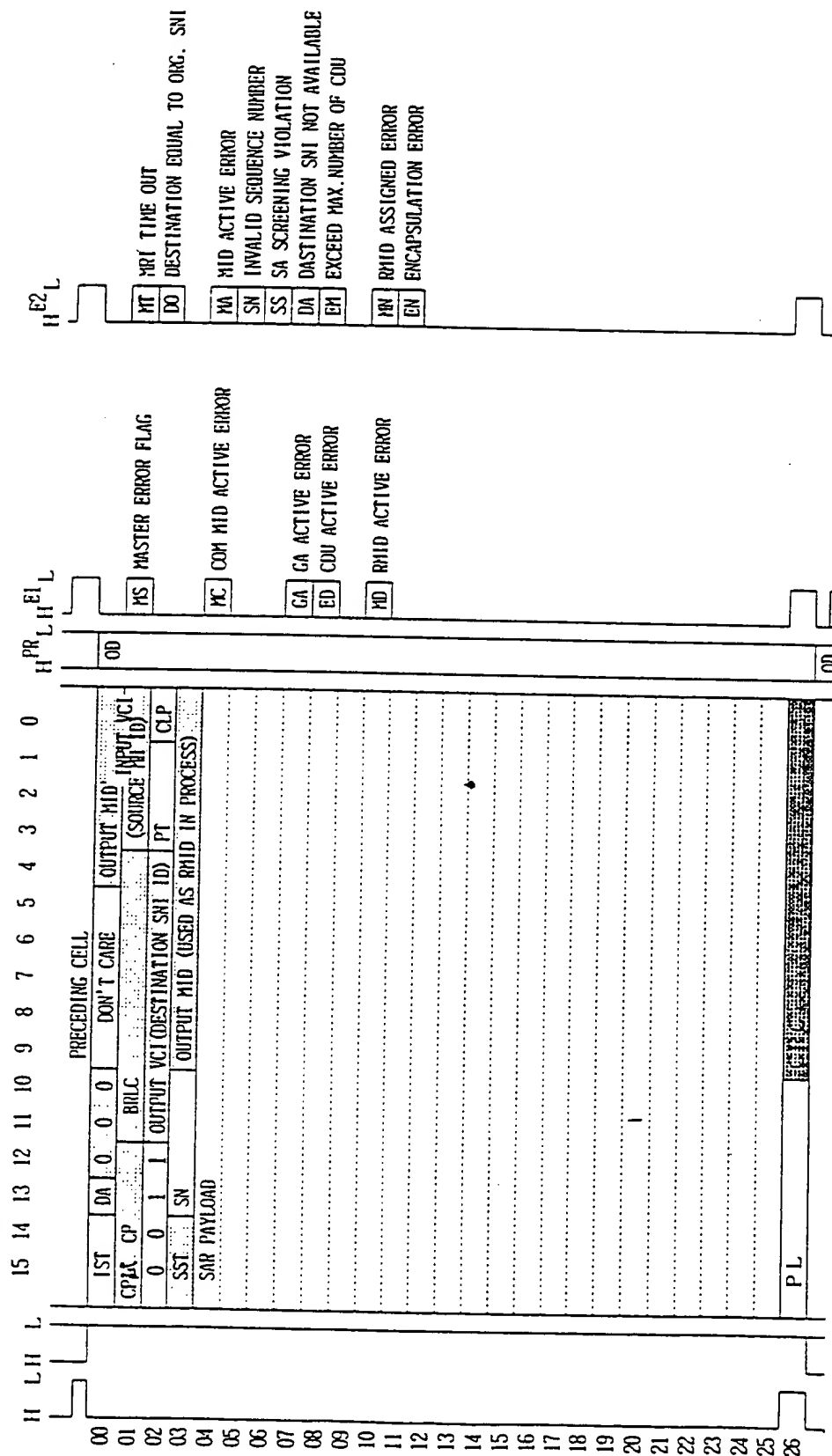
'ON' : EF WHICH IS SET ON WHEN CHECK RESULT
 INDICATES NG.
 'O' : CHECK IS MADE ONLY WHEN EF WITH THIS
 MARK INDICATES OK.
 'SUB' : SUBSCRIBER LOOPBACK TEST
 'ASS' : TEST USING INTER-MH ASSIGNED DA

'-' : CHECK IS MADE REGARDLESS OF OK/NG OF EF
 WITH THIS MARK
 'SPE' : TEST USING INTER-MH SPECIAL DA
 'x' : NO CHECK IS MADE WHEN CELL TESTED IN
 SPECIFIED PVC TEST.

FIG. 290

669260 672260

DESTINATION PROCESSING UNIT, PH UNIT, TH UNIT



AREA CHANGED BY TRANSMISSION TO PH UNIT IN DESTINATION PROCESSING UNIT

AREA CHANGED BY TRANSMISSION TO ACCOUNTING UNIT IN DESTINATION PROCESSING UNIT

ITEM		INTER - MH BOM	SIP BOM	SIP COM	ECM	SIP SSM	INTER - MH SSM
CELL00	IST	10	00	00	01	01	11
CELL03	SST	10	10	10	01	11	11
CELL26	PL	2CH	2CH	2CH	4H-2CH	24H-2CH	—
E101	EFMS	ERRONEOUS OR (ERROR: L)					L
E201	EFMT	(NONE)		L AT MRI TIMEOUT		(NONE)	
E204	EFMA	L WHEN ACTIVE (NOT OBJECT OF EFMS)	(NONE)		L IN NO ACTIVE		L IN ACTIVE STATE (NOT OBJECT OF EFMS)
E104	EFMC	(NONE)	L WHEN NO ACTIVE		(NONE)		
E205	EFMN	NO CHECK	L AT SN ORDER ERROR				NO CHECK
E210	EFMH	L WHEN RMID IS UNAVAILABLE	(NONE)				L WHEN RMID IS UNAVAILABLE
E110	EFMD	(NONE)	L WHEN RMID IS NOT CONVERTIBLE				(NONE)
E211	EFEN	(NONE)					ALL "L"
E106	EFGA	DISCARDED CELL L WHEN RMID ACTIVE	(NONE) *				L WHEN RMID ACTIVE
E207	EFDA	L WHEN DESTINATION SNI IS UNAVAILABLE	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L WHEN DESTINATION SNI IS UNAVAILABLE
E202	EFDO	L AT SELF-LOOPBACK	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L AT SELF-LOOPBACK
E206	EFSS	L AT SCREENING VIOLATION	(STOP AT SIMULTANEOUS TRANSMISSION NUMBER LIMITING MECHANISM)				L AT SCREENING VIOLATION
E208	EFEM	L AT DISCARD UNDER SIMULTANEOUS TRANSMISSION CONTROL	NONE				(NO CHECK)
E108	EFED	(NONE)	L AT STOP UNDER SIMULTANEOUS TRANSMISSION CONTROL				(NONE)

FIG. 292

[illegible]

FIG. 294

INTER MH EOM/SIP EOM CELL

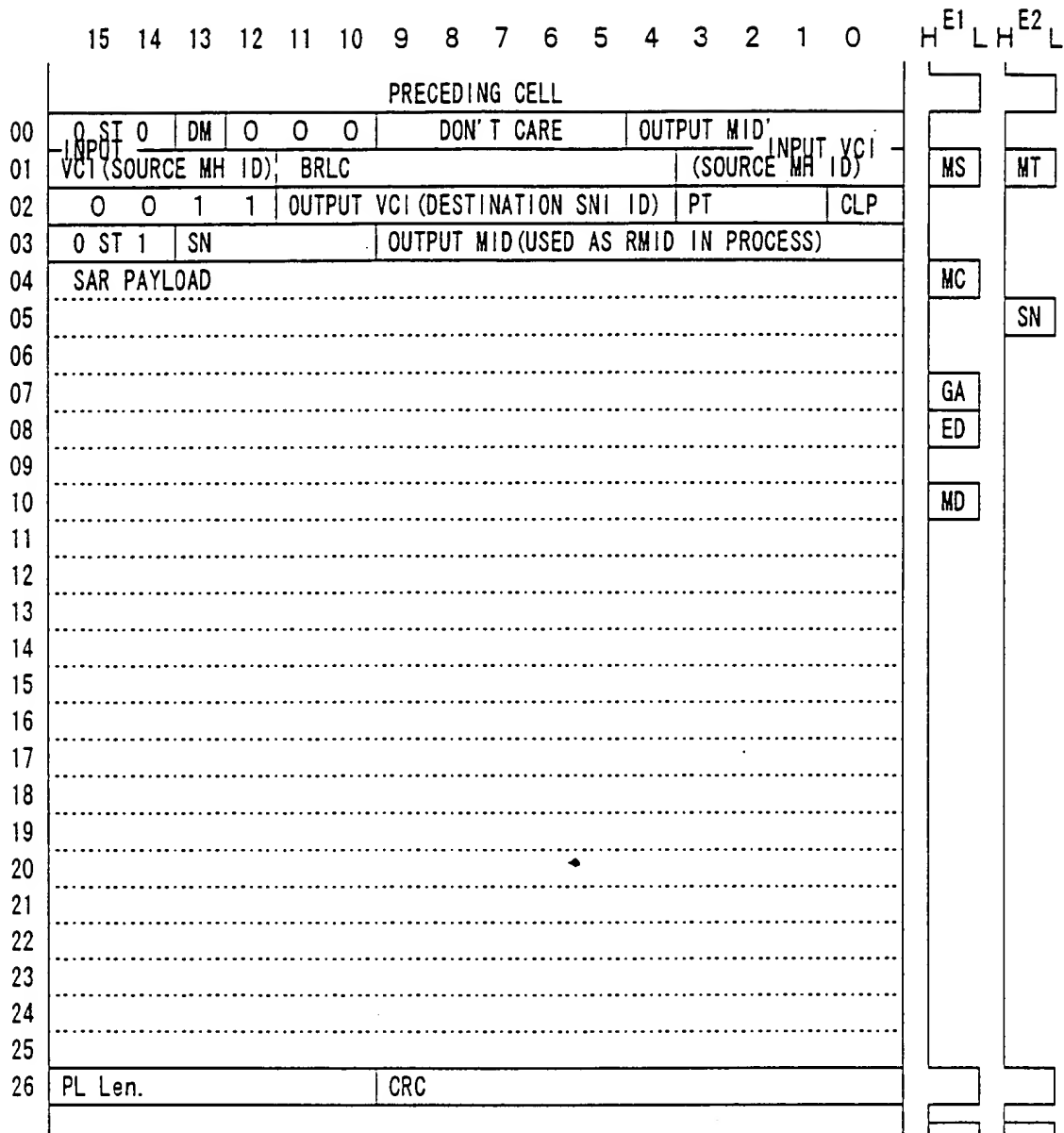
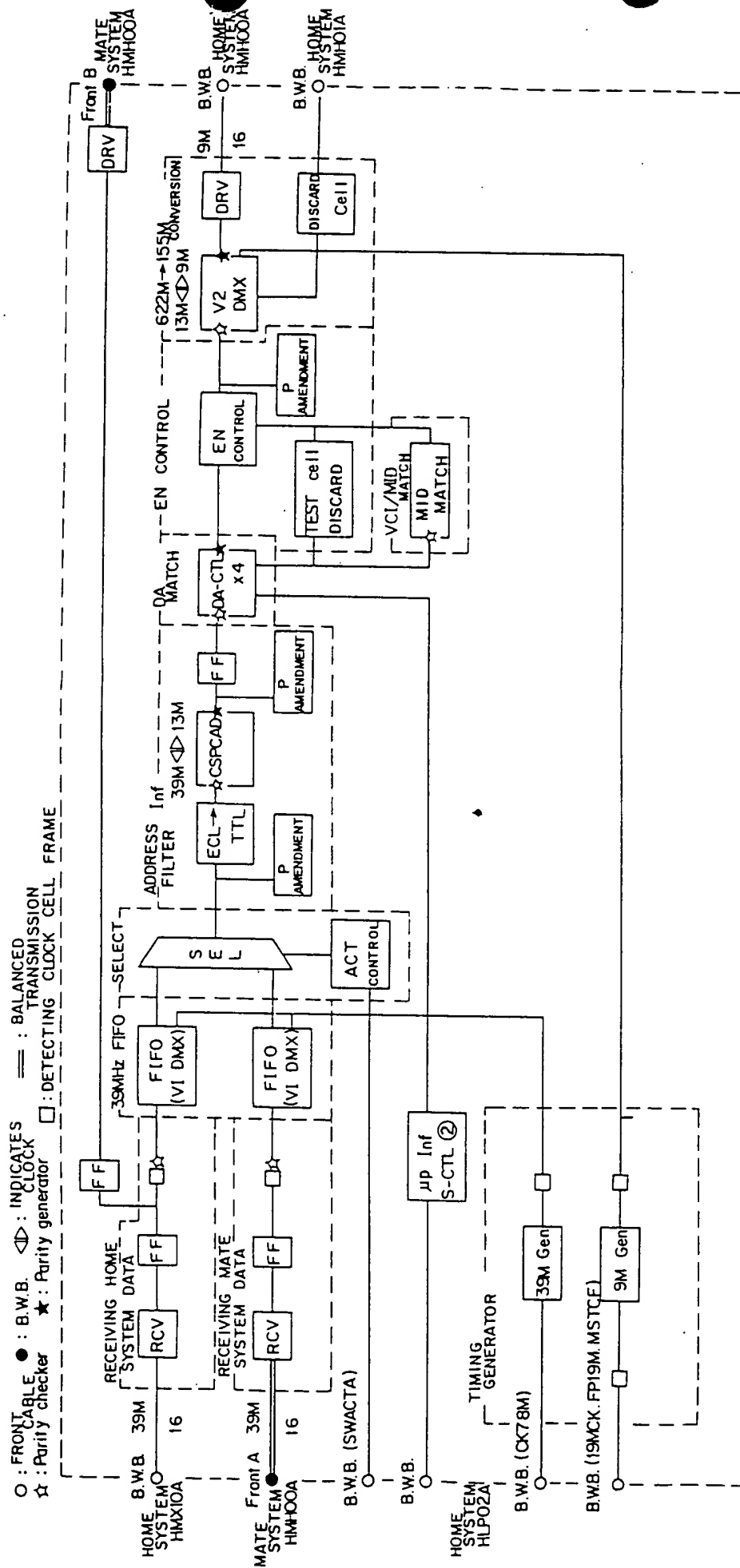


FIG. 295

[illegible]

ITEM	BLOCK NAME	REMARKS
01	CROSS-CONNECTION SELECT R	SELECTING ACTIVE SYSTEM DATA OF MDX ACCORDING TO SWITCH SYSTEM INFORMATION
02	TIMING GENERATOR R	RECEIVING 78MHz CLOCK FROM HLP02A FOR USE IN RMLP. GENERATING 39MHz AND 9MHz CLOCK AND CELL FRAME
03	ADDRESS FILTER R	SELECTING CELL TO BE PROCESSED AT RMLP FROM CELLS IN 622M DATA, AND BUFFERING AND PASSING SELECTED CELL TO 155M PROCESSING UNIT

FIG. 297

- ▼ : POSITION OF TERMINAL RESISTOR
- - : UNBALANCED TRANSMISSION
- : BALANCED TRANSMISSION

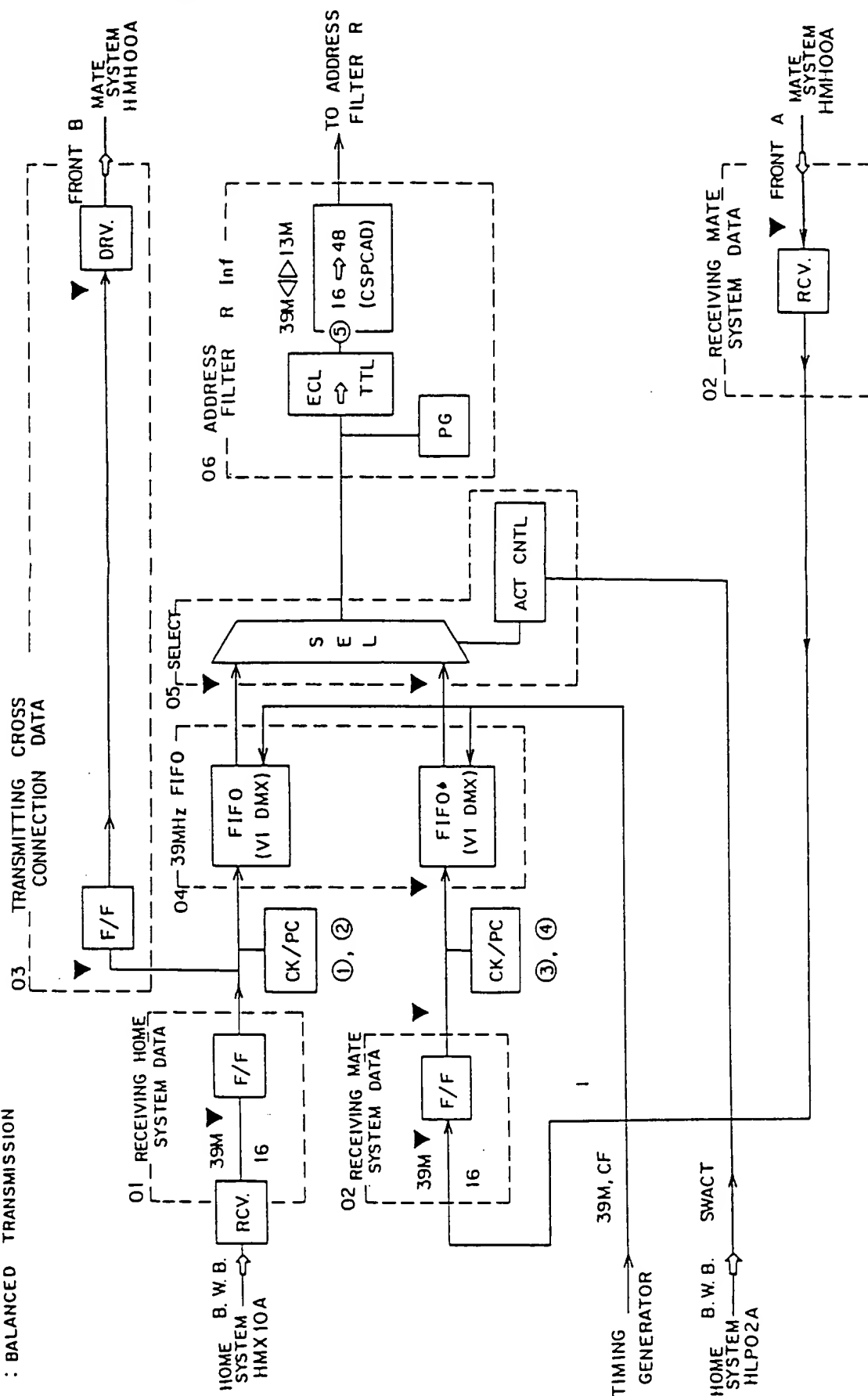


FIG. 298

ITEM	FUNCTION BLOCK NAME	REMARKS
O 1	RECEIVING HOME SYSTEM DATA	RECEIVING 39M16 PARALLEL DATA AS ECL UNBALANCED FROM HOME SYSTEM MHCOM THROUGH B.W.B CHECKING CLOCK, CELL FRAME DISCONNECTION, AND PARITY
O 2	RECEIVING MATE SYSTEM DATA	RECEIVING 39M16 PARALLEL DATA AS ECL BALANCED FROM MATE SYSTEM MHCOM THROUGH FRONT ACONN. CHECKING CLOCK, CELL FRAME DISCONNECTION, AND PARITY.
O 3	TRANSMITTING CROSS-CONNECTION DATA	TRANSMITTING DATA RECEIVED FROM HOME MHCOM THROUGH B.W.B TO HMH00A OF MATE SYSTEM.
O 4	39MHz FIFO	REALLOCATING CLOCK USING V1 DMX LSI. READING DATA RECEIVED BY HOME AND MATE SYSTEMS IN SYNCHRONISM WITH READING CLOCK AND CELL FRAME.
O 5	SELECTING CROSS-CONNECTION DATA	SELECTING DATA RECEIVED FROM MHCOM OF HOME AND MATE SYSTEM ACCORDING TO ACT OF MHCOM. SWITCHING SYSTEMS IN SYNCHRONISM WITH FIFO READ CELL FRAME.
O 6	ADDRESS FILTER R INF	CONVERTING 39M/16 PARALLEL ECL DATA INTO 13M/48 PARALLEL TTL USING C5PCAD LSI TO INTERFACE WITH ADDRESS FILTER R.

FIG. 299

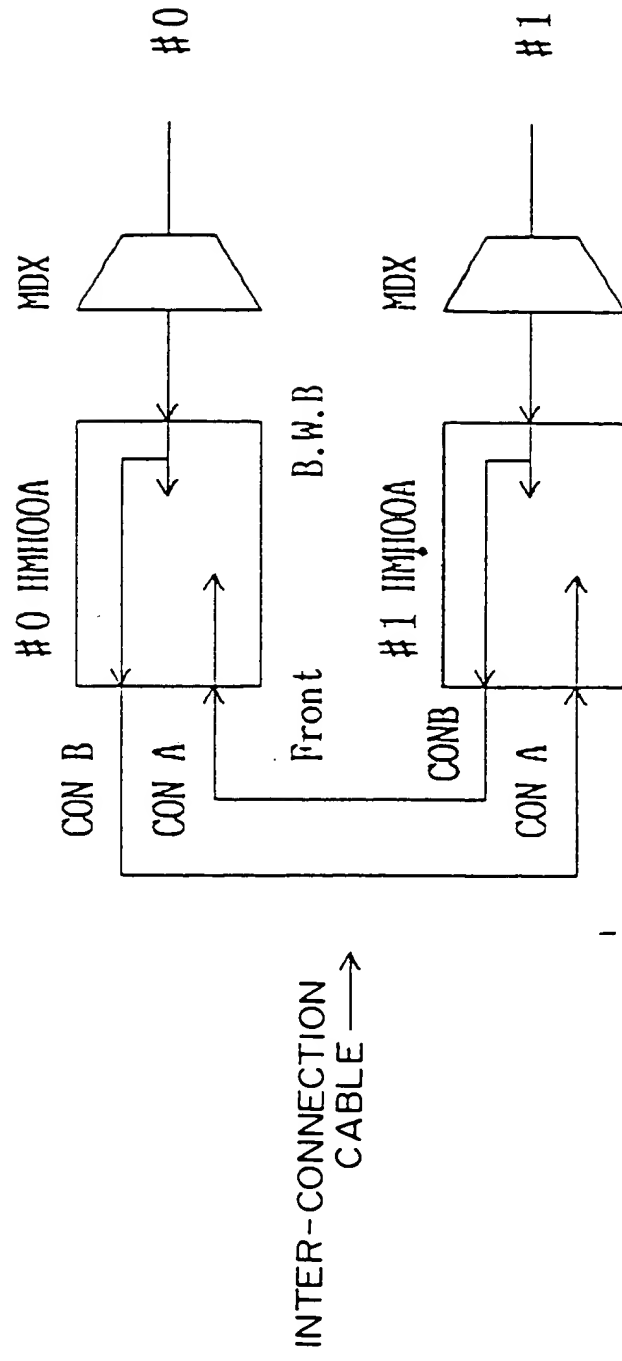


FIG. 300

009220" 6122200

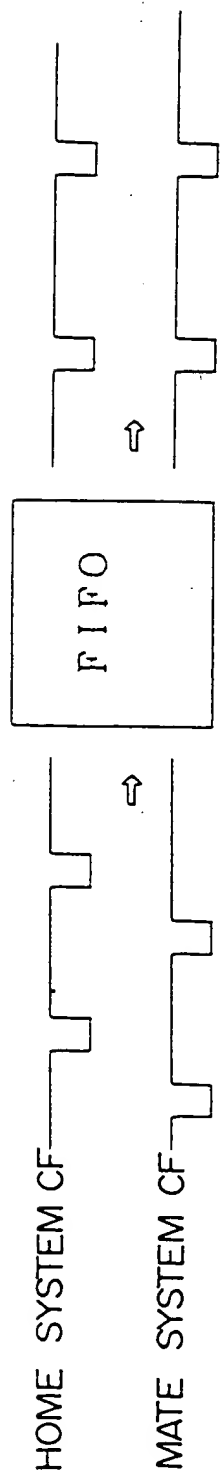


FIG. 301

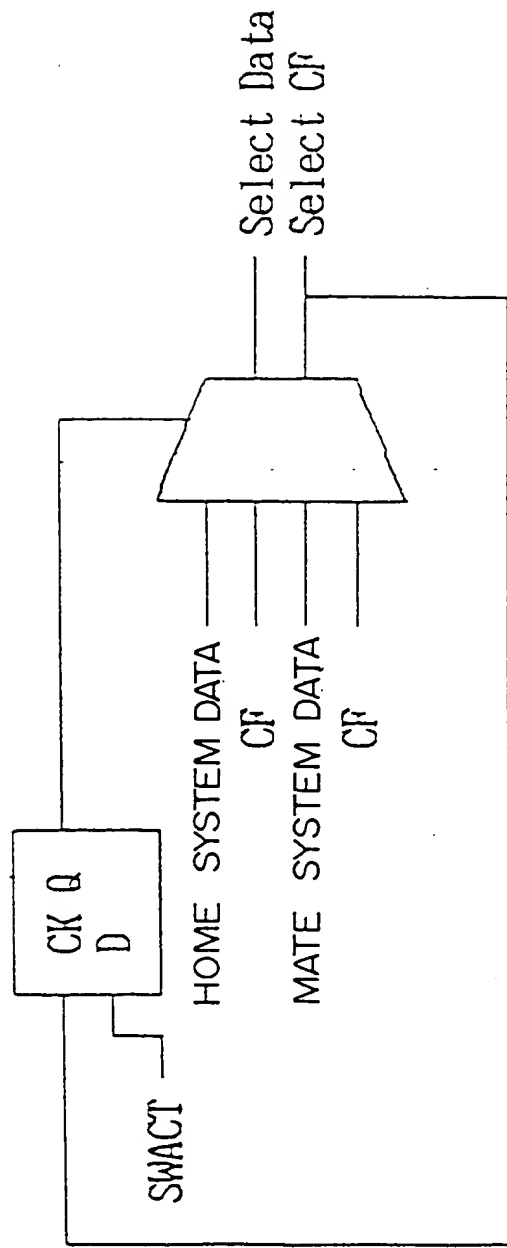


FIG. 302

ITEM	POINT NAME	REMARKS
①	HRDXCK	DISCONNECTION OF INPUT CLOCK 39M AND CELL FRAME FROM HOME SYSTEM MHCOM
②	HRDXPC	PARITY CHECK ERROR OF INPUT DATA FROM HOME SYSTEM MHCOM
③	MRDXCK	DISCONNECTION OF INPUT CLOCK 39M AND CELL FRAME FROM MATE SYSTEM MHCOM
④	MRDXPC	PARITY CHECK ERROR OF INPUT DATA FROM MATE SYSTEM MHCOM
⑤	CSPCPC	PARITY CHECK ERROR OF INPUT DATA TO CSPCAD LSI

FIG. 303

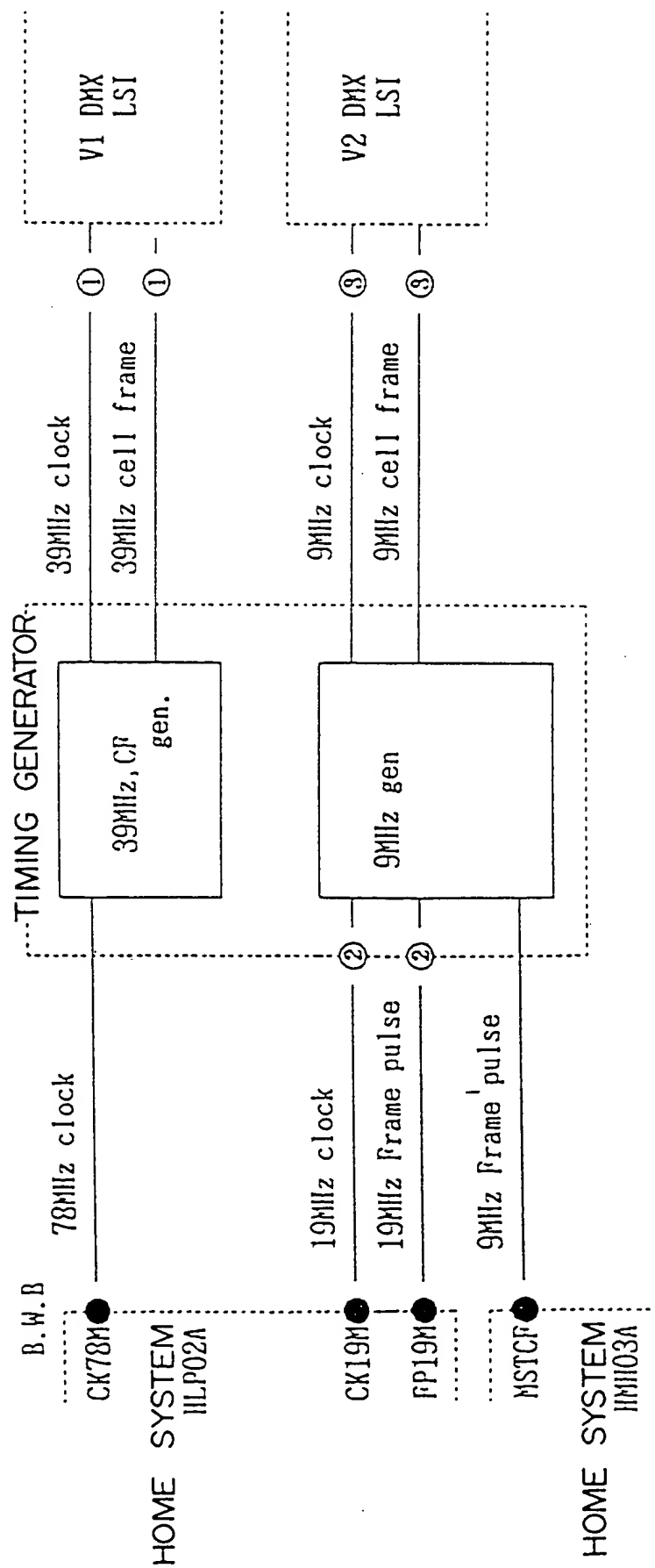


FIG. 304

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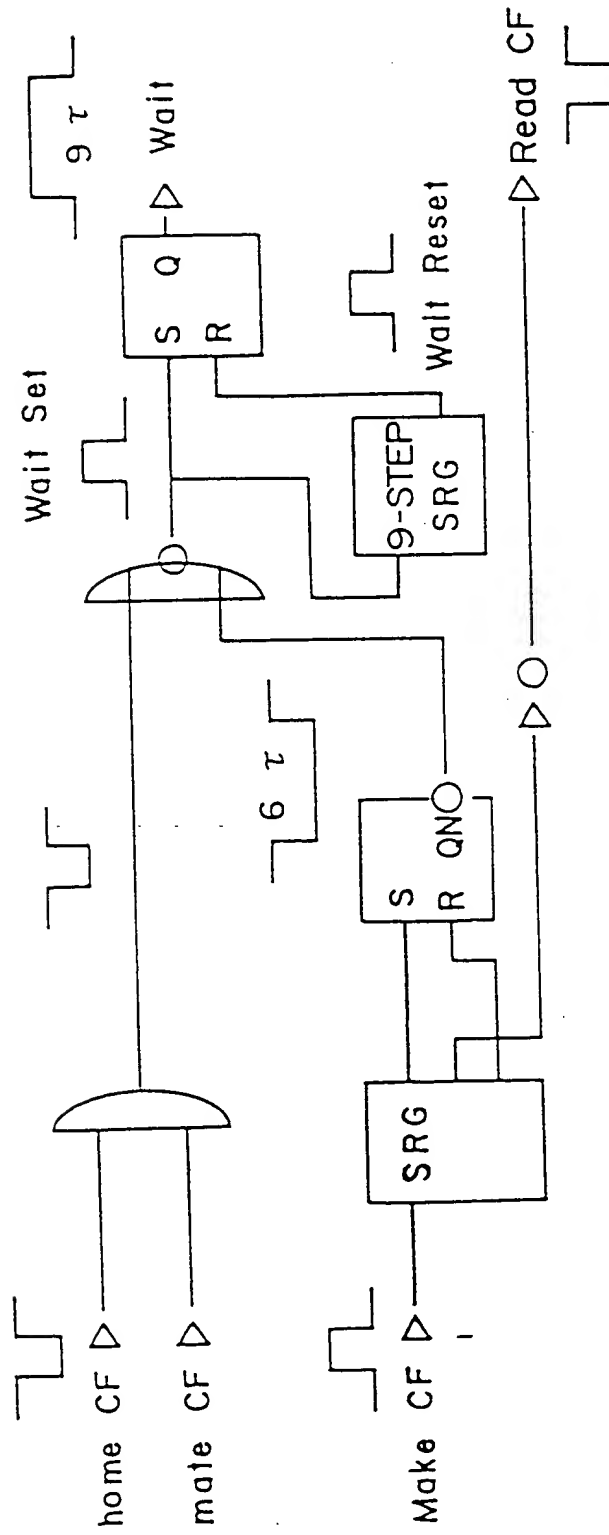
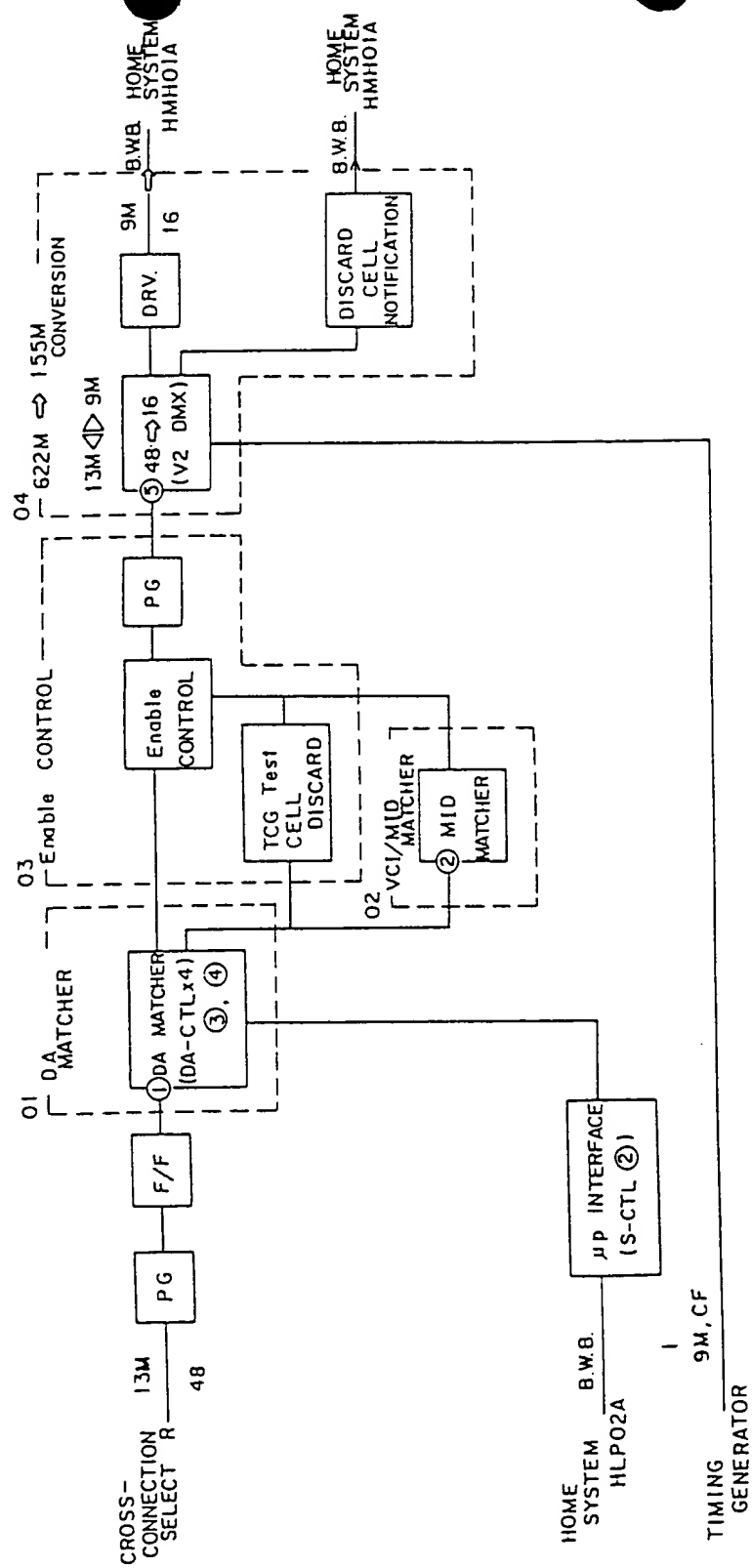


FIG. 306

ITEM	POINT NAME	REMARKS
①	CK39M	DISCONNECTION OF GENERATED 39M CLOCK AND CELL FRAME
②	CK19M	DISCONNECTION OF GENERATED 9M CLOCK AND FRAME PULSE
③	CK9M	DISCONNECTION OF GENERATED 9M CLOCK AND CELL FRAME

FIG. 307



ITEM	FUNCTION BLOCK NAME	REMARKS
01	DA MATCHER	OPERATING MATCHER ON BOM ADN SSM USING DA-CTL LSI AT DESTINATION ADDRESS (DA). WRITING T TAG PORTION DEGENERATED RDA ARISING AT DA FILTER.
02	VCI/MID	OPERATING MATCHER ON COM AND EOM AT VCI/MID.
03	ENABLE CONTROL	OUTPUTTING ONLY MATCHING CELLS TO PROCESSING UNIT ACCORDING TO RESULT OF DA MATCHER AND MID MATCHER.
04	622M→155M CONVERSION	CONVERTING SPEED OF 622M (13M, 48 PARALLEL) INTO 155M (9M, 16 PARALLEL) USING V2 DMX LSI.

FIG. 309

OOBT	SEGMENT TYPE		DA-CTL MATCH	READ DATA	WRITE DATA	ENABLE PROCESS	REMARKS
	ST01	ST00					
1	—	—	—	—	—	INVALID	DISCARD
0	0	0	—	0	—	INVALID	DISCARD
	0	COM	—	1	—	VALID	FETCH
	0	1	—	0	—	INVALID	DISCARD
	0	EOM	—	1	0	VALID	FETCH AND WRITE "0"
	1	0	0	0	—	INVALID	DISCARD
	1	BOM	0	1	0	VALID	FETCH AND WRITE "0"
	1	BOM	1	—	1	VALID	FETCH AND WRITE "1"
	1	1	0	0	—	INVALID	DISCARD
	1	SSM	0	1	0	VALID	FETCH AND WRITE "0"
	1	SSM	1	—	0	VALID	FETCH AND WRITE "0"

FIG. 310

ITEM	POINT NAME	REMARKS
(1)	DACTLP	PARITY CHECK ERROR OF INPUT DATA TO DACTL LSI
(2)	MIDMEM	PARITY CHECK ERROR BY DATA WRITE/READ IN RAM FOR VCI/MID MATCHER
(3)	MATADP	DACTL LSI MATCH ADDRESS PARITY ERROR
(4)	MIDPC	DACTL LSI VCI/ST/MID PARITY ERROR
(5)	OUTPC	PARITY CHECK ERROR OF INPUT DATA TO V2 DMX LSI

FIG. 311

1. **Introduction**
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 95. **Appendix**
 96. **Notes**
 97. **References**
 98. **Appendix**
 99. **Notes**
 100. **References**

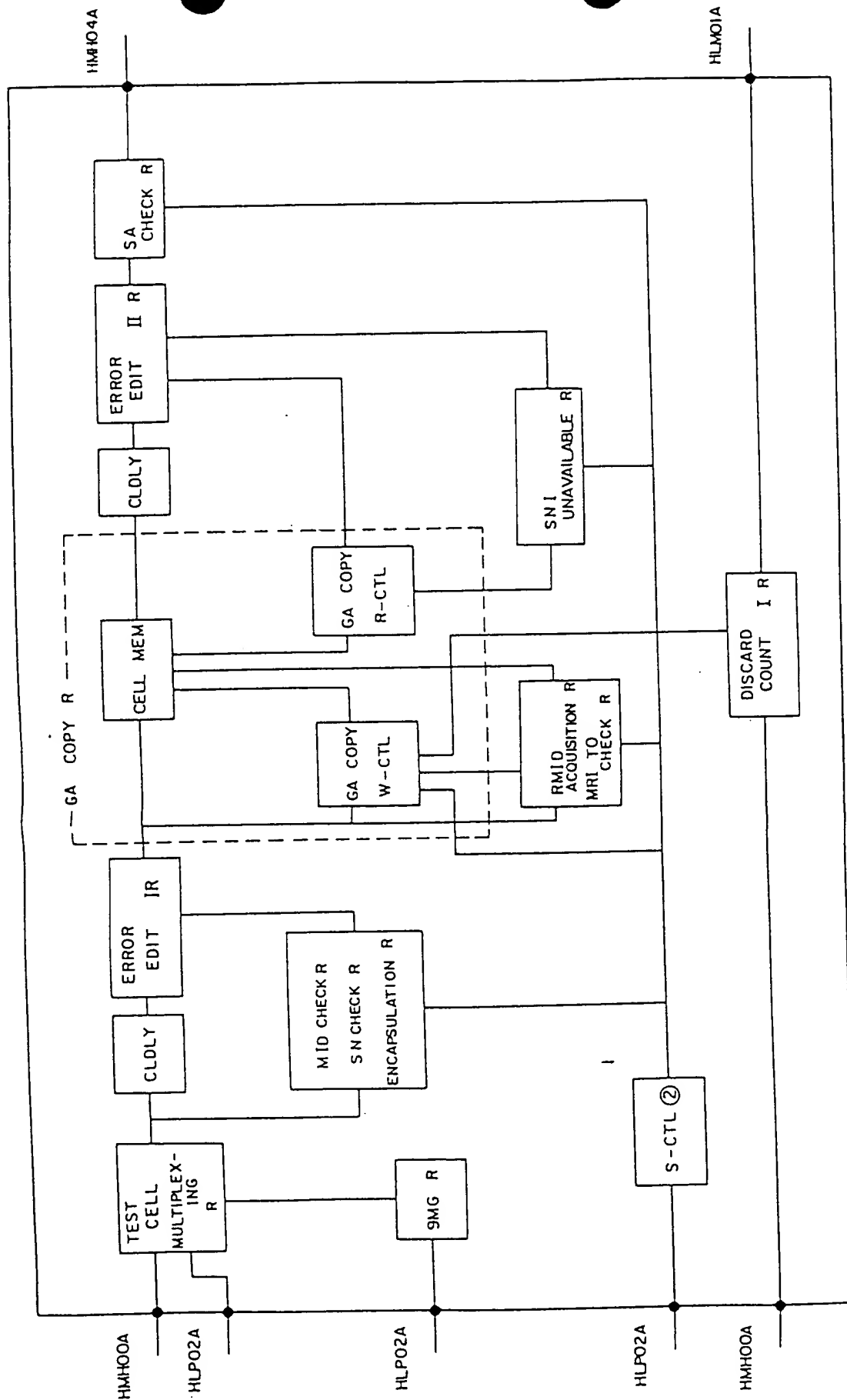


FIG. 3.12

ITEM	BLOCK NAME	C O N T E N T S
0 1	TEST CELL MULTIPLEX R 9MG R	MULTIPLEXING TEST CELL WHEN LINE CONTAINS IDLE CELLS GENERATING 9MCK USING 19MCK AND FP FROM HLP02A
0 2	MID CHECK R	CHECKING WHETHER OR NOT VCI/MID IS NOT ACTIVE AT BOM AND WHETHER OR NOT VCI/MID IS ACTIVE AT COM AND EOM.
0 3	SN CHECK R	INITIALIZING SN AT BON AND SSM AND CHECKING SEQUENCE IN SN AT COM AND EOM.
0 4	ENCAPSULATION R	ETCHING SIP INF. PDU FROM INTER-MH INF. PDU AND CHANGING SEGMENT TYPE(ST).
0 5	ERROR EDIT I R	ASSIGNING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG
0 6	RMID ACQUISITION R	COMPRESSING MID FOR INTERNAL PROCESS
0 7	MID TIMEOUT CHECK R	DETERMINING MRI TIMEOUT
0 8	GA COPY R	OUTPUTTING CELL INPUT AT GA TO EACH SUBSCRIBER
0 9	SNI AVAILABLE R	DISCARDING CELL AT DT FAULT OF SNI OR OTHER DISABLED RECEPTION
1 0	ERROR EDIT II R	ASSIGNING ERROR CHECKED BY EACH CHECKER TO EACH POSITION OF ERROR FLAG
1 1	SA CHECK R	RETURNING SELF-LOOPBACK CELL IN RESPONSE TO GA MESSAGE
1 2	DISCARD COUNTER IR	COUNTING DISCARDED CELLS AT V2 DMX OF HMF00A AND GA COPY UNIT OF HMF01A

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ITEM	POINT NAME	REMARKS
①	INPC	PARITY CHECK ERROR OF INPUT DATA (LINE CELL) FROM HMH00A
②	TSTPC	PARITY CHECK ERROR OF INPUT DATA (TEST CELL) FROM HMH02A
③	INCF	DISCONNECTION CHECK OF 9MCK GENERATED BASED ON INPUT CELL FRAME FROM HMH00A AND 19MCK AND FP FROM HLP02A

FIG. 315

ITEM	FUNCTION BLOCK NAME	REMARKS
01	ST CHECK	LATCHING SEGMENT TYPE (ST) OF INPUT CELL AND STORING FOR PROCESS FOR EACH ST.
02	MID CHECK	CHECKING THAT VCI/MID IS NOT IN USE AT BOM AND SSM AND THAT VCI/MID IS IN USE AT COM AND EOM.

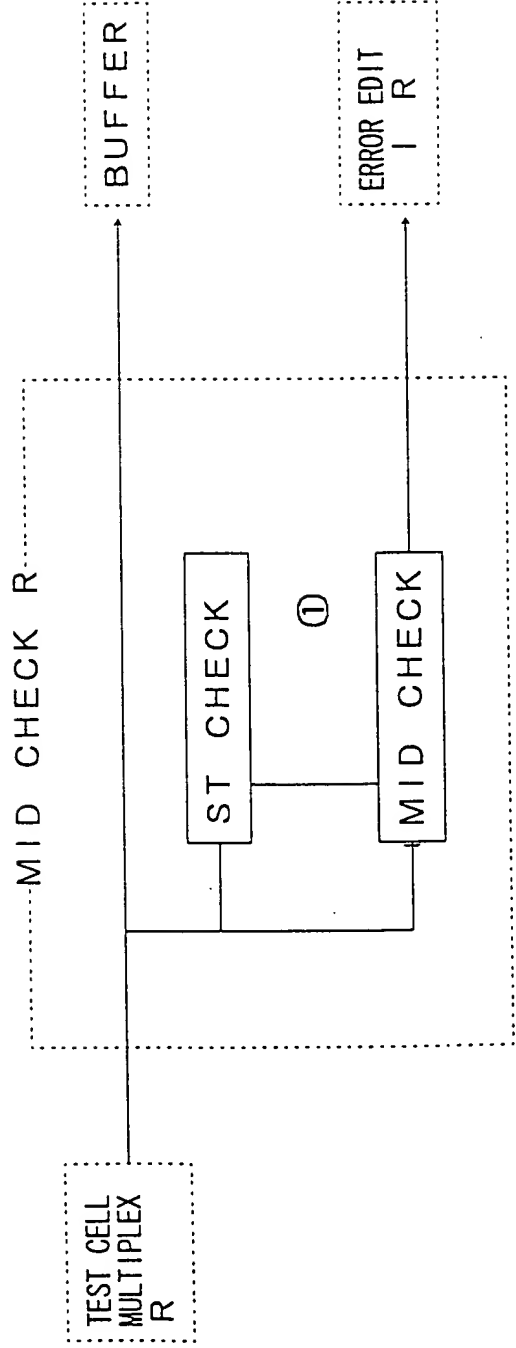


FIG. 316

SEGMENT TYPE	DM	RAM INFORMATION (READ)	PROCESS
INTER-MH BOM	MATCH	ACT	SETTING IN ACT STATE
INTER-MH BOM	UNMATCH	ACT	RELEASING
INTER-MH BOM	MATCH	NOT ACT	SETTING IN ACT STATE
INTER-MH BOM	UNMATCH	NOT ACT	RELEASING
INTER-MH SSM	MATCH	ACT	RELEASING
INTER-MH SSM	UNMATCH	ACT	RELEASING
INTER-MH SSM	MATCH	NOT ACT	RELEASING
INTER-MH SSM	UNMATCH	NOT ACT	RELEASING
INTER-MH COM	D. C.	ACT	SETTING IN ACT STATE
INTER-MH COM	D. C.	NOT ACT	RELEASING
INTER-MH EOM	D. C.	ACT	RELEASING
INTER-MH EOM	D. C.	NOT ACT	RELEASING

—

Segment Type	error	DM	Error Flag	
Inter-MII BOM	VCI/MID Is Active	0	EF1	EFMS(Master Error Flag)
			EF2	EFMA(MID Active Error)
		1	EF2	EFMA(MID Active Error)
Inter-MII SSH	VCI/MID Is Active	0	EF1	EFMS(Master Error Flag)
			EF2	EFMA(MID Active Error)
		1	EF2	EFMA(MID Active Error)
Inter-MII COM	VCI/MID Is Not Active	EF1	EF1	EFMC(COM MID Active Error) EFMS(Master Error Flag)
Inter-MII EOM	VCI/MID Is Not Active	EF1	EF1	EFMC(COM MID Active Error) EFMS(Master Error Flag)

FIG. 318

ITEM	POINT NAME	address	bit	REMARKS
①	SNMEM	0210	06	SN check memory parity NG

FIG. 319

ITEM	FUNCTION BLOCK NAME	REMARKS
0 1	SN+1	ADDING 1 TO SEQUENCE NUMBER(SN)
0 2	SN CHECK	STORING SN+1 WHEN BOM ARRIVES. COMPARING LATCHED SN WITH STORED SN WHEN COM ARRIVES TO CHECK WHETHER OR NOT THEY MATCH (SEQUENTIAL). EOM AND COM PERFORM SIMILAR PROCESSES. SSM IS NOT OBJECT OF CHECK.

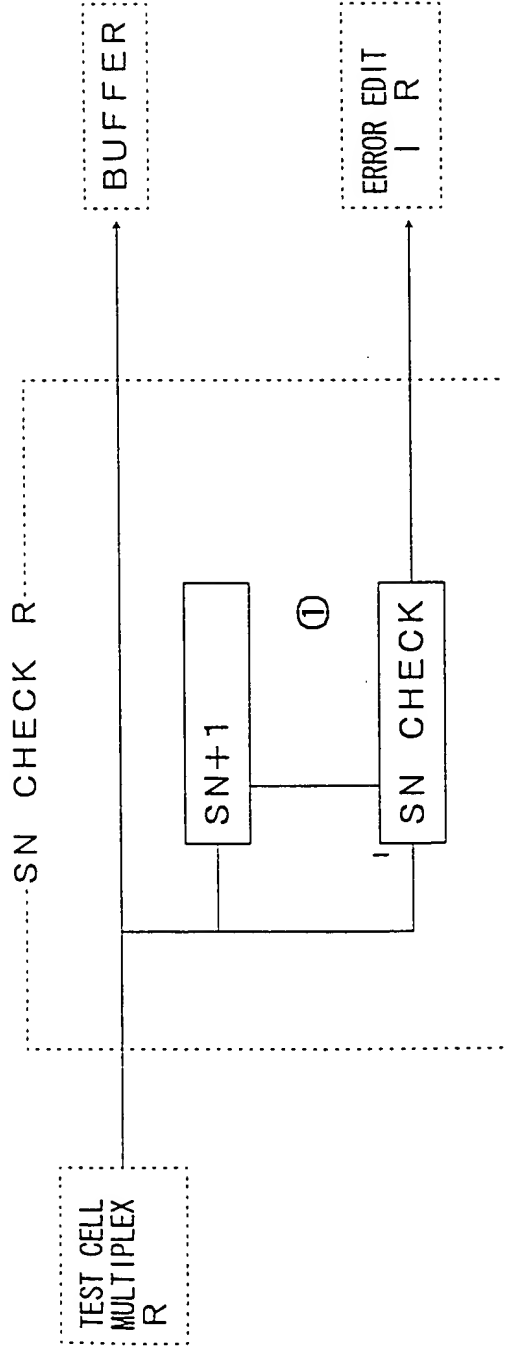


FIG. 320

Segment Type	error	Error Flag	
		EF1	EFMS (Master Error Flag)
Inter-MII COM	DIFFERENT SEQUENCES	EF2	EFMS (Invalid Sequence Number)
		EF1	EFMS (Master Error Flag)
Inter-MII EOM	DIFFERENT SEQUENCES	EF2	EFMS (Invalid Sequence Number)
		EF1	EFMS (Master Error Flag)

FIG. 321

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SN CHECK	LATCHING SEGMENT TYPE(ST) OF INPUT CELL AND STORING IT FOR USE IN PROCESS OF EACH ST.
02	ENCAPSULATION	CHANGING INTO BOM IF COM IS NEXT TO BOM, AND INTO SSM IF EOM IS NEXT TO BOM.

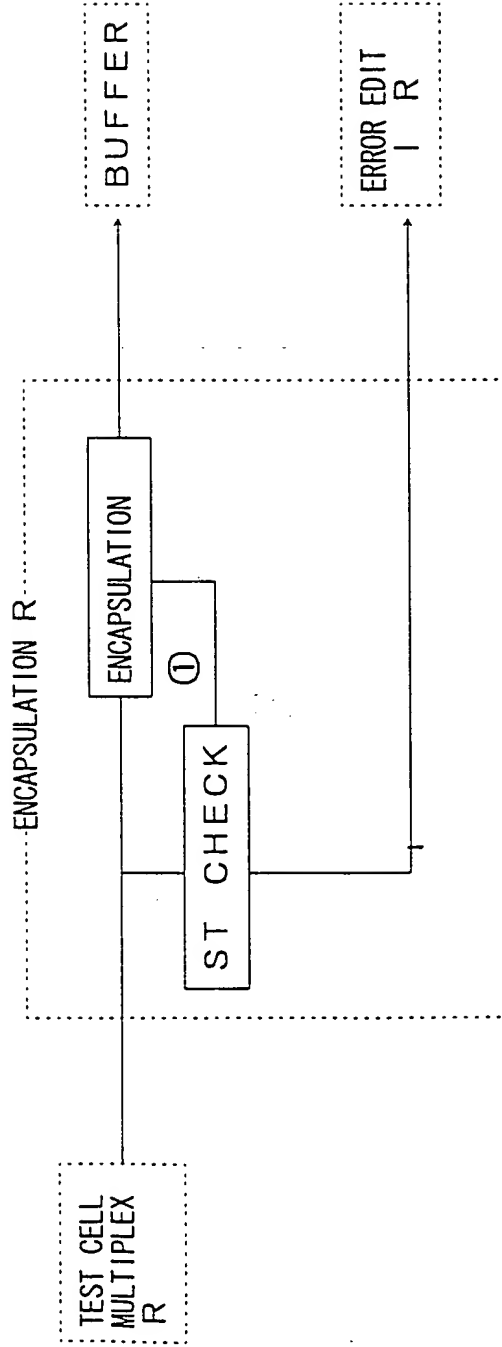


FIG. 323

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Segment Type	error	Error Flag	
Inter-MI SMI	UNCONDITIONAL ERROR	EF1	ERMS(Master Error Flag)
		EF2	EFEN(Encapsulation Error)

FIG. 324

[illegible]

ITEM	FUNCTION BLOCK NAME	REMARKS
O 1	DEFINING ERROR	ASSIGNING ERROR INFORMATION OF EACH CHECKER TO POSITION OF EACH ERROR FLAG.

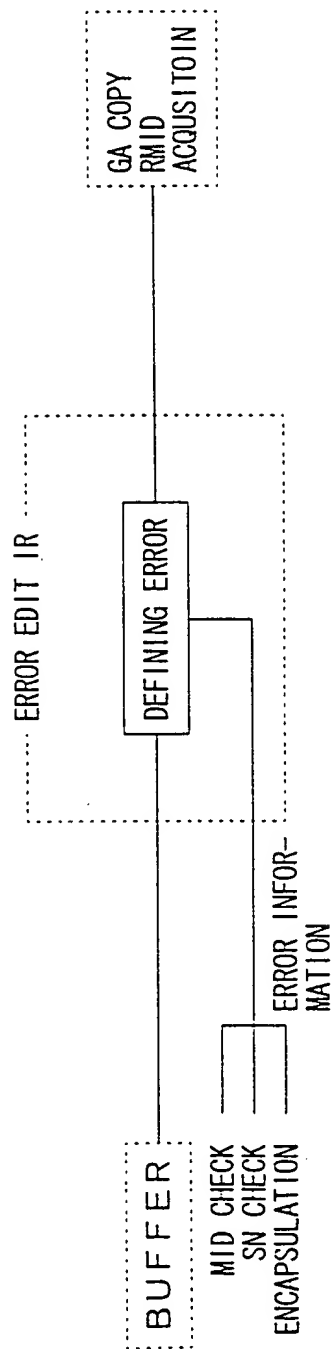


FIG. 326

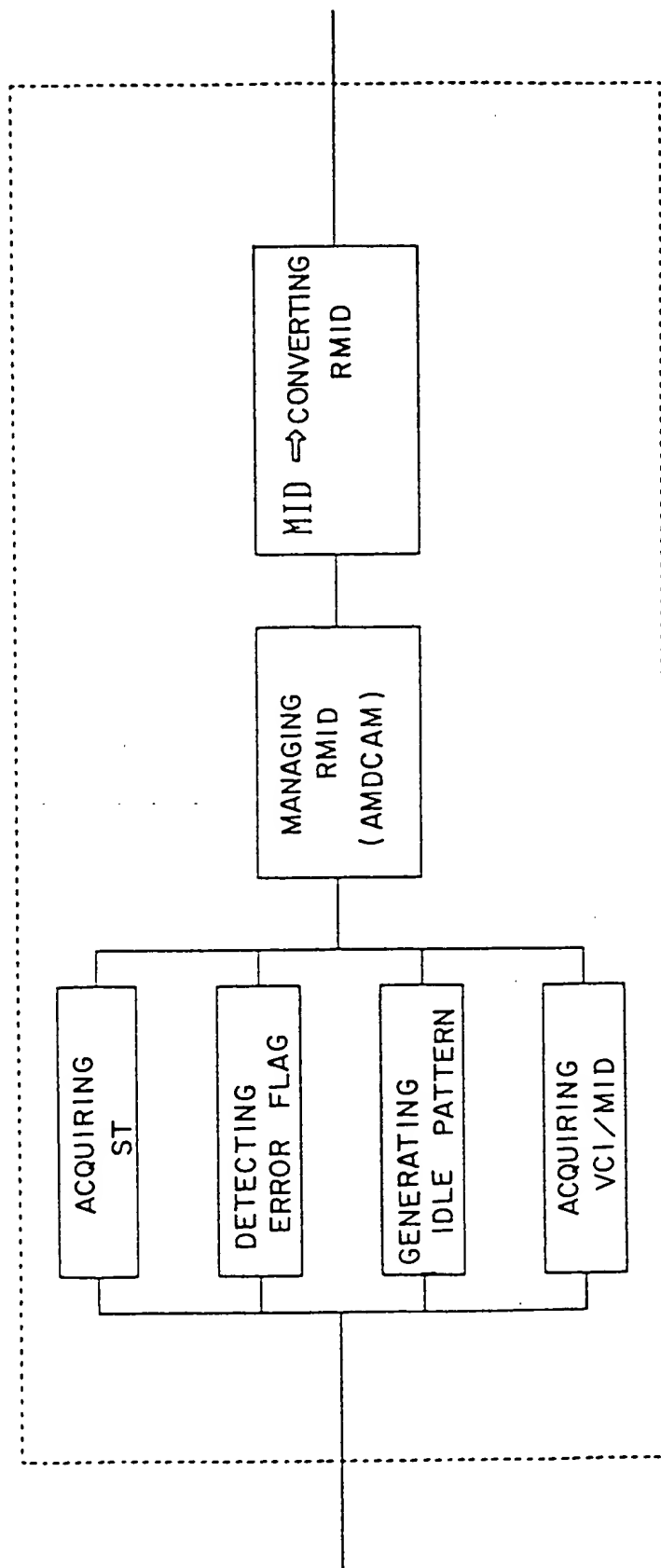


FIG. 327

ITEM	FUNCTION BLOCK NAME	REMARKS
01	ACQUIRING ST	FETCHING ST OF VALID CELL AND DETERMINING ST.
02	GENERATING IDLE PATTERN	TRANSMITTING IDLE PATTERN (ALL 1) TO AMD-CAM AS INITIALIZATION
03	ACQUIRING VCI/MID	ACQUIRING VCI/MID OF VALID CELL AND TRANSMITTING IT TO RMID MANAGEMENT
04	MANAGING RMID (AMD-CAM)	DETERMINING WHETHER OR NOT ACQUIRED VCI/MID MATCH IF MATCHING, MATCH ADDRESS SIGNAL IS OUTPUT
05	CONVERTING RMID ⇔ MID	OVERWRITING MATCH ADDRESS SIGNAL (RMID) OUTPUT AT AMD-CAM ON MID OF CELL

FIG. 328

SEGMENT TYPE	E R R O R	E R R O R	
		EF1	EF2
INTER-MH BOM	WHEN RMID CANNOT BE ACQUIRED	EF1	EFMS (MASTER ERROR FLAG)
		EF2	EFMN (RMID ASSIGNED ERROR)
INTER-MH SSM	WHEN RMID CANNOT BE ACQUIRED	EF1	EFMS (MASTER ERROR FLAG)
		EF2	EFMN (RMID ASSIGNED ERROR)
INTER-MH COM	WHEN RMID IS NOT ACQUIRED PREVIOUSLY, AND IS RELEASED	EF1	EFMD (RMID ACTIVE ERROR) EFMS (MASTER ERROR FLAG)
INTER-MH EOM	WHEN RMID IS NOT ACQUIRED PREVIOUSLY, AND IS RELEASED	EF1	EFMD (RMID ACTIVE ERROR) EFMS (MASTER ERROR FLAG)

FIG. 329

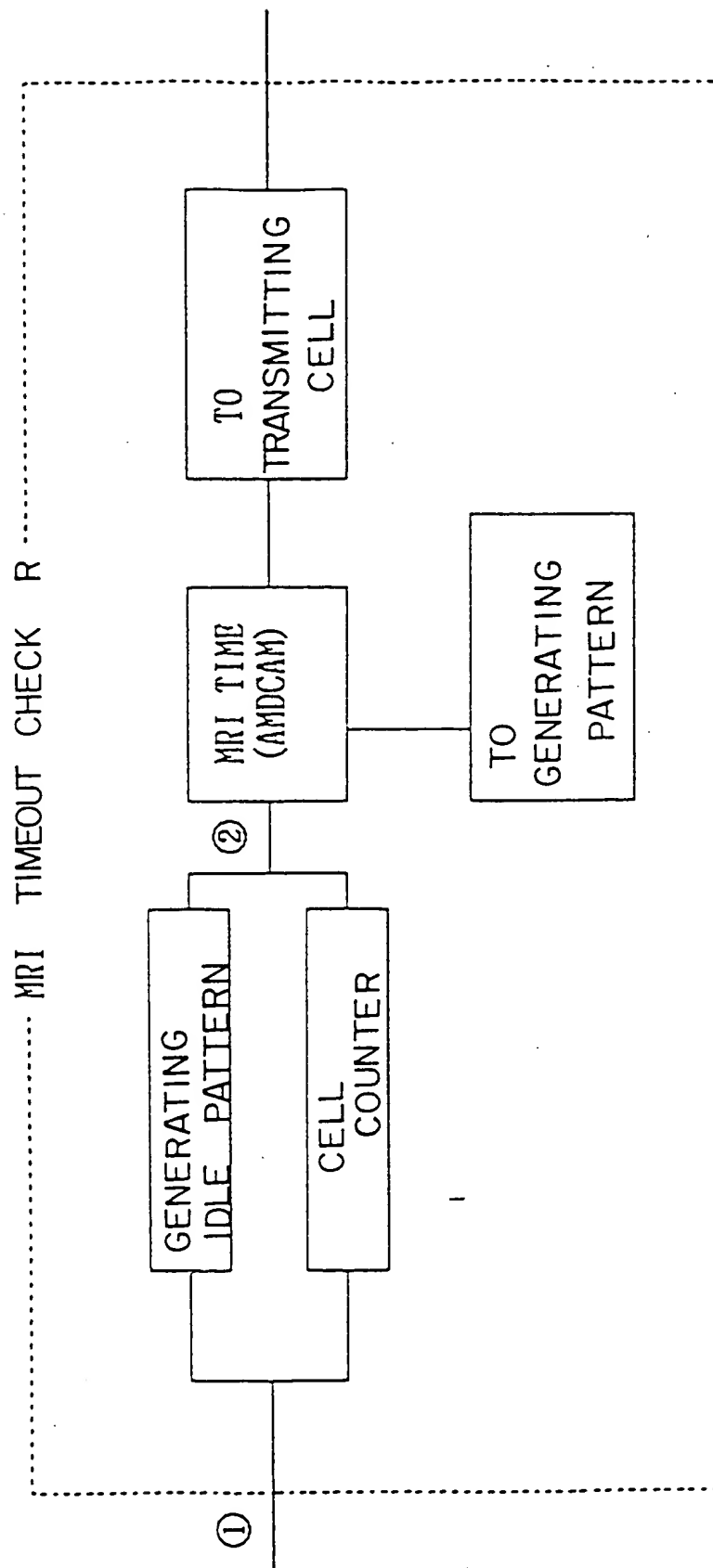


FIG. 330

ITEM	FUNCTION BLOCK NAME	REMARKS
0 1	CELL ST DETERMINATION (CONCURRENT WITH MID COMPRESSION)	FETCHING ST OF VALID CELL AND DETERMINING ST.
0 2	CELL COUNTER	CELL COUNTER HAVING MODE IN WHICH CELLS ARE COUNTED EACH TIME ALL CELLS ARRIVE AND HAVING MODE IN WHICH ONLY VALID CELLS ARE COUNTED
0 3	GENERATING IDLE PATTERN (CONCURRENT WITH MID COMPRESSION)	INITIALIZING MRI TIME (AMD-CAM) TRANSMITTING IDLE PATTERN FOR BOM
0 4	MRI TIME (AMDCAM)	CHECKING FOR TIMEOUT FOR EACH CELL
0 5	TO GENERATING PATTERN	OUTPUTTING TO PATTERN TO MRI TIME (AMD-CAM) AT TIMEOUT
0 6	TO TRANSMITTING CELL	OUTPUTTING TO CELL INSTEAD OF EOM OF TIMEOUT MESSAGE

FIG. 331

0000000000000000

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0	D. C.														
0	D. C.														
0	D. C.			0	0	0	DESTINATION	SNI - ID					D. C.		
0	D. C.														

D.C.: Don't care

FIG. 332

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Segment Type	error	Error Flag	
		EF1	EFMS(Master Error Flag)
Inter MH COM	IEOM DOES NOT ARRIVE WITHIN 177MS AFTER IBOM ARRIVED	EF2	EFMT(MRI time out)
Inter MH COM Inter MH EOM	CELL ARRIVED AFTER TO CELL IS TRANSMITTED	EF1	EFMD(RMID Active Error) EFMS(Master Error Flag)

FIG. 333

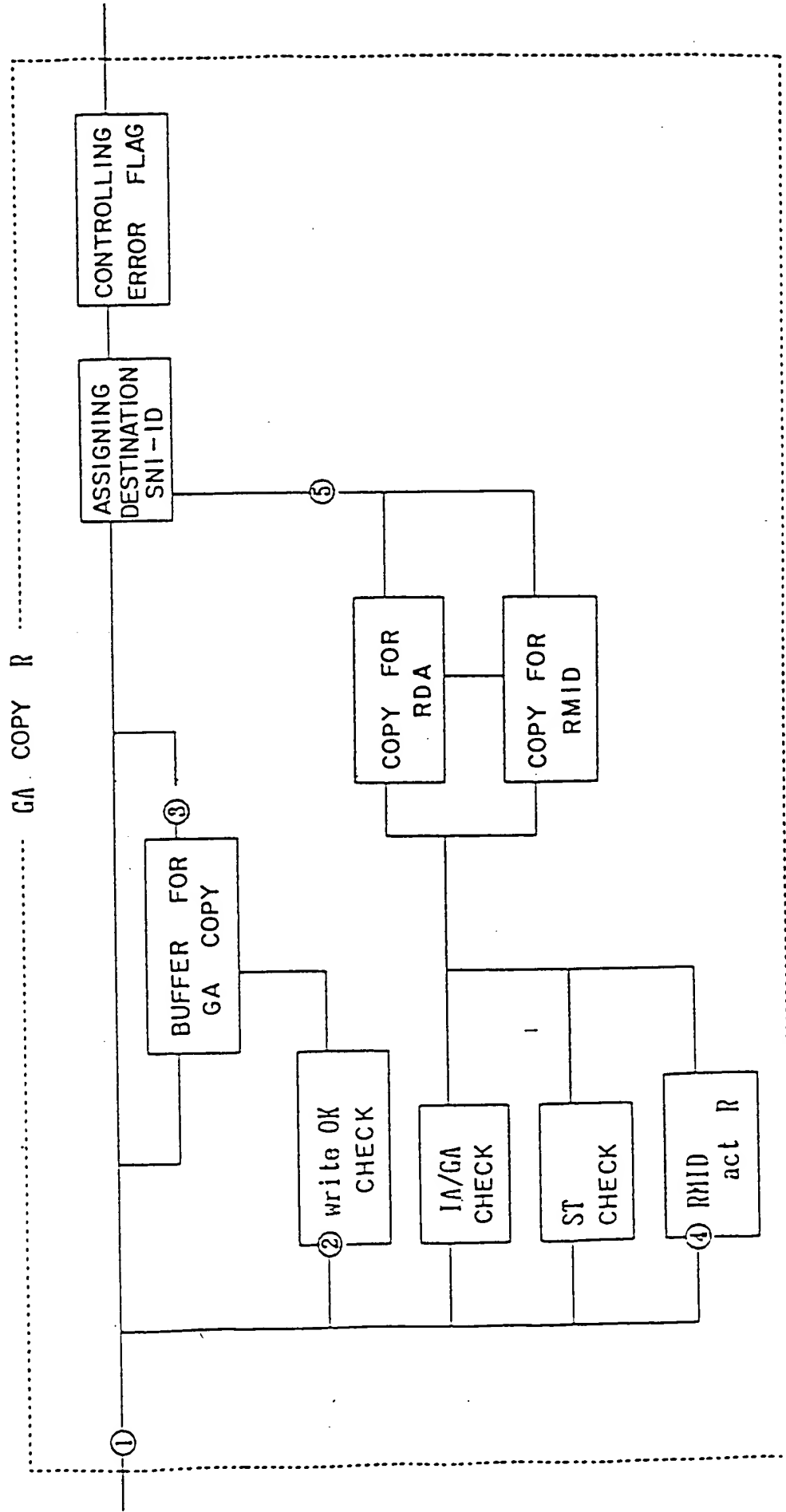


FIG. 334

ITEM	FUNCTION BLOCK NAME	R E M A R K S
O 1	WRITE OK CHECK	READING WRITE O.K.R TABLE ACCORDING TO VCI/RMID AND DETERMINING WHETHER OR NOT DATA CAN BE WRITTEN TO BUFFER FOR GA COPY. IF BUFFER IS FULL (NOT WRITABLE), DISCARD SIGNAL IS TRANSMITTED TO DISCARD COUNT.
O 2	BUFFER FOR GA COPY	BUFFER IN WHICH CELLS ARE WRITTEN TO MAKE COPIES AT GA COPY.
O 3	RMID ACT R	STORING, FOR EACH RMID, INFORMATION ABOUT WHETHER OR NOT PRESENTLY RECEIVED MESSAGE IS BEING GA COPIED.
O 4	IA/GA CHECK	DETERMINING WHETHER RDA OF EACH MESSAGE IS IA OR GA.
O 5	ST CHECK	LATCHING SIP SEGMENT TYPE (SST) OF INPUT CELL AND STORING IT TO PROCESS IT FOR EACH ST.
O 6	COPY FOR RDA	IF RDA IS GA IN IBOM, COPIED-TO SNI IS DETERMINED FROM GA COPY R TABLE USING ADDRESS OF RDA AND COPIED CELL IS TRANSMITTED.
O 7	COPY FOR RMID	IF RDA OF ICOM AND IEOM IS GA, COPIED-TO SNI IS DETERMINED FROM MESSAGE COPY TABLE USING ADDRESS OF RMID AND COPIED CELL IS TRANSMITTED.
O 7	ASSIGNING DESTINATION SNI-ID	ASSIGNING DESTINATION SNI-ID TO TRANSMITTED CELL. IF RDA IS IA, IT IS OBTAINED DIRECTLY FROM RDA. IF RDA IS GA, IT IS OBTAINED FROM COPY TABLE.
O 9	CONTROLLING ERROR FLAG	IF EFMS(MASTER ERROR FLAG) OF CELL IS SET 'ON' AND CELL IS COPIED, ERROR FLAG AT EF2 IS MASKED TO PREVENT DOUBLE COUNT AT TM PORTION OF HLM01A.

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Segment Type	error	Error Flag	
		ERI	EFMS(Master Error Flag)
Inter MII BOM	IEOM HAS NOT ARRIVED AND IBOM HAVING SAME RMID ARRIVES	ERI	EFMS(Master Error Flag)
Inter MII BOM Inter MII COM Inter MII EOM	EFMS (MASTER ERROR FLAG) OF CELL IS SET 'ON' AND CELL IS COPIED	ERI	EFMS(Master Error Flag)

FIG. 336

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ITEM	POINT NAME	REMARKS
①	GACOPY	GA COPY INPUT UNIT LINE ERROR
②	WOKMEM	Write OK memory Parity Check Error
③	GAMEM	GA copy cell memory Parity Check Error
④	GAACTP	GA ACT Parity Check Error
⑤	GACPPC	GA copy bit map Parity Check Error

FIG. 337

ITEM	FUNCTION BLOCK NAME	REMARKS
0 1	SNI BLOCK INFORMATION	SUPPRESSING TRANSMISSION OF MESSAGE TO SNI ACCORDING TO BLOCK INFORMATION.

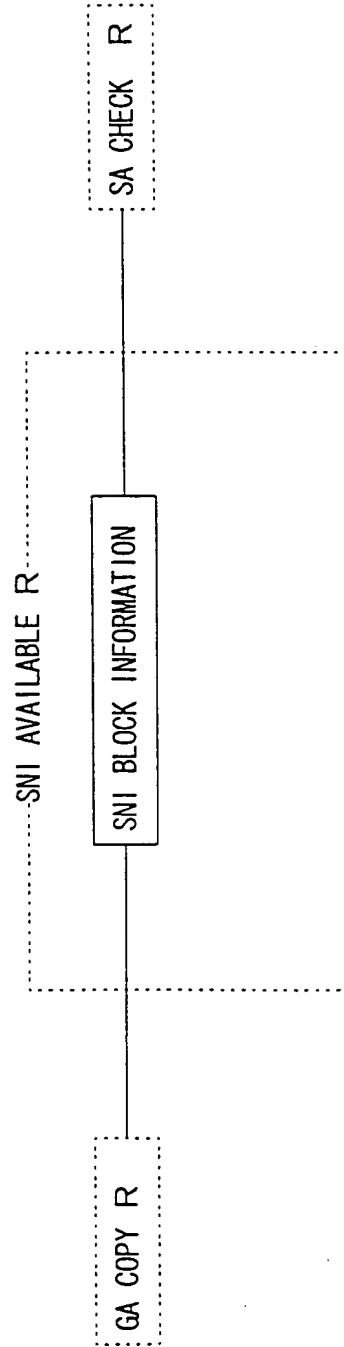


FIG. 338

Segment Type	error	Error Flag	
		EF1	EFMS (Master Error Flag)
Inter-MII BOM	not Available	EF2	EFDA (Destination SNI not Available)
		EF1	EFMS (Master Error Flag)
Inter-MII SSM	not Available	EF2	EFDA (Destination SNI not Available)
		EF1	EFMS (Master Error Flag)

FIG. 339

ITEM	POINT NAME	REMARKS
①	AVPC	SNI AVAILABLE PARITY CHECK ERROR
②	BRLCPC	BRLC NUMBER PARITY CHECK ERROR

FIG. 340

ITEM	FUNCTION BLOCK NAME	REMARKS
01	DEFINING ERROR	ASSIGNING ERROR INFORMATION OF EACH CHECKER TO POSITION OF EACH ERROR FLAG.

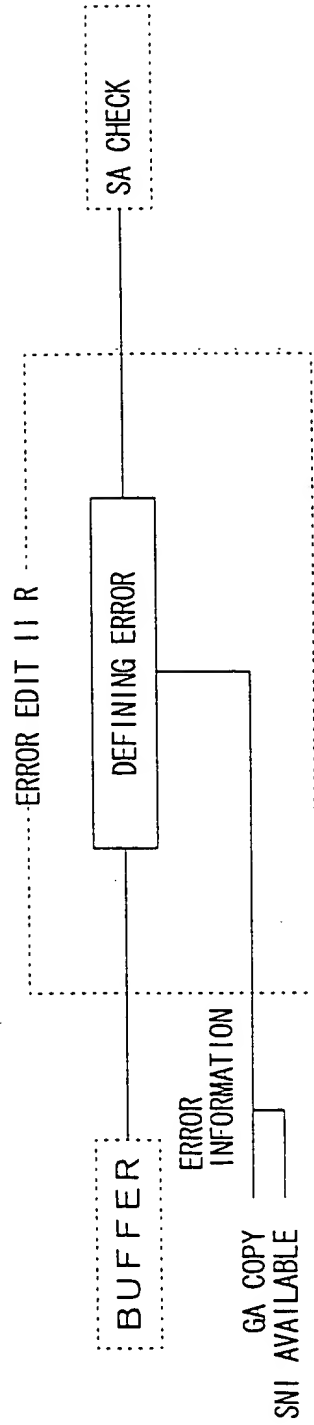


FIG. 341

ITEM	FUNCTION BLOCK NAME	REMARKS
01	SA CHECK	RETURNING LOOPBACK CELL RECEIVED FROM ENTERED SA

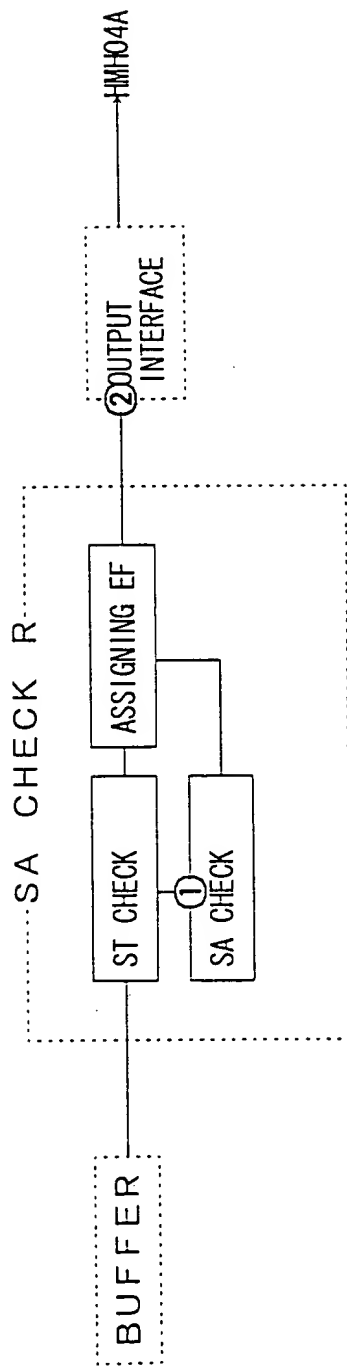


FIG. 342

Segment Type	error	Error Flag	
		EF1	EFMS(Master Error Flag)
Inter-MH BOM	SELF-LOOPBACK CELL	EF2	EFDO(Destination equal to Org.SNI)
		EF1	EFMS(Master Error Flag)
Inter-MH SSM	SELF-LOOPBACK CELL	EF2	EFDO(Destination equal to Org.SNI)
		EF1	EFMS(Master Error Flag)

NOTE : INTER-MH COM AND INTER-MH COM ARE D.C.
 NOT OBJECT OF CHECK IF HIGHEST ORDER BIT OF DESTINATION SNI-ID IS 1
 NOT OBJECT OF CHECK IF EFMS OF CELL HAS ALREADY BEEN SET "ON"

FIG. 343

ITEM	POINT NAME	REMARKS
①	SAMADP	PARITY CHECK ERROR OF SA CHECK MATCH ADDRESS
②	OUTPC	HMHO1A EXIT PARITY CHECK ERROR

FIG. 344

SC ATTRIBUTE	WHEN MATCHING AT CAM	WHEN NON-MATCHING AT CAM
1	ERROR (UNACCEPTABLE AT ENTERD ADDRESS)	TRANSMISSION ENABLED
2	TRANSMISSION ENABLED	ERROR (UNACCEPTABLE AT ADDRESS OTHER THEN ENTERED ADDRESS)

FIG. 345

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□: ENTIRE CABLE ■: B.W.B.

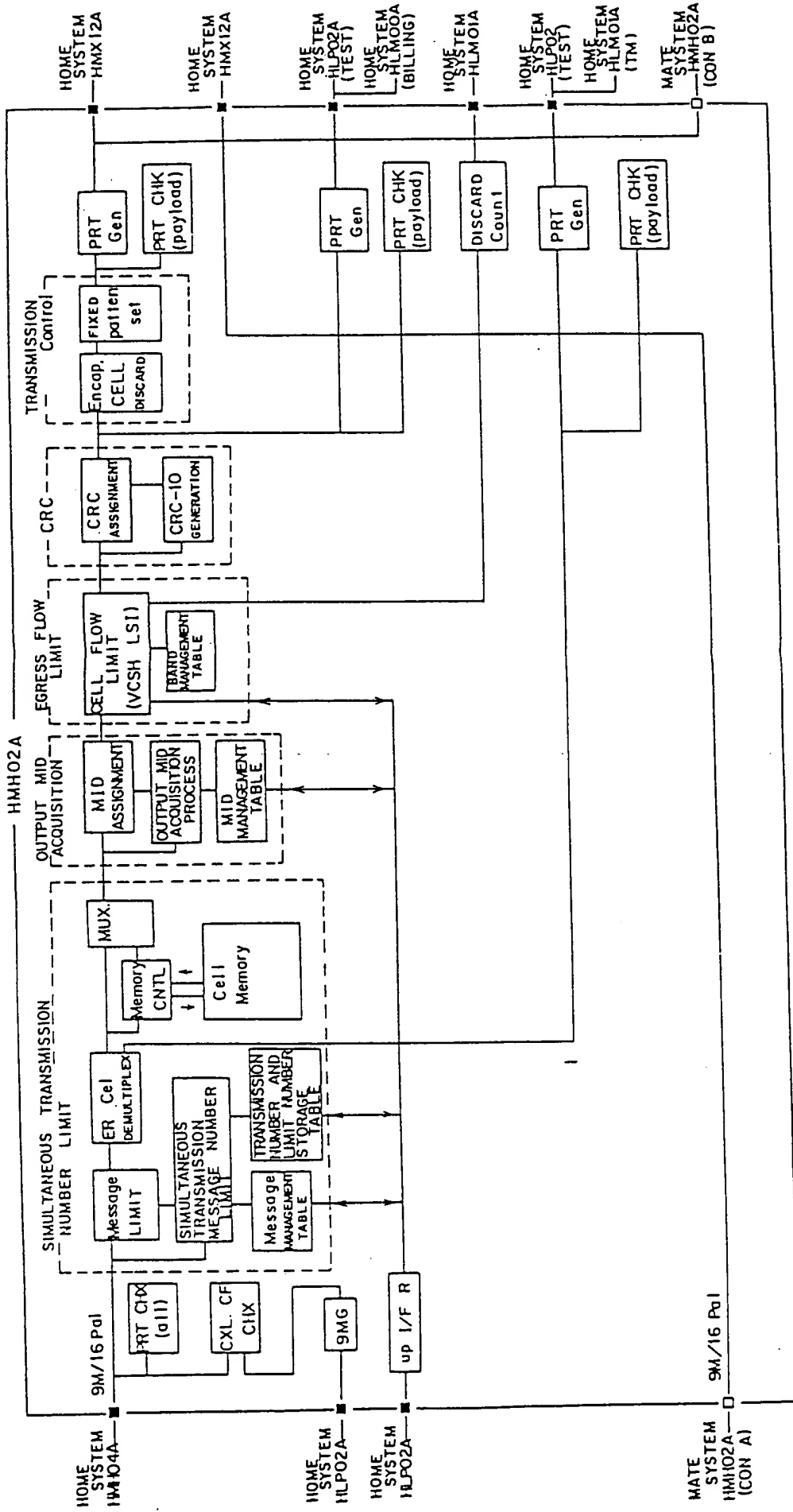


FIG. 346

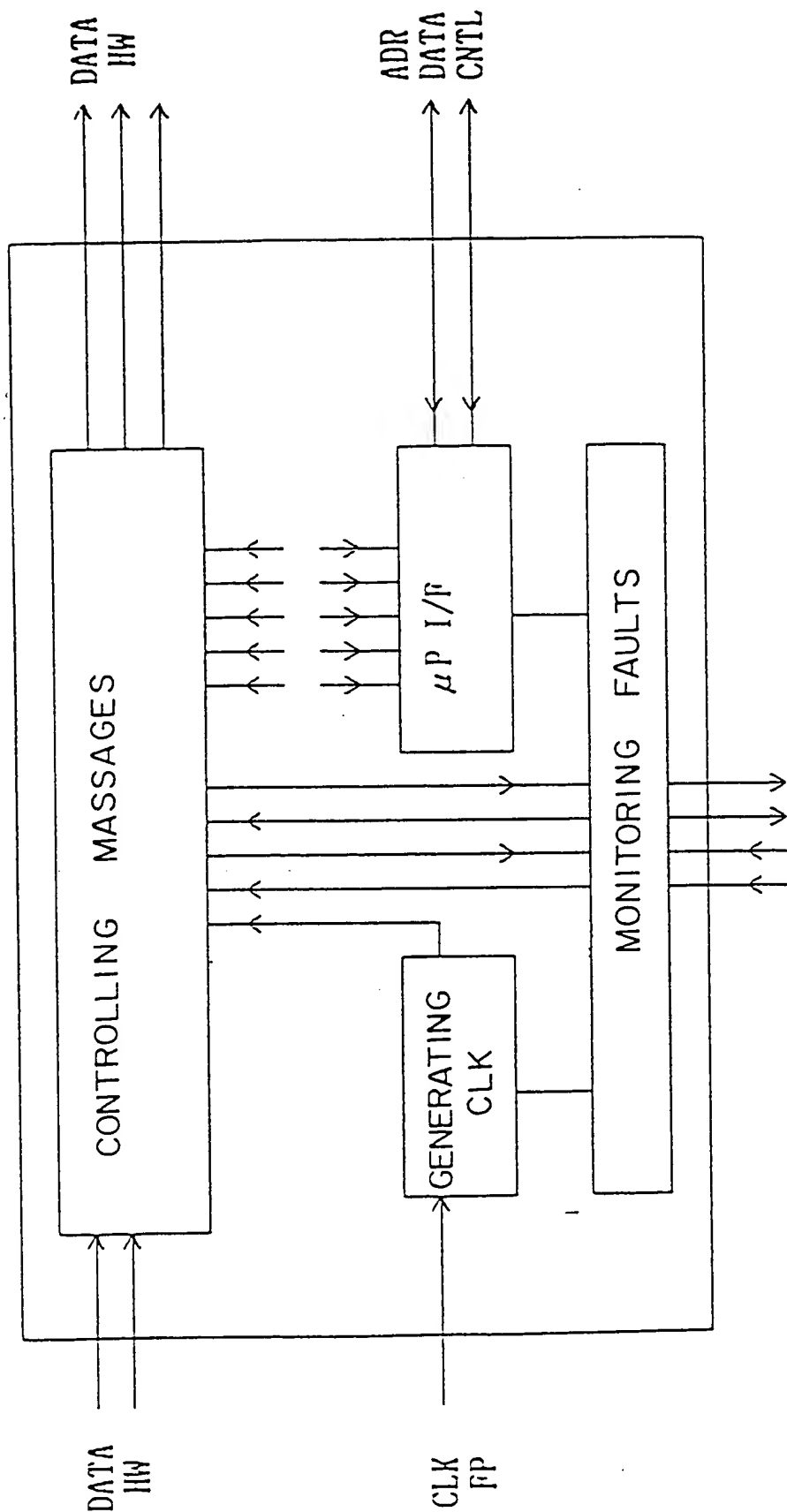


FIG. 347

ITEM	FUNCTION	REMARKS
01	CONTROLLING MESSAGE	TRANSMISSION LIMIT OF MESSAGE AND BAND CONTROL
02	μ P I/F	RECEIVING VARIOUS CONTROL SIGNAL TRANSMITTED FROM μ P AND DATA, AND INTERNAL CONTROL
03	GENERATING CLK	GENERATING 9MHz. CLK BASED ON RECEIVED 19MHz. CLK
04	MONITORING FAULTS	MONITORING FAULT MONITOR OBJECT POINT IN PWCB

FIG. 348

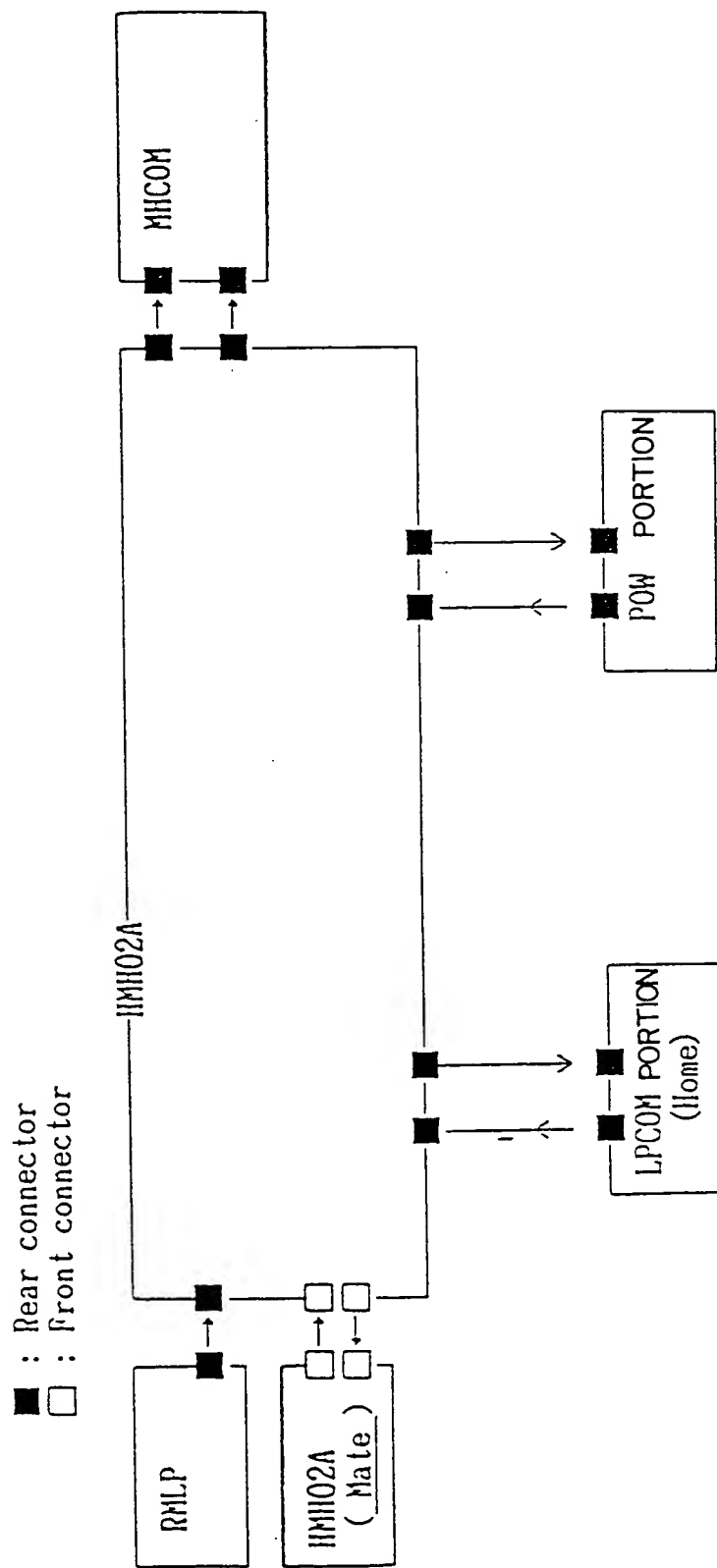


FIG. 349

ITEM	FUNCTION	
01	SIMULTANEOUS TRANSMISSION LIMIT	LIMITING NUMBER OF MESSAGES FOR EACH SNI
02	OUTPUT MID ACQUISITION	CONVERTING RMID (COMPRESSED MID) INTO OUTPUT MID
03	EGRESS FLOW LIMIT	LIMITING OUTPUT BAND (PEAK RATE) FOR EACH SNI
04	DISCARD COUNTER	COUNTING AND STORING CELLS AND MESSAGES DISCARD AT EGRESS FLOW LIMITING UNIT
05	CRC-10 GENERATION	GENERATING AND ASSIGNING CRC-10 OF CELL PAYLOAD
06	TRANSMISSION CONTROL	MANIPULATING HEADER PATTERN FOR SPECIFIED CELL AND RELEASING ENCAPSULATION
07	INTER-SYSTEM CROSS-CONNECTION	FETCHING HW DATA FROM HMH02A OF MATE SYSTEM AND TRANSMITTING DATA TO MDX UNIT OF HOME SYSTEM

FIG. 350

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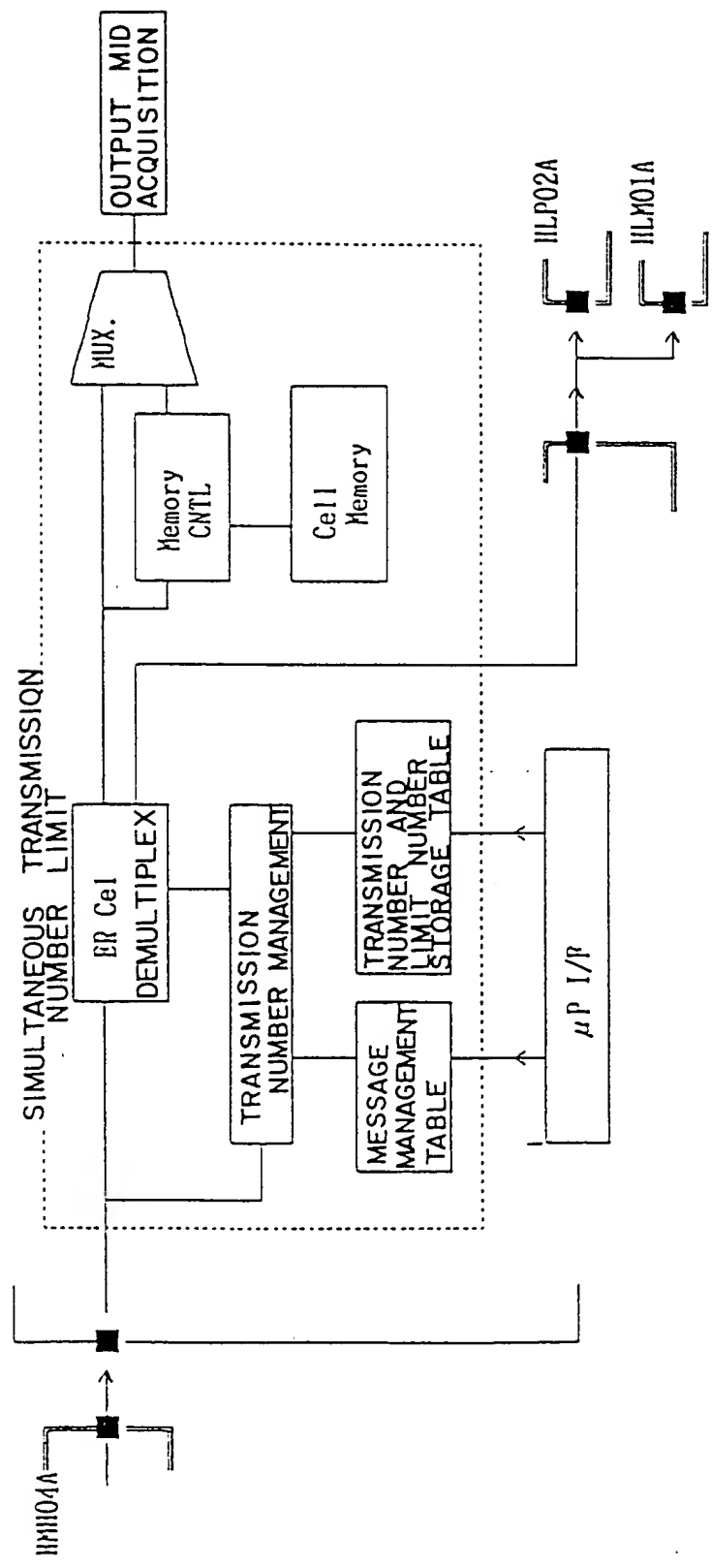


FIG. 351

LIMIT NUMBER	TRANSMISSION NUMBER : LIMIT NUMBER	
1	NUMBER OF MESSAGES = 0	MESSAGE TRANSMISSION ENABLED
	NUMBER OF MESSAGES = 1	NEXT MESSAGE IS BUFFERED AND SUBSEQUENT MESSAGES CANNOT BE TRANSMITTED
16	16 > NUMBER OF MESSAGES	MESSAGE TRANSMISSION ENABLED
	NUMBER OF MESSAGES = 16	NEXT MESSAGE IS BUFFERED AND SUBSEQUENT MESSAGES CANNOT BE TRANSMITTED

FIG. 352

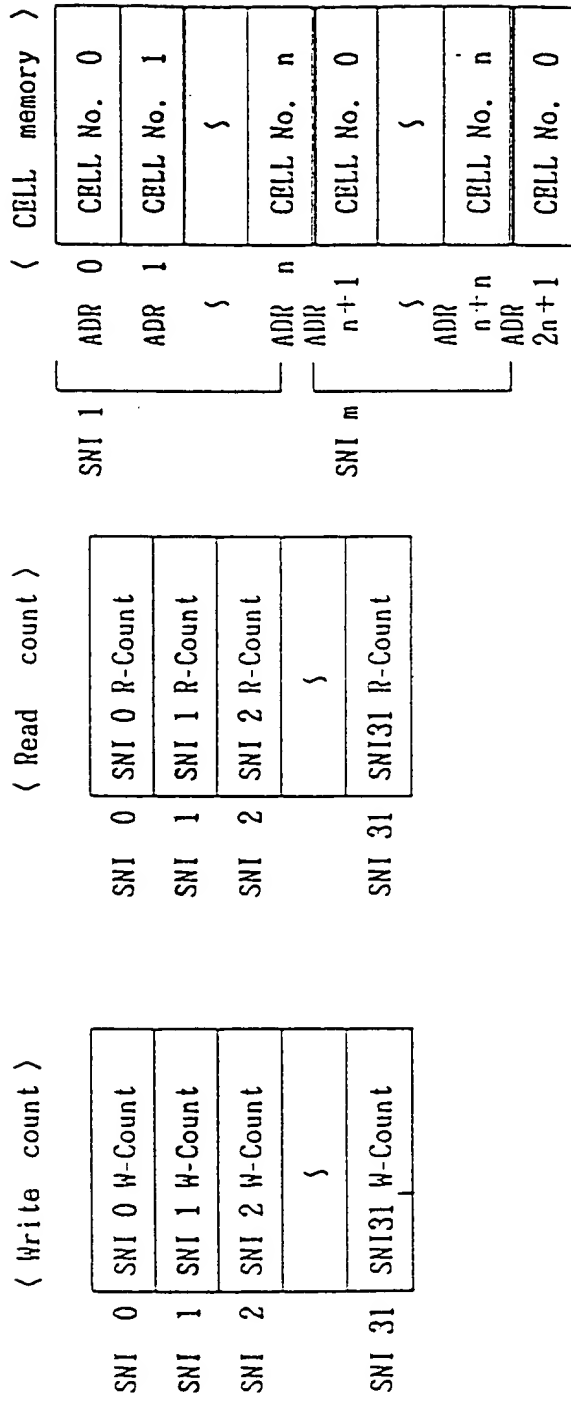


FIG. 353

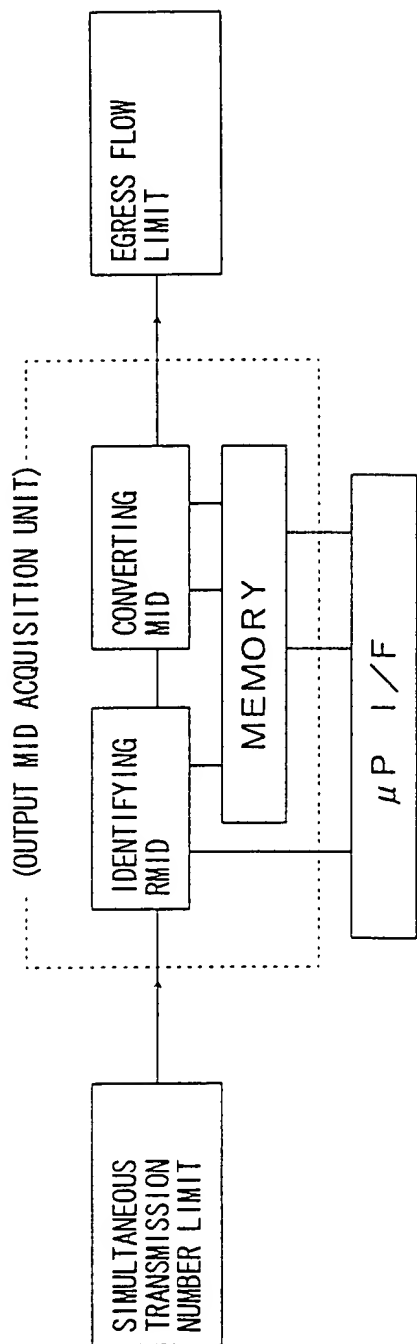


FIG. 354

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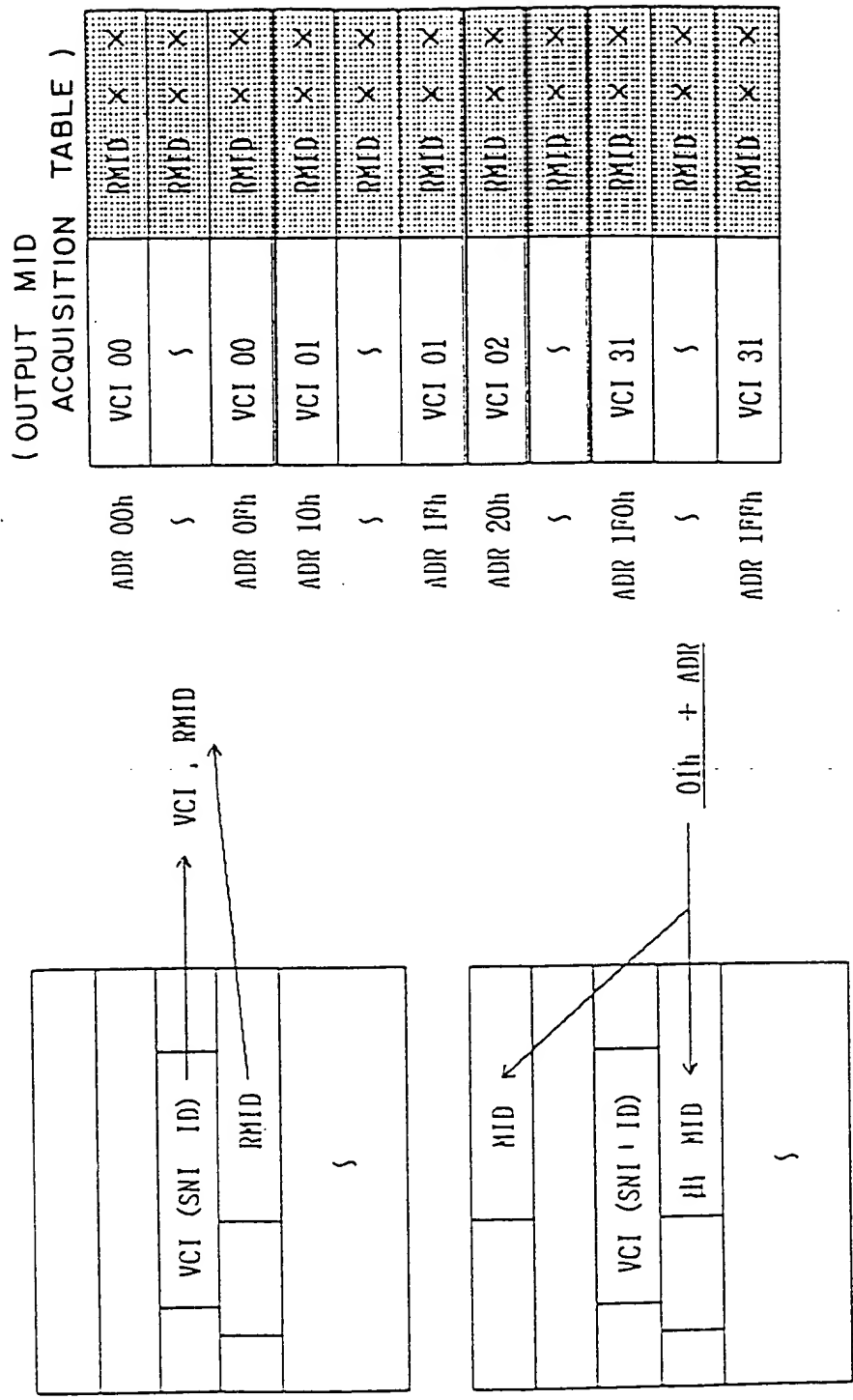


FIG. 355

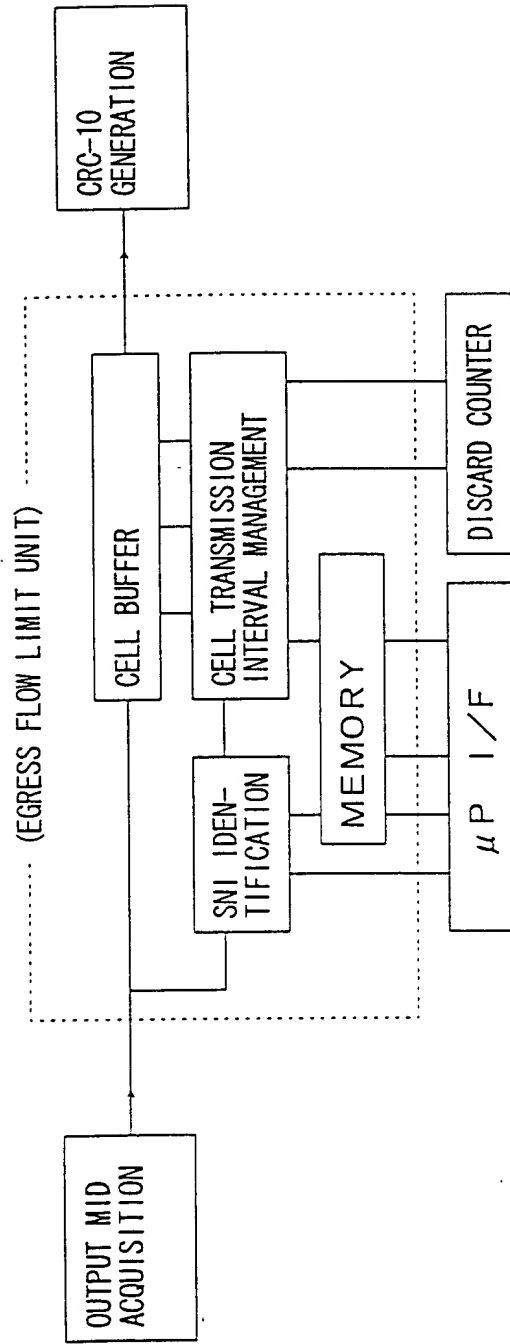


FIG. 356

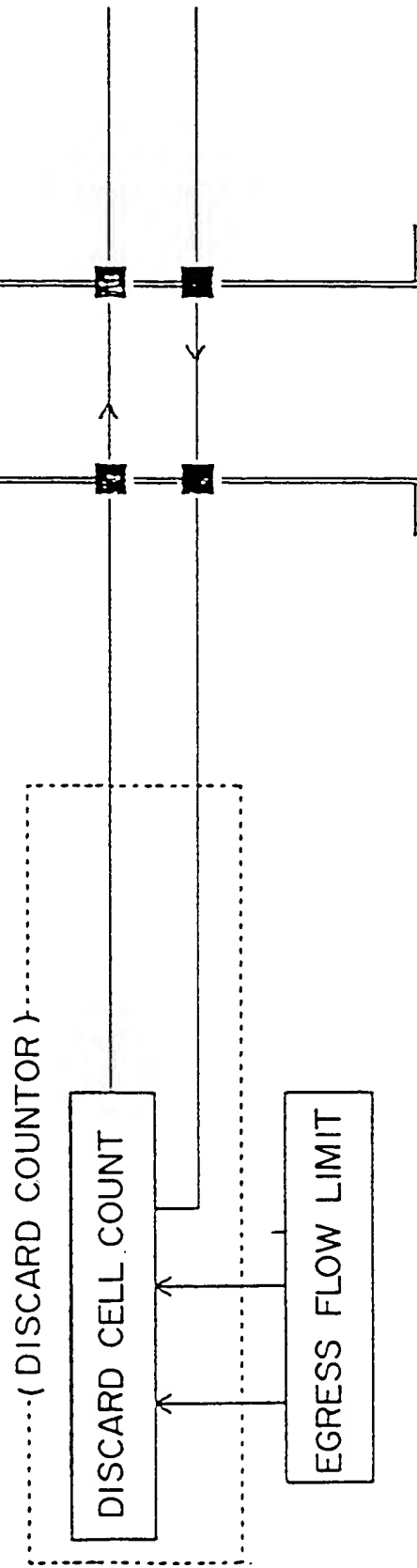


FIG. 357

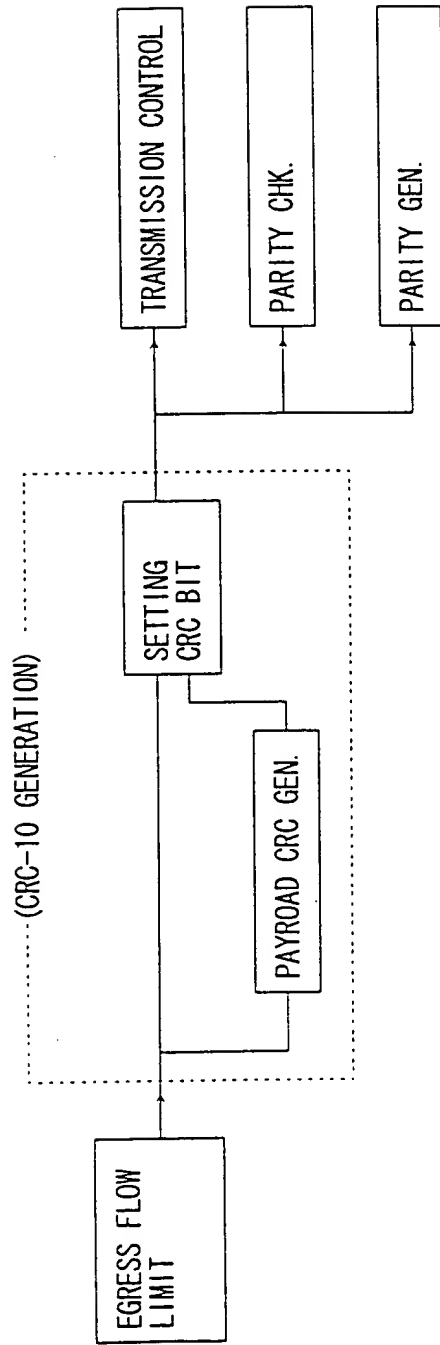


FIG. 358

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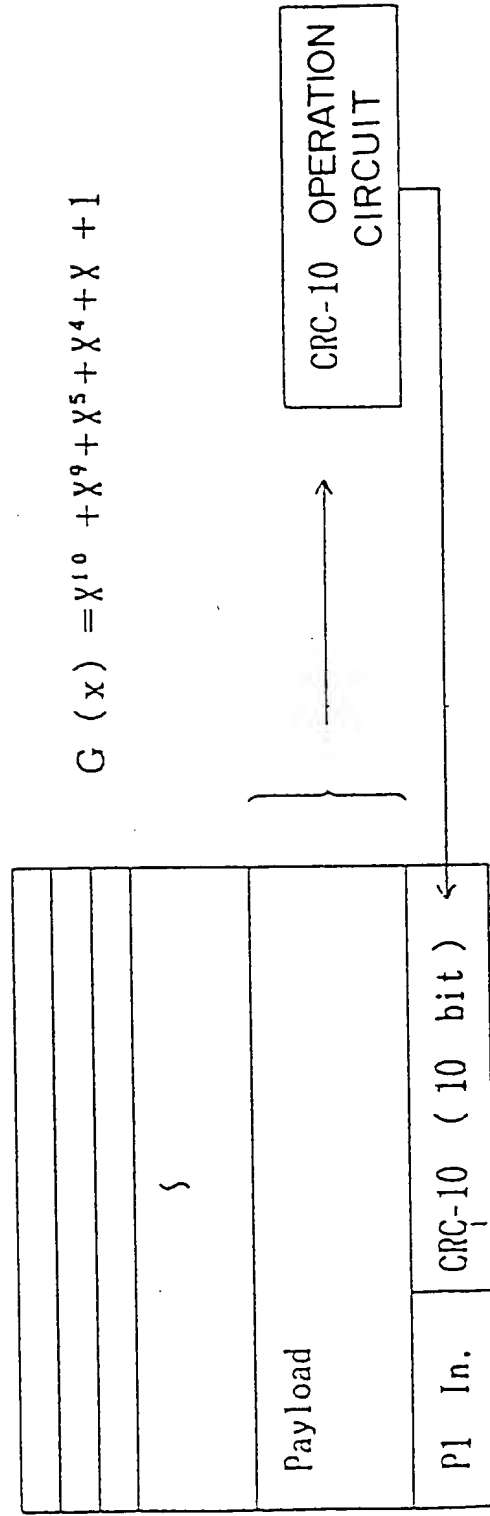


FIG. 359

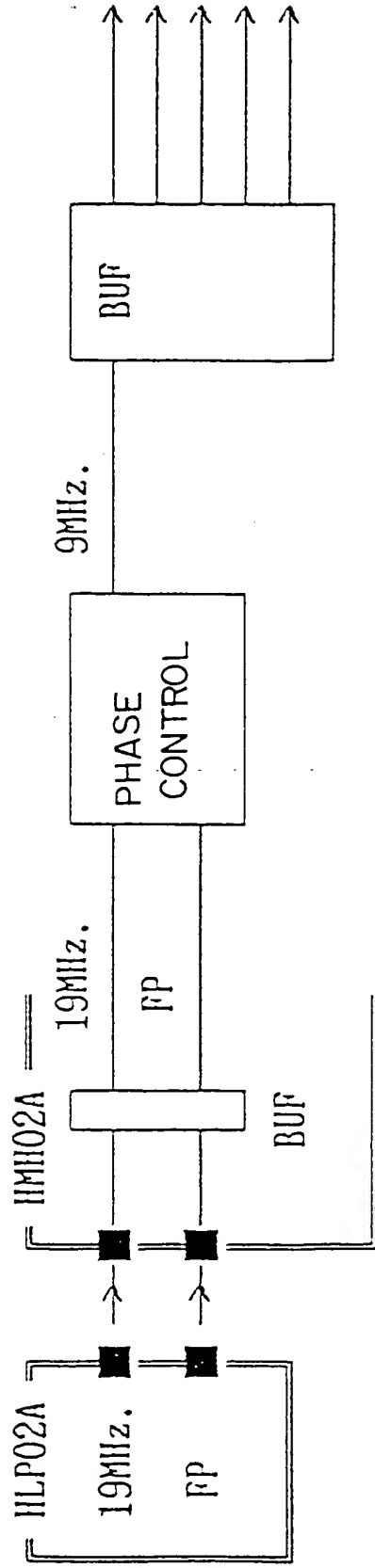


FIG. 360

66360: 66360

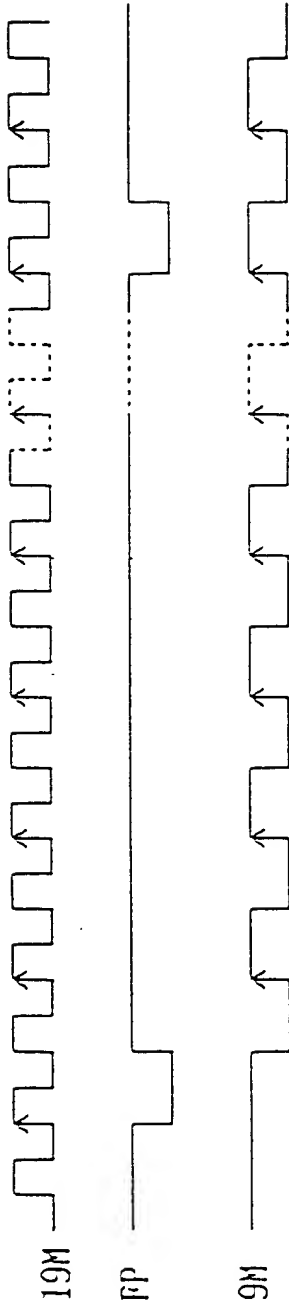


FIG. 361

ITEM	FUNCTION	
01	MESSAGE CONTROL CONTROL	CONTROLLING EACH FUNCTION OF MESSAGE CONTROL UNIT
02	MEMORY WRT/RED CONTROL	MANAGING AND CONTROLLING MEMORY OF EACH FUNCTION BLOCK
03	I/F	INTERFACING WITH MNG μ -P OF HLP02A

FIG. 362

PHCB CODE	OUTLINE OF FUNCTIONS
HMX10A	SMUX FUNCTION (MULTIPLEXING ATM-CELL FROM SMLP TO 622 MBPS HIGHWAY)
	RDMX FUNCTION (TRANSMITTING 622MBPS HIGHWAY FROM ASSW TO RMLP)
	TDMX FUNCTION (DMUXING TEST CELL FROM 622 MBPS HIGHWAY FROM ASSW)
HMX11A	RMUX FUNCTION (MULTIPLEXING ATM-CELL FROM RMLP TO 622 MBPS HIGHWAY)
	SDMX FUNCTION (DMUXING SMLP CELL FROM 622 MBPS HIGHWAY FROM ASSW)
	SIG-MUX FUNCTION (MULTIPLEXING INTRA-STATION COMMUNICATIONS CELL TO 622 MBPS HIGHWAY TO ASSW)
	SIG-DMX FUNCTION (DMUXING INTRA-STATION COMMUNICATIONS CELL FROM 622 MBPS HIGHWAY FROM ASSW)
HMX12A	SVCC FUNCTION (VCCM-CONVERTING ATM CELL FROM SMLP)
	RVCC FUNCTION (VCCM-CONVERTING ATM CELL FROM RMLP)
	TMUX FUNCTION (MULTIPLEXING TEST CELL DMUXED IN TDMX OF HMX10A TO RMLP HIGHWAY, AND MULTIPLEXING CELL DMUXED IN SDMX OF HMX11A TO SMLP HIGHWAY)
	SCHEDULER FUNCTION (CONTROLLING SMUX/RMUX OPERATION)
HSF05A	LAP TERMINATING FUNCTION (TERMINATING INTRA-STATION COMMUNICATIONS SIMPLE LAP AND COMMUNICATING WITH BSGC-SH)
	MSCN/MSD TERMINATING/EDITING FUNCTION
	VCC COPY FUNCTION
	CLOCK DISTRIBUTING FUNCTION

FIG. 363

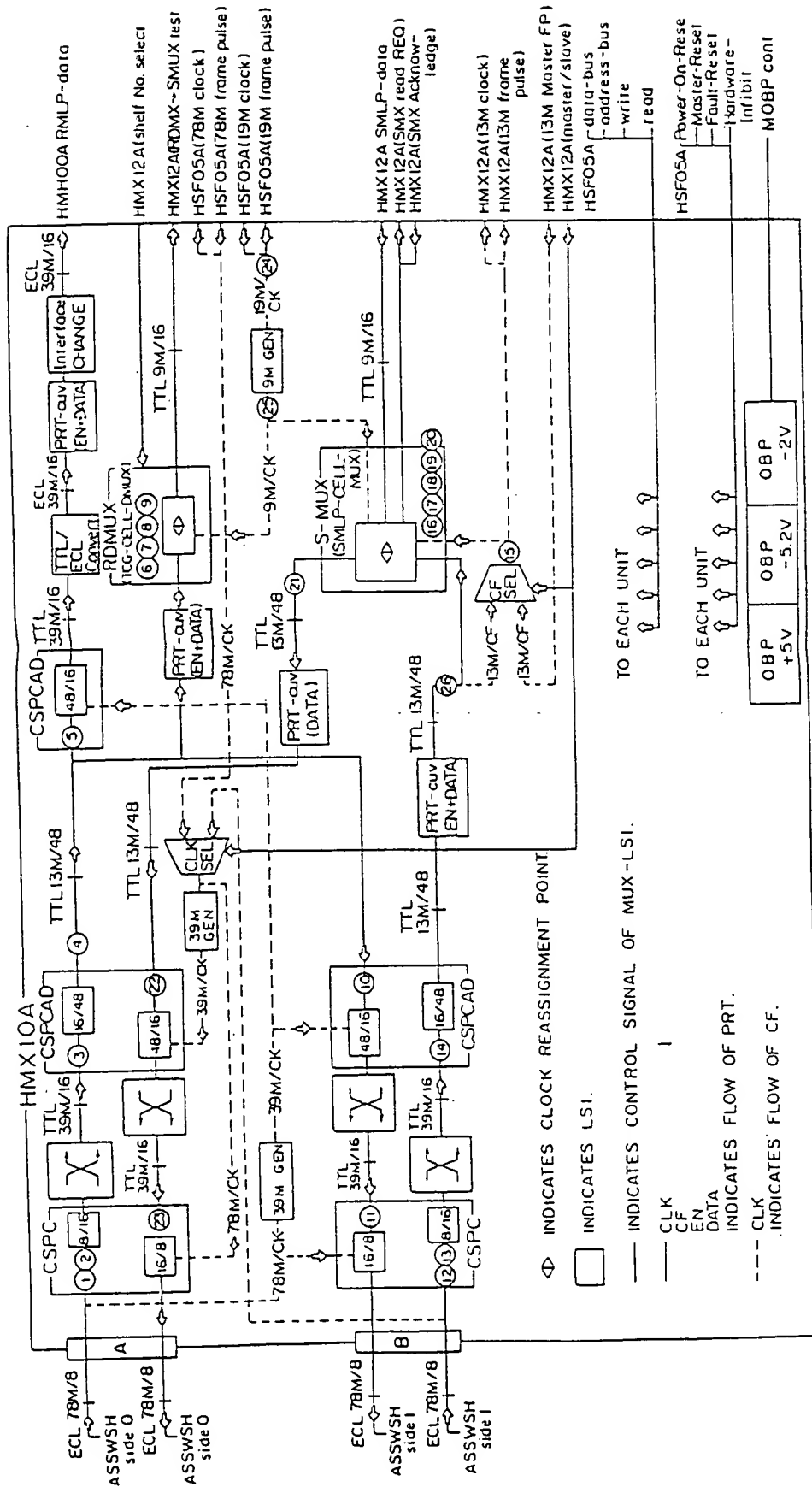


FIG. 364

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
CSINPC		ASSW(UPWARS DAISY CHAIN) ⇒ INPUT HW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSINCK		ASSW(UPWARS DAISY CHAIN) ⇒ INPUT HW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADINPC		ASSW(UPWARS DAISY CHAIN) ⇒ INPUT HW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
DXINCK		DMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
RADPC		RMLP SIDE CSPCAD INPUT PARITY CHECK (RMLP-CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
RDXPC		RTCG-DMUX INPUT PARITY CHECK (RTCG-DMUX INPUT) DATA+EN ODD PARITY	RTCG-DMUX INTERNAL MONITOR
TDXFIPC		RTCG-DMUX INTERNAL PARITY CHECK (RTCG-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	RTCG-DMUX INTERNAL MONITOR
TDXSLD 0		RTCG-DMUX CONGESTION STATE CHECK (P=0, CON=0) (RTCG-DMUX INTERNAL FIFO)	RTCG-DMUX INTERNAL MONITOR
TDXSLD 1		RTCG-DMUX CONGESTION STATE CHECK (P=0, CON=1) (RTCG-DMUX INTERNAL FIFO)	
TDXSLD 2		RTCG-DMUX CONGESTION STATE CHECK (P=1, CON=0) (RTCG-DMUX INTERNAL FIFO)	
TDXSLD 3		RTCG-DMUX CONGESTION STATE CHECK (P=1, CON=1) (RTCG-DMUX INTERNAL FIFO)	
TDXBFFL		RTCG-DMUX BUFFER-FULL CHECK (RTCG-DMUX INTERNAL FIFO)	RTCG-DMUX INTERNAL MONITOR
ADIMOPC		ASSW ⇒ DOWNWARD DAISY CHAIN PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSIMOPC		ASSW ⇒ DOWNWARD DAISY CHAIN PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSIMIPC		DOWNWARD DAISY CHAIN ⇒ ASSW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
CSIMICK		DOWNWARD DAISY CHAIN ⇒ ASSW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADIMIPC		DOWNWARD DAISY CHAIN ⇒ ASSW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
MXINCK		MUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 365

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
MXINPC		DOWNWARD DAISY CHAINAIN) \Rightarrow ASSW HIGH-SPEED PARITY CHECK (HIGH-SPEED INPUT) DATA+EN ODD PARITY	SMLP-MUX INTERNAL MONITOR EXCKUDING LOWEST ORDER SH
MXSPC		SMLP-MUX INPUT PARITY CHECK (SMLP-MUX INPUT) DATA+EN ODD PARITY	SMLP-MUX INTERNAL MONITOR
MXFIPC		SMLP-MUX INTERNAL PARITY CHECK (SMLP-MUX INTERNAL FIFO) DATA+EN ODD PARITY	CSPCAD INTERNAL MONITOR
MXSLD 0		SMLP \Rightarrow SMLP-MUX CONGESTION STATE CHECK (P=0,COM=0) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	SMLP-MUX INTERNAL MONITOR
MXSLD 1		SMLP \Rightarrow SMLP-MUX CONGESTION STATE CHECK (P=0,COM=1) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSLD 2		SMLP \Rightarrow SMLP-MUX CONGESTION STATE CHECK (P=1,COM=0) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSLD 3		SMLP \Rightarrow SMLP-MUX CONGESTION STATE CHECK (P=1,COM=1) (SMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXBFFL		SMLP \Rightarrow SMLP-MUX BUFFER-FULL CHECK (SMLP-MUX INTERNAL FIFO)	SMLP-MUX INTERNAL MONITOR
MXOCK		SMLP-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
ADOPC		SMLP-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSOPC		SMLP-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
19MCK		HSF05A \Rightarrow MASTER 19MHz CLOCK CHECK (19MHz CLOCK)	PWCB INTERNAL MONITOR
9MCK		PWCB INTERNAL ,ASTER 9MHz CLOCK CHECK (9MHz CLOCK)	PWCB INTERNAL MONITOR
SHXICK		SMUX INPUT 13 MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 366

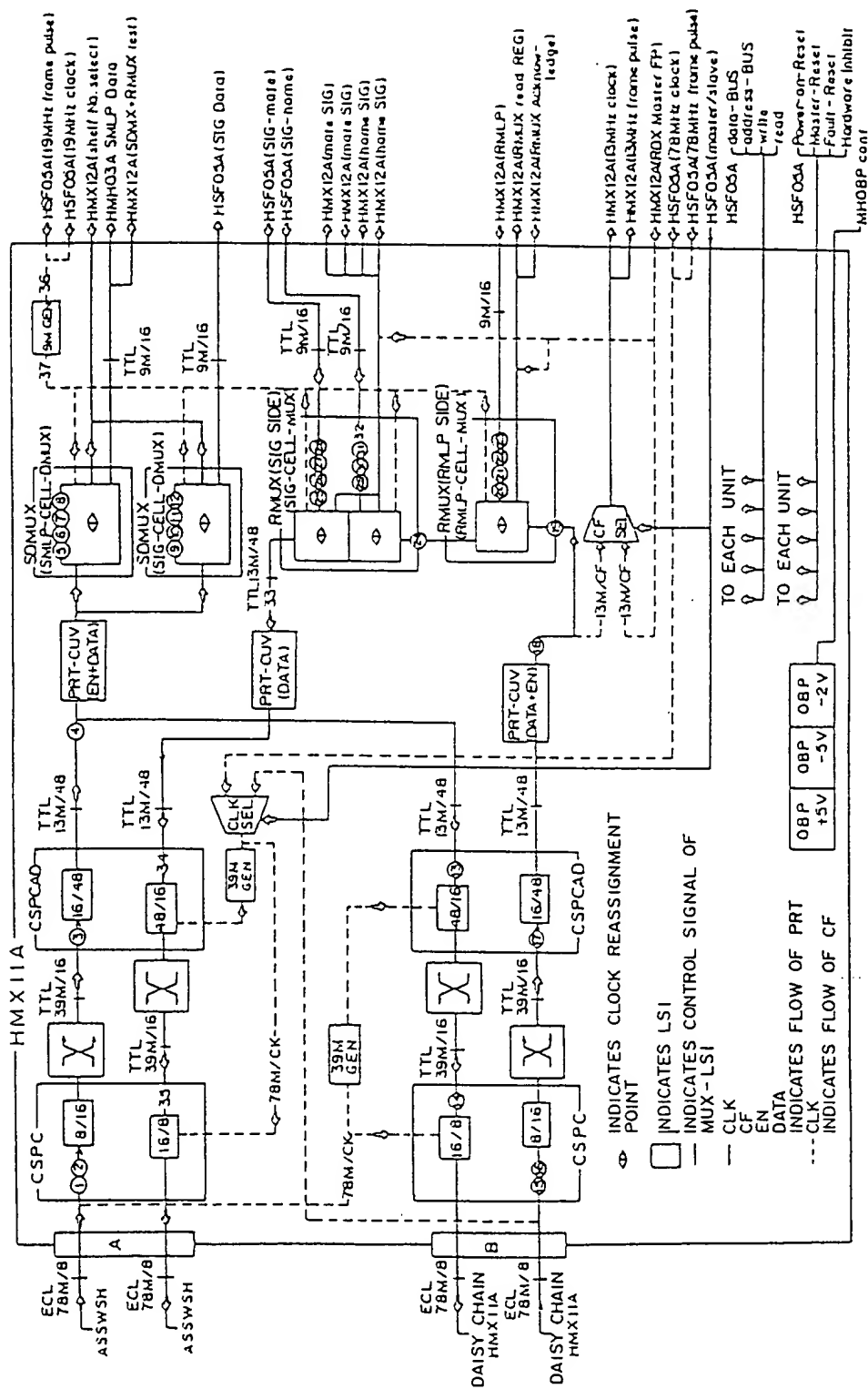


FIG. 367

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
CSINPC	①	ASSW (UPWARD DAISY CHAIN) ⇒ INPUT HW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSINCK	②	ASSW (UPWARD DAISY CHAIN) ⇒ INPUT HW 78MHz CLOCK (78MHz CLOCK) CHECK	CSPC INTERNAL MONITOR
ADINPC	③	ASSW (UPWARD DAISY CHAIN) ⇒ INPUT HW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
DXINCK	④	DMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
SDXINPC	⑤	SMLP-DMUX INPUT PARITY CHECK (SMLP-DMUX INPUT) DATA+EN ODD PARITY	SMLP-DMUX INTERNAL MONITOR
SDXFIPC	⑥	SMLP-DMUX INTERNAL PARITY CHECK (SMLP-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	SMLP-DMUX INTERNAL MONITOR
SDXSLD 0	⑦	SMLP-DMUX CONGESTION STATE CHECK (P=0, CON=0) (SMLP-DMUX INTERNAL FIFO)	SMLP-DMUX INTERNAL MONITOR
SDXSLD 1		SMLP-DMUX CONGESTION STATE CHECK (P=0, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SDXSLD 2		SMLP-DMUX CONGESTION STATE CHECK (P=1, CON=0) (SMLP-DMUX INTERNAL FIFO)	
SDXSLD 3		SMLP-DMUX CONGESTION STATE CHECK (P=1, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SDXBFFL	⑧	SMLP-DMUX BUFFER-FULL CHECK (SMLP-DMUX INTERNAL FIFO)	SMLP-DMUX INTERNAL MONITOR
SGDXIPC	⑨	SIG-DMUX INPUT PARITY CHECK (SMLP-DMUX INPUT) DATA+EN ODD PARITY	SIG-DMUX INTERNAL MONITOR
SGDXFIPC	⑩	SIG-DMUX INTERNAL PARITY CHECK (SMLP-DMUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-DMUX INTERNAL MONITOR
SGDXSLD 0	⑪	SIG-DMUX CONGESTION STATE CHECK (P=0, CON=0) (SMLP-DMUX INTERNAL FIFO)	SIG-DMUX INTERNAL MONITOR
SGDXSLD 1		SIG-DMUX CONGESTION STATE CHECK (P=0, CON=1) (SMLP-DMUX INTERNAL FIFO)	
SGDXSLD 2		SIG-DMUX CONGESTION STATE CHECK (P=1, CON=0) (SMLP-DMUX INTERNAL FIFO)	
SGDXSLD 3		SIG-DMUX CONGESTION STATE CHECK (P=1, CON=1) (SMLP-DMUX INTERNAL FIFO)	

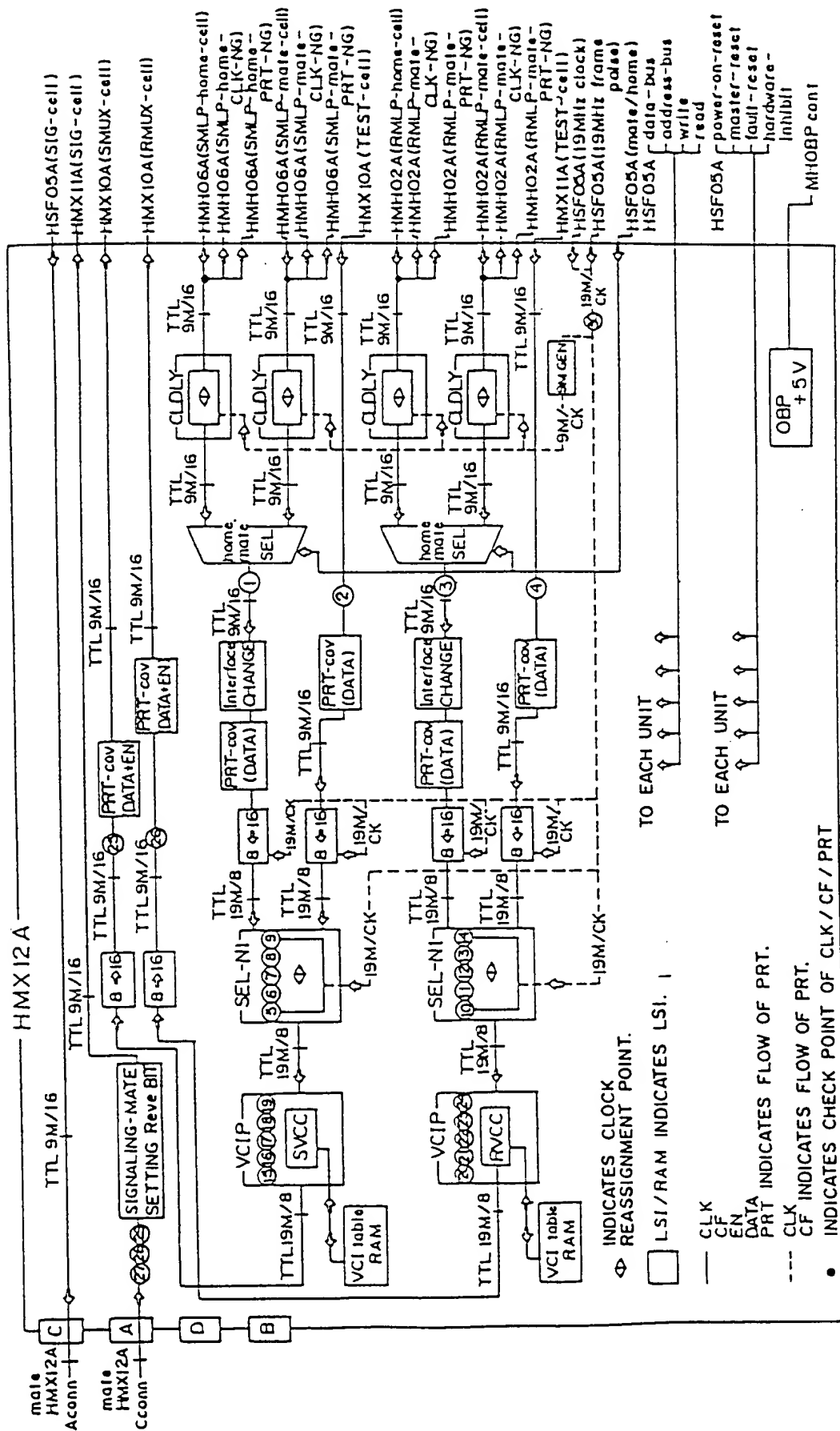
FIG. 368

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SGDXBFL	(12)	SIG-DMUX BUFFER-FULL CHECK (SMLP-MUX INTERNAL FIFO)	SIG-DMUX INTERNAL MONITOR
ADIMOPC	(13)	ASSW ⇒ DOWNWARD DAISY CHAIN PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSIMOPC	(14)	ASSW ⇒ DOWNWARD DAISY CHAIN PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
CSIMIPC	(15)	DOWNWARD DAISY CHAIN ⇒ ASSW PARITY CHECK (CSPC S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
CSIMICK	(16)	DOWNWARD DAISY CHAIN ⇒ ASSW 78MHz CLOCK CHECK (78MHz CLOCK)	CSPC INTERNAL MONITOR
ADIMIPC	(17)	DOWNWARD DAISY CHAIN ⇒ ASSW PARITY CHECK (CSPCAD S/P INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
RDXICK	(18)	RMUX INPUT 13MHz CLOCK CHECK (13MHz CLOCK)	PHCS INTERNAL MONITOR
MXIMPC	(19)	DOWNWARD DAISY CHAIN ⇒ ASSW HIGH-SPEED DATA PARITY CHECK (RMLP-MUX HIGH-SPEED INPUT) DATA+EN ODD PARITY	RMLP-MUX INTERNAL MONITOR EXCLUDING LOWEST ORDER SH
MXRPC	(20)	RMLP-MUX INPUT PARITY CHECK (RMLP-MUX INPUT) DATA+EN ODD PARITY	RMLP-DMUX INTERNAL MONITOR
MXFIPC	(21)	RMLP-MUX INTERNAL PARITY CHECK (RMLP-MUX INTERNAL FIFO) DATA+EN ODD PARITY	RMLP-DMUX INTERNAL MONITOR
MXSDL 0	(22)	RMLP-MUX CONGESTION STATE CHECK (P=0, CON=0) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	RMLP-MUX INTERNAL MONITOR
MXSDL 1		RMLP-MUX CONGESTION STATE CHECK (P=0, CON=1) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSDL 2		RMLP-MUX CONGESTION STATE CHECK (P=1, CON=0) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXSDL 3		RMLP-MUX CONGESTION STATE CHECK (P=1, CON=1) (RMLP-MUX LOW-SPEED INPUT INTERNAL FIFO)	
MXBFL	(23)	RMLP-MUX BUFFER-FULL CHECK (RMLP-MUX INTERNAL FIFO)	RMLP-MUX INTERNAL MONITOR
SGXXPC	(24)	RMLP-MUX ⇒ SIG-MUX HIGH-SPEED DATA PARITY CHECK (SIG-MUX HIGH-SPEED INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGX MPC	(25)	SIG(MATE)-MUX INPUT PARITY CHECK (SIG MATE-MUX INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR

FIG. 369

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SGXMFIPC	(26)	SIG(MATE)-MUX INTERNAL PARITY CHECK (SIG MATE-MUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXMSL 0	(27)	SIG(MATE)-MUX CONGESTION STATE CHECK (P=0, CON=0) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXMSL 1		SIG(MATE)-MUX CONGESTION STATE CHECK (P=0, CON=1) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXMSL 2		SIG(MATE)-MUX CONGESTION STATE CHECK (P=1, CON=0) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXMSL 3		SIG(MATE)-MUX CONGESTION STATE CHECK (P=1, CON=1) (SIG MATE-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXBFFL	(28)	SIG(MATE)-MUX BUFFER-FULL CHECK (SIG MATE-MUX INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXHPC	(29)	SIG(HOME)-MUX INPUT PARITY CHECK (SIG HOME-MUX INPUT) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXHFI PC	(30)	SIG(HOME)-MUX INTERNAL PARITY CHECK (SIG HOME-MUX INTERNAL FIFO) DATA+EN ODD PARITY	SIG-MUX INTERNAL MONITOR
SGXHSL	(31)	SIG(HOME)-MUX CONGESTION STATE CHECK (P=0, CON=0) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=0, CON=1) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=1, CON=0) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHSL		SIG(HOME)-MUX CONGESTION STATE CHECK (P=1, CON=1) (SIG HOME-MUX LOW-SPEED INPUT INTERNAL FIFO)	
SGXHBFFL	32	SIG(HOME)-MUX BUFFER-FULL CHECK (SIG HOME-MUX INTERNAL FIFO)	SIG-MUX INTERNAL MONITOR
MXOCK	33	SIG-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) 13MHz CLOCK CHECK (13MHz CLOCK)	PWCB INTERNAL MONITOR
ADOPC	34	SIG-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPCAD P/S INPUT) DATA ODD PARITY	CSPCAD INTERNAL MONITOR
CSOPC	35	SIG-MUX \Rightarrow ASSW(UPWARD DAISY CHAIN) PARITY CHECK (CSPC P/S INPUT) DATA ODD PARITY	CSPC INTERNAL MONITOR
19MCK	36	HSF05A \Rightarrow MASTER 19MHz CLOCK CHECK (19MHz CLOCK)	PWCB INTERNAL MONITOR
9MCK	37	PWCB INTERNAL MASTER 9MHz CLOCK CHECK (19MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 370

[illegible]

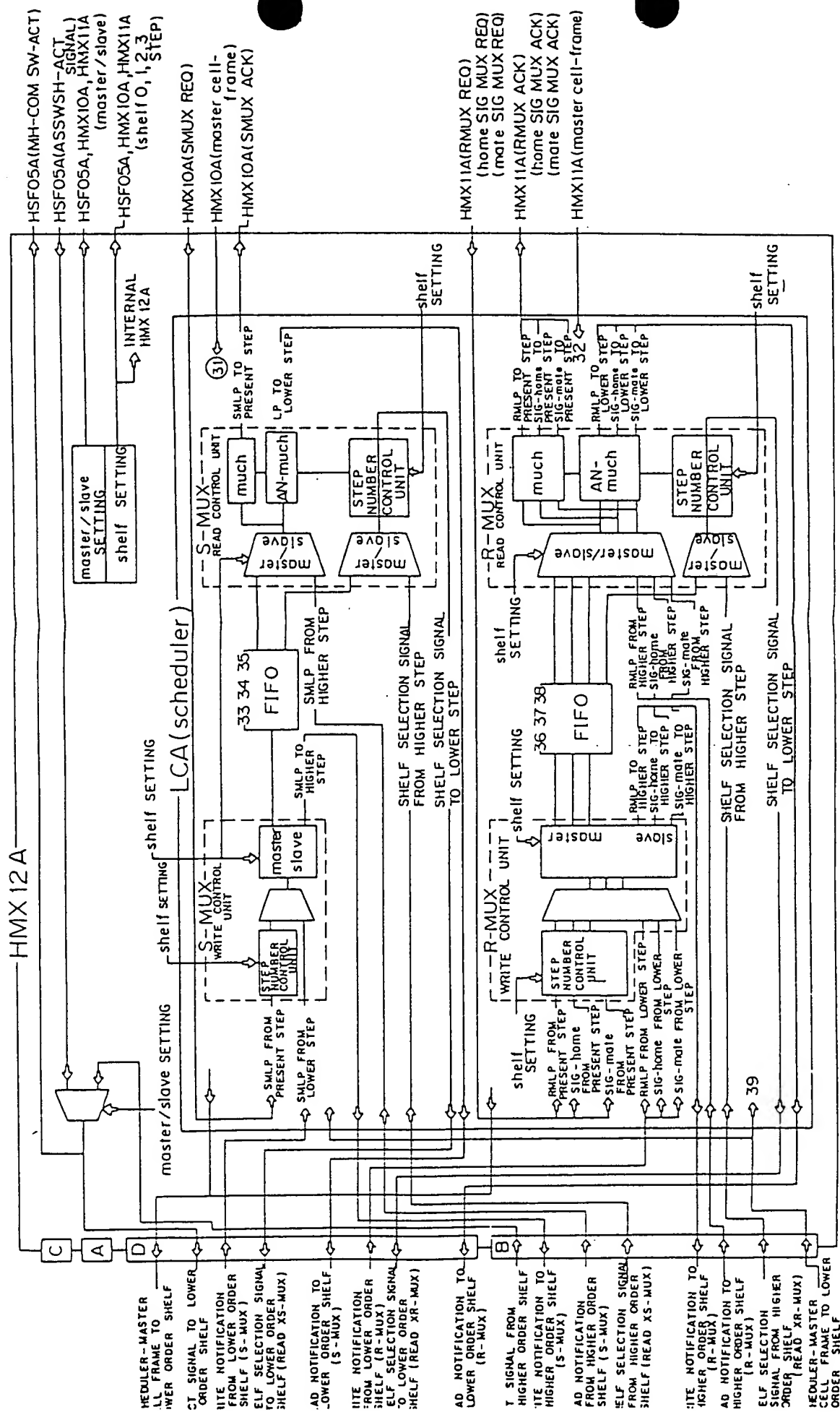


FIG. 372

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SN1PC	①	SMLP-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
STN1PC	②	STCG-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
RN1PC	③	RMLP-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
RTN1PC	④	RTCG-CELL DATA SEL-N1 INPUT PARITY CHECK DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
SN1MPC	⑤	SEL-N1 MEMORY PARITY CHECK (SMLP, STCG SEL-N1) DATA ODD PARITY	SEL-N1 INTERNAL MONITOR
SN1SL	⑥	SMLP SEL-N1 CONGESTION STATE CHECK (SMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
STN1SL	⑦	STCG SEL-N1 CONGESTION STATE CHECK (STCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
SN1BFFL	⑧	SMLP SEL-N1 BUFFER-FULL CHECK (SMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
STN1BFFL	⑨	STCG SEL-N1 BUFFER-FULL CHECK (STCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RN1MPC	⑩	SEL-N1 MEMORY PARITY CHECK (RMLP, RTCG SEL-N1) DATA ODD PARITY	SEL-N1 INTERNAL MONITOR
RN1SL	⑪	RMLP SEL-N1 CONGESTION STATE CHECK (RMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RTN1SL	⑫	RTCG SEL-N1 CONGESTION STATE CHECK (RTCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RN1BFFL	⑬	RMLP SEL-N1 BUFFER-FULL CHECK (RMLP-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
RTN1BFFL	⑭	RTCG SEL-N1 BUFFER-FULL CHECK (RTCG-SEL-N1 INTERNAL FIFO)	SEL-N1 INTERNAL MONITOR
SVCHDPC	⑮	SMLP VCIP INPUT DATA HEADER FIELD PARITY CHECK (SMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR

FIG. 373

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SVCDTPC		SMLP VCIP INPUT DATA PARITY CHECK (SMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
SVCTBPC		SMLP VCIP VCC-TABLE PARITY CHECK	VCIP INTERNAL MONITOR
SVCMP		SMLP VCIP VCC MEMORY CHECK	VCIP INTERNAL MONITOR
SVCALM		SMLP VCIP UNSET CELL ARRIVAL ALM	VCIP INTERNAL MONITOR
RVCHDPC		RMLP VCIP INPUT DATA HEADER FIELD PARITY CHECK (RMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
RVCDTPC		RMLP VCIP INPUT DATA PARITY CHECK (RMLP VCIP INPUT) DATA ODD PARITY	VCIP INTERNAL MONITOR
RVCTBPC		RMLP VCIP VCC-TABLE PARITY CHECK	VCIP INTERNAL MONITOR
RVCMP		RMLP VCIP VCC MEMORY CHECK	VCIP INTERNAL MONITOR
RVCALM		RMLP VCIP UNSET ARRIVAL ALM	VCIP INTERNAL MONITOR
SVCOPC		SMLP-VCIP ⇒ SMLP-MUX OUTPUT PARITY CHECK DATA ODD PARITY	PWCB INTERNAL MONITOR
RVCOPV		RMLP-VCIP ⇒ RMLP-MUX OUTPUT PARITY CHECK DATA ODD PARITY	PWCB INTERNAL MONITOR
LAPCK		LAP MATE SYSTEM CROSS-CONNECTION MASTER 9MHz CLOCK CHECK (SIGNALING-9M CLOCK)	PWCB INTERNAL MONITOR
LAPPC		LAP MATE SYSTEM CROSS-CONNECTION PARITY CHECK (SIGNALING-DATA) DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
SYFP		INTRA-SYSTEM PHASE MONITOR FRAME CHECK	PWCB INTERNAL MONITOR HIGHEST ORDER CH
19MCK		HSF05A ⇒ MASTER 19MHz CLOC CHECK (19MHz CLOCK)	PWCB INTERNAL MONITOR

FIG. 374

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
SHFP	31	SMLP MUX SCHEDULER MASTER FRAME CHECK (HMX 10A ⇒ HMX12A)	PWCB INTERNAL MONITOR
SHSGFP	32	RMLP, SIG MUX SCHEDULER MASTER FRAME CHECK (HMX11A ⇒ HMX12A)	PWCB INTERNAL MONITOR
SSHFI PC	33	SMLP MUX SCHEDULER FIFO PARITY CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
SSHCLT	34	SMLP MUX SCHEDULER CONTROL FAULT CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
SSHBFFL	35	SMLP MUX SCHEDULER FIFO FULL CHECK	SMLP-SCHEDULER-LCA INTERNAL MONITOR
RSHFI PC	36	RMLP, SIG MUX SCHEDULER FIFO PARITY CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
RSHCLT	37	RMLP SIG MUX SCHEDULER CONTROL FAULT CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
RSHBFFL	38	RMLP, SIG MUX SCHEDULER FIFO FULL CHECK	RMLP, SIG SCHEDULER LCA INTERNAL MONITOR
IMSYFP	39	INTER-DAISY-CHAIN PHASE SYNCHRONIZING MASTER FRAME CHECK	PWCB INTERNAL MONITOR

FIG. 375

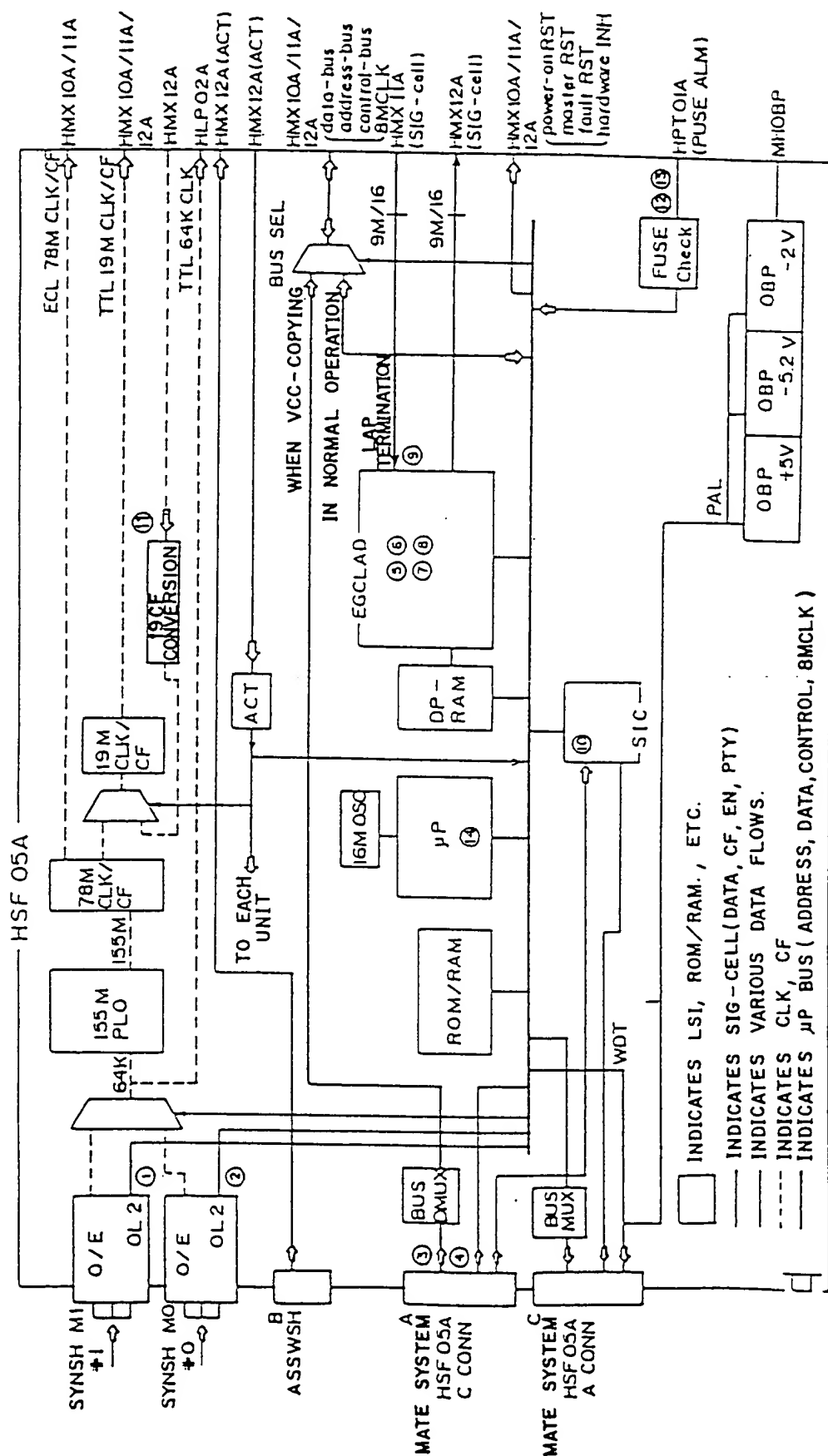
[illegible]

FIG. 376

MONITOR POINT NAME	POINT-NO	DETAILED FAULT MONITOR	REMARKS
OPTOCK		SYSTEM 0 OPTICAL 8MHz CLOCK CHECK (O# OL2)	PWCB INTERNAL MONITOR
OPTICK		SYSTEM 1 OPTICAL 8MHz CLOCK CHECK (1# OL2)	PWCB INTERNAL MONITOR
CR8MCK		MATE SYSTEM μ P 8MHz CLOCK CHECK	PWCB INTERNAL MONITOR
OBPALM		MATE SYSTEM OBP FAULT CHECK	PWCB INTERNAL MONITOR
EGINPC		EGCLAD SIGNALING-DATA INPUT PARITY CHECK (HMX11A \Rightarrow HSF05A) DATA+EN ODD PARITY	EGCLAD INTERNAL MONITOR
EGINMPC		EGCLAD INTERNAL MEMORY PARITY CHECK	EGCLAD INTERNAL MONITOR
EGEXNPC		EGCLAD EXTERNAL MEMORY PARITY CHECK	EGCLAD INTERNAL MONITOR
EGBFLL		EGCLAD BUFFER-FULL CHECK	EGCLAD INTERNAL MONITOR
EGEXPC		SIGNALING-DATA PWCB INPUT PARITY CHECK (HMX11A \Rightarrow HSF05A) DATA+EN ODD PARITY	PWCB INTERNAL MONITOR
SIPTC		INTER-SYSTEM COMMUNICATIONS PARITY, TIME-OUT CHECK	SIC INTERNAL MONITOR
SYFP		INTER-SYSTEM PHASE SYNCHRONIZATION FRAME CHECK (HLP02A \Rightarrow HSF05A)	PWCB INTERNAL MONITOR
FALM0		FUSE DISCONNECTION CHECK (HPT01A \Rightarrow HSF05A)	PWCB INTERNAL MONITOR
FALM1			
WDT0F		MATE SYSTEM WATCHDOG TIMER CHECK	μ P INTERNAL MONITOR

FIG. 377

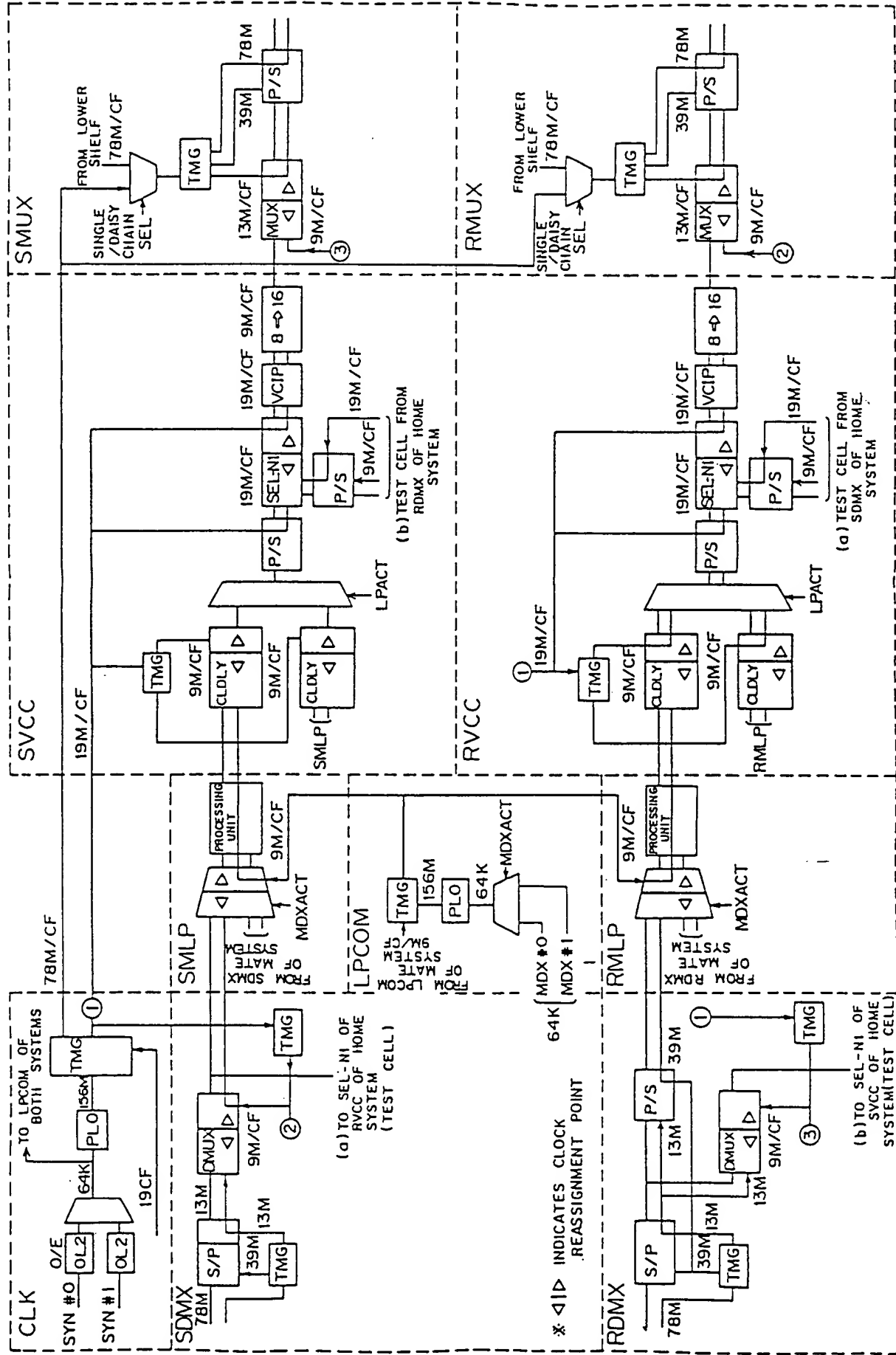


FIG. 378

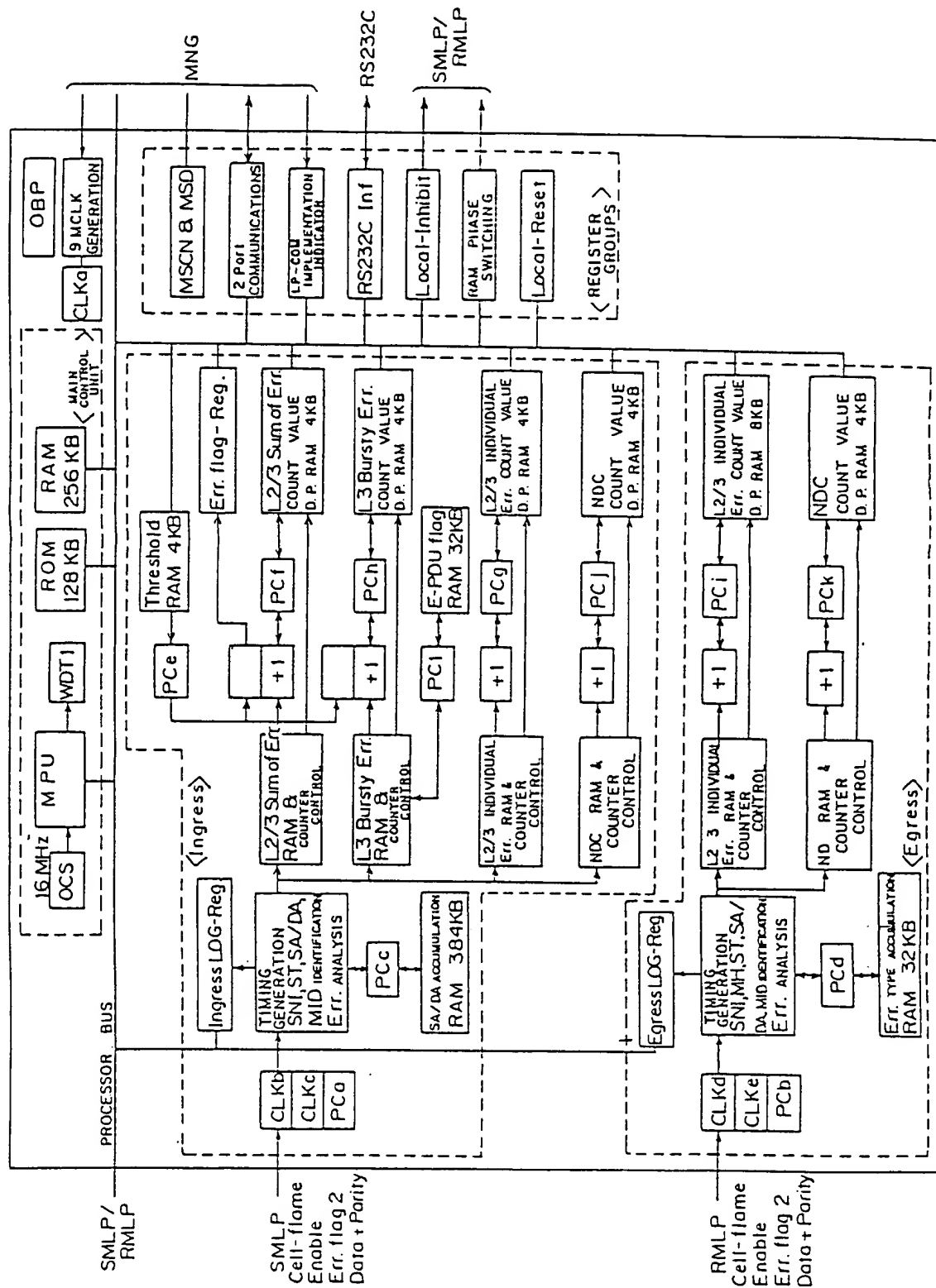


FIG. 379

BLOCK	F U N C T I O N	
MAIN CONTROL UNIT	MPU	16BIT MICROPROCESSOR (80C186-10)
	RAM	128K X 16 BIT SRAM FOR FIRMWARE WORK
	ROM	64K X 16 BIT EPROM FOR FIRMWARE STORAGE
	OCS	16 MHz OSCILLATOR
REGISTER GROUPS	MSCN & MSD	MSCN: AREA FOR USE IN REPORTING EACH CHECK NG (LISTED IN FIGURE 6.1.2) TO HLP02A
		MSD : AREA FOR USE IN SETTING PSEUDO-FAULT FROM HLP02A
	2PORT COMMUNICATIONS	ACTIVATING/RELEASING INTERRUPTION DURING COMMUNICATIONS WITH HLP02A
	LP-COM IMPLEMENTATION INDICATOR	INDICATING IMPLEMENTATION OF LP-COM AND OTHER PWCB (HLP02A AND HLM00A)
	RS232C INF	INTERFACE WITH WORK STATION FOR DEBUGGING
	LOCAL-INHIBIT	INITIAL STATE INDICATOR OF PM/TM COUNT VALUE STORAGE RAM
	RAM PHASE SWITCHING	INDICATOR OF HARDWARE ACCESS PHASE OF PM/TM COUNT VALUE STORAGE 2-PHASE RAM
	LOCAL-RESET	INTERNAL RESET
CLK GENERATION		GENERATING 9MCLK USING 19MCLK AND 19MFP FROM HLP02A
OBP		CONVERTING ON BOARD POWER -48V INTO +5V

FIG. 380

BLOCK	FUNCTION
INGRESS	COUNTING INGRESS L2/3 SUM OF ERROR, L2/3 INDIVIDUAL ERROR, L3 BURSTY ERROR, NETWORK DATA COLLECTION DERIVED ACCORDING TO TR774.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL FRAME (CF), AND ENABLE (EN) SIGNAL.
SNI, ST, SA/DA, MID IDENTIFICATION	IDENTIFYING SOURCE SNI, SEGMENT TYPE, SA/DA, MID AND MID FROM CELL DATA
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (FF) SIGNAL
INGRESS LOG-REG.	AREA FOR USE IN REPORTING ERROR TYPE, SOURCE SNI, SA, AND DA WHEN LOG OBJECT ERROR ARISES
SA/DA TYPE ACCUMULATION RAM	RAM FOR ACCUMULATING SA AND DA TO COLLECT LOG.
THRESHOLD RAM	FIRMWARE SETS THRESHOLD OF L2/3 SUM OF ERROR, AND NI AND NB OF L3 BURSTY ERROR AT INITIALIZATION
L2/3 SUM OF ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 SUM OF ERROR
ERR. FLAG-REG.	AREA FOR USE IN REPORTING TO FIRMWARE WHEN SUM OF ERROR COUNT VALUE EXCEEDS THRESHOLD
L3 BURSTY ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING L3 BURSTY ERROR PDU COUNT VALUE, ERRORED-PDU COUNT VALUE, INTERVAL COUNT VALUE, AND BAD INTERVAL COUNT VALUE
E-PDU FLAG RAM	RAM FOR USE IN COUNTING NUMBER OF ERRORED PDU OF L3 BURSTY ERROR
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF NETWORK DATA COLLECTION
EGRESS	COUNTING EGRESS L2/3 INDIVIDUAL ERROR AND NETWORK DATA COLLECTION DEFINED ACCORDING TO TR774.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL FRAME (CF), AND ENABLE (EN) SIGNAL.
SNI, MH, ST, SA/DA, MID IDENTIFICATION	IDENTIFYING DESTINATION SNI, SOURCE MH, SEGMENT TYPE, SA/DA, AND MID FROM CELL DATA
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (FF) SIGNAL
EGRESS LOG-REG.	AREA FOR USE INREPORTING ERROR TYPE, SOURCE SNI, SA, AND DA WHEN LOG OBJECT ERROR ARISES
ERR. TYPE ACCUMULATION RAM	ACCUMULATING ERROR TYPE FOR LOG COLLECTION
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM FOR STORING COUNT VALUE OF NETWORK DATA COLLECTION

FIG. 381

CHECK NAME	OBJECT OF CHECK
CL K a	DISCONNECTION CHECK OF 19M CLOCK AND FRAME PULSE FROM HLP02A
CL K b	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND CELL FRAME FROM SMLP
CL K c	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND ERROR FLAG 2 FROM SMLP
CL K d	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND CELL FRAME FROM RMLP
CL K e	DISCONNECTION CHECK OF INTERNALLY GENERATED 9M CLOCK AND ERROR FLAG 2 FROM RMLP
WD T I	TIMEOUT OF WATCHDOG TIMER, AND DISCONNECTION OF MPU OUTPUT 8M CLOCK
PC a	PARITY CHECK OF DATA AND ENABLE FROM SMLP
PC b	PARITY CHECK OF DATA AND ENABLE FROM RMLP
PC c	PARITY CHECK OF SA/DA ACCUMULATION RAM
PC d	PARITY CHECK OF ERROR TYPE ACCUMULATION RAM
PC e	PARITY CHECK OF THRESHOLD RAM
PC f	PARITY CHECK OF L2/3 SUM OF ERR. COUNT VALUE D.P. RAM
PC g	PARITY CHECK OF INGRESS L2/3 INDIVIDUAL ERR. COUNT VALUE D.P. RAM
PC h	PARITY CHECK OF L3 BURSTY ERR. COUNT VALUE D.P. RAM
PC i	PARITY CHECK OF EGRESS L2/3 INDIVIDUAL ERR. COUNT VALUE D.P. RAM
PC j	PARITY CHECK OF INGRESS NDC COUNT VALUE D.P. RAM
PC k	PARITY CHECK OF EGRESS NDC COUNT VALUE D.P. RAM
PC l	PARITY CHECK OF E-PDU FLAG RAM

F I G. 3 8 2

009220 000000

CHECK NAME	CHECK CONDITION
P C c	RECEIVING ERROR NOTIFICATION OF LOG REQUIRED ERROR FROM SMLP
P C d	CELL RECEIVED FROM RMLP IS SIP-BOM OR SIP-SSM
P C e	RECEIVING ERROR NOTIFICATION OF L2/3 SUM OF ERROR FROM SMLP
P C f	RECEIVING ERROR NOTIFICATION OF L2/3 SUM OF ERROR FROM SMLP
P C g	RECEIVING ERROR NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM SMLP
P C h	CELL RECEIVED FROM SMLP IS INTER-BOM (SIP-BOM OR SIP-SSM UNLESS ENCAPSULATED).
	RECEIVING ERROR NOTIFICATION OF L3 BURSTY ERROR THAT ERRORED-PDU SHOULD BE COUNTED
	$N1 = \text{PDU COUNT AS RESULT OF } N1 \text{ COMPARISON IN L3 BURSTY ERROR PROCESS}$
	$N1 \leq \text{ERRORED-PDU COUNT AS RESULT OF } N8 \text{ COMPARISON IN L3 BURSTY ERROR PROCESS}$
	CHECKING UNDER ANY OF FOUR ABOVE LISTED CONDITIONS
P C i	RECEIVING ERROR NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM RMLP
P C j	CELL RECEIVED FROM SMLP IS CELL OTHER THAN INTER-BOM.
	CELL RECEIVED FROM SMLP IS INTER-BOM (SIP-BOM OR SIP-SSM UNLESS ENCAPSULATED).
	RECEIVING ERROR NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM SMLP
	CHECKING UNDER ANY OF THREE ABOVE LISTED CONDITIONS
P C k	CELL RECEIVED FROM RMLP IS CELL OTHER THAN INTER-BOM
	CELL RECEIVED FROM RMLP IS SIP-BOM OR SIP-SSM.
	RECEIVING ERROR NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM RMLP
	CHECKING UNDER ANY OF THREE ABOVE LISTED CONDITIONS
P C l	CELL RECEIVED FROM SMLP IS EOM.

F I G. 3 8 3

66560-672260

GROUP	ITEM	Source	LEVEL	Check	Action	No
A	1	Maintenance	L3	MRI time out	Count Log	1
B	1	TR-772	L2	Busy Bit = 0	Stop	—
C	1	Maintenance	L2	HCS Violation	Stop Count	—
D	1	TR-772	L2	NCI ≠ 規定pattern	Stop	—
E	1	Maintenance	L2	Payload CRC Violation	Stop Count	2
F	1	Maintenance	L2	Payload Length Error	Stop Count	3
	2	Maintenance	L2	BOMs/SSMs with Invalid MIDs	Stop Count	4
G	1	Maintenance	L2	MID Currently Active	Stop Count	5
	2	Maintenance	L2	Unapproved MID	Stop Count	5
H	1	Maintenance	L2	Invalid Sequence Number	Stop Count	6
I	1	Maintenance	L3	Invalid SA Type	Stop Count	7
	2	Maintenance	L3	Invalid DA Type	Stop Count	8
J	1	Maintenance	L3	Invalid SMDS Address Type	Stop Count	9
K	1	Maintenance	L3	Individual DA Assign to Org. SNI	Stop Count	10
	2	Maintenance	L3	DA Field Format Error	Stop Count Log	11
	3	Maintenance	L3	SA Field Format Error	Stop Count Log	12
L	1	Maintenance	L3	Invalid BAsize Field Value	Stop Count Log	13
	2	NDC	L3	Access Class Violation	Stop Count Log	14
M	1	Maintenance	L3	Invalid HEL Field Value	Stop Count Log	15
	2	Maintenance	L3	Invalid HE- Carrier Selection	Stop Count Log	16
	3	Maintenance	L3	Invalid HE- Version	Stop Count Log	17
	4	NDC	L3	Exceed Max. Number of COU —	Stop Count Log	18
	5	NDC	L3	SA not Assigned to Org. SNI	Stop Count Log	19
	6	NDC	L3	DA Screening Violation	Stop Count Log	20
N	1	Maintenance	L3	BEtag Mismatch	Stop Count Log	21
	2	Maintenance	L3	Incorrect Length	Stop Count Log	22
	3	Maintenance	L3	BAsize Field ≠ Length Field	Stop Count Log	23
O	1	UNIQUE SPECIFICATION	--	MID Assigned Error	Stop Count	24
	2	UNIQUE SPECIFICATION	L3	End User Blocking	Stop Count	25

FIG. 384

Timing diagram showing the relationship between the 9M clock, cell frame, enable, and error notification signals. The diagram is divided into two sections: (0) to (11) and (25) to (26). The 9M clock is a periodic square wave. The cell frame signal is high from (0) to (11) and low from (25) to (26). The enable signal is high from (0) to (11) and low from (25) to (26). The error notification signal is high from (0) to (11) and low from (25) to (26).

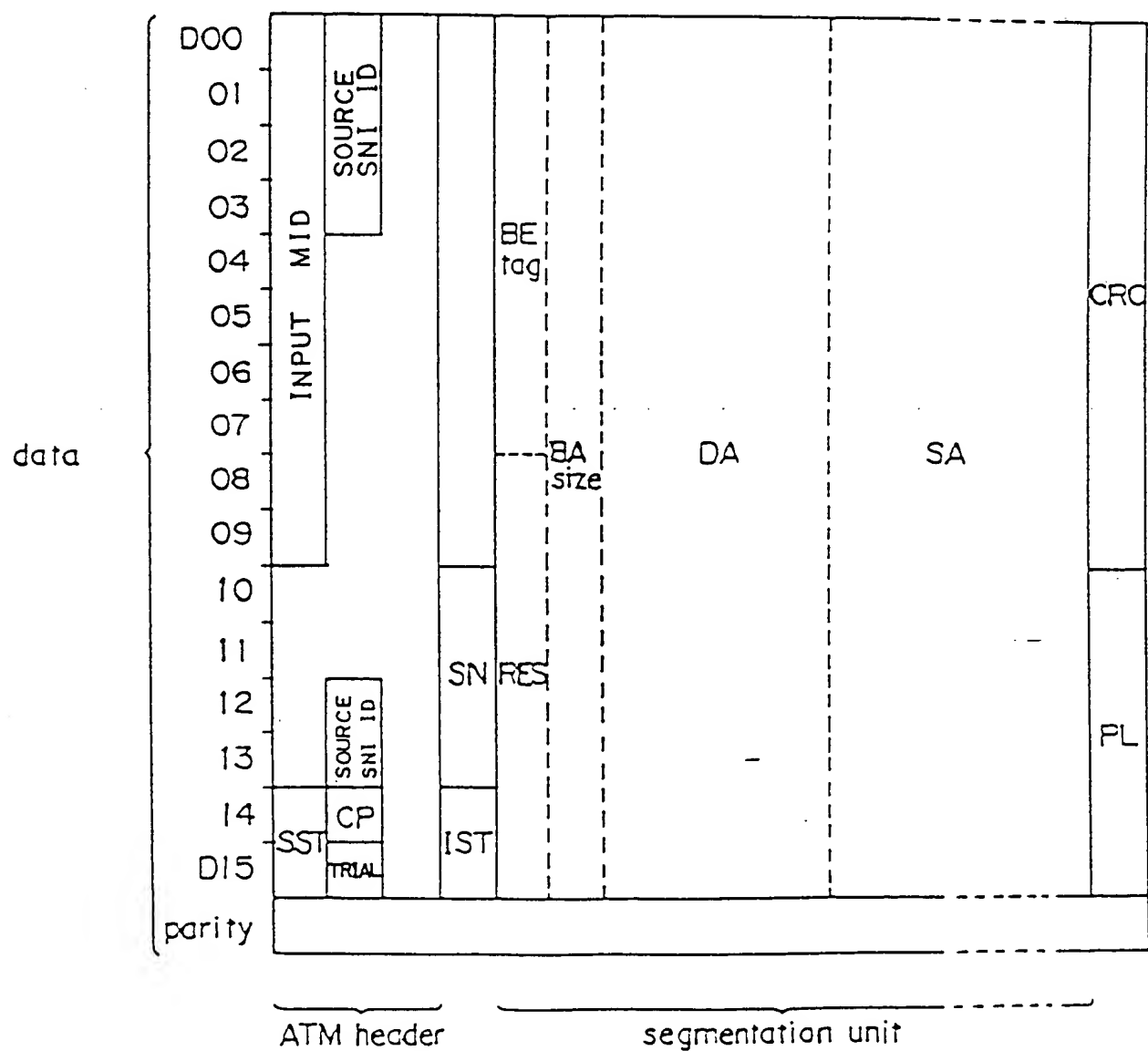


FIG. 385

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	—	ALL SIGNALS OTHER THAN BASIC CLOCK CHANGE AT RISE OF THIS CLOCK
CELL FRAME	⇒	LAST 1 τ OF SIGNAL CELL INDICATING BOUNDARY OF CELL ONLY INDICATES L
ENABLE	⇒	SIGNAL INDICATING VALID/INVALID OF CELL ENTIRE CELL AREA INDICATES L WHEN VALID
ERROR NOTIFICATION (2)	⇒	SIGNAL INDICATING ERROR TYPE DESCRIBED LATER IN DETAIL L INDICATES ERROR
DATA	POSITIVE	16 PARALLEL DATA + PARITY PARITY IS ODD PARITY IN TOTAL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE

FIG. 386

	SST	IST
Inter-BOM	1 0	1 0
SIP-BOM	1 0	(0 0)
COM	0 0	0 0
EOM	0 1	0 1
SIP-SSM	1 1	(0 1)

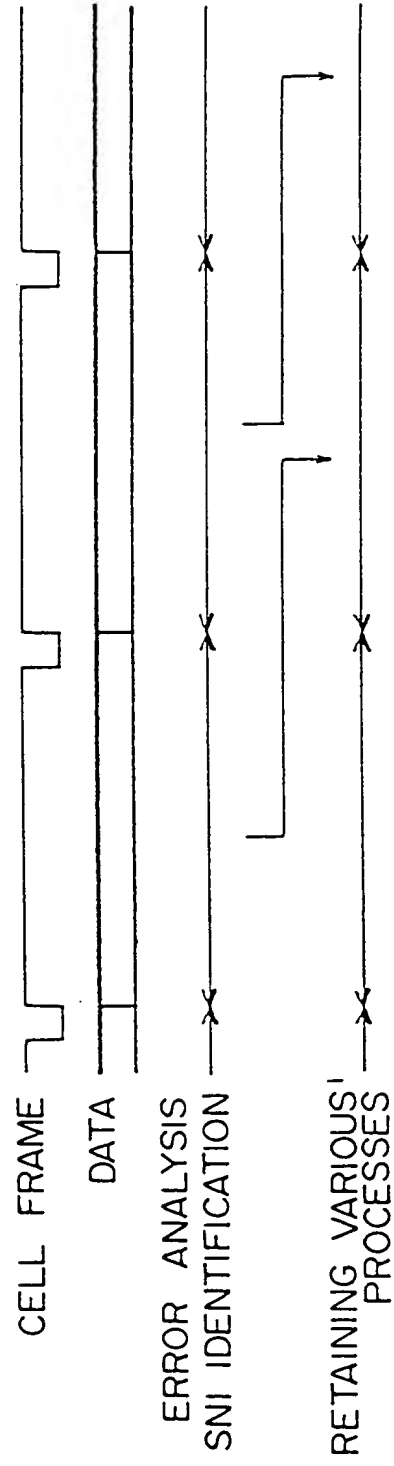
[illegible]

FIG. 388

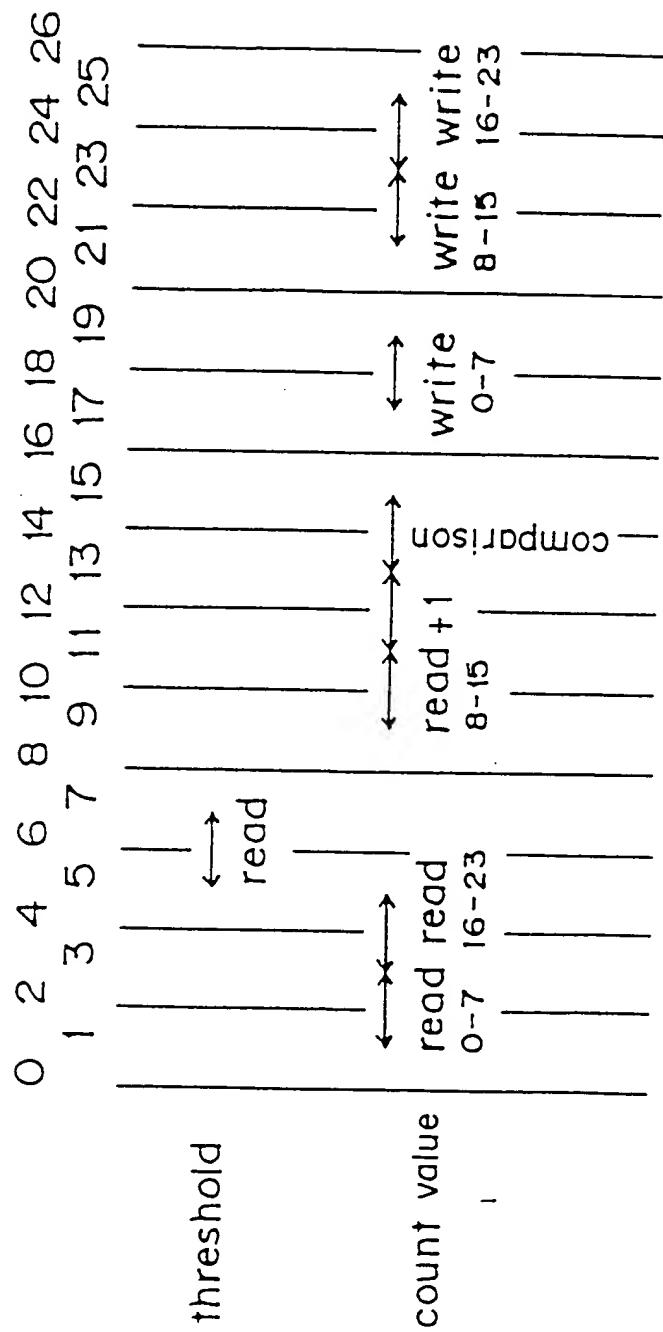


FIG. 389

1000
 900
 800
 700
 600
 500
 400
 300
 200
 100
 0

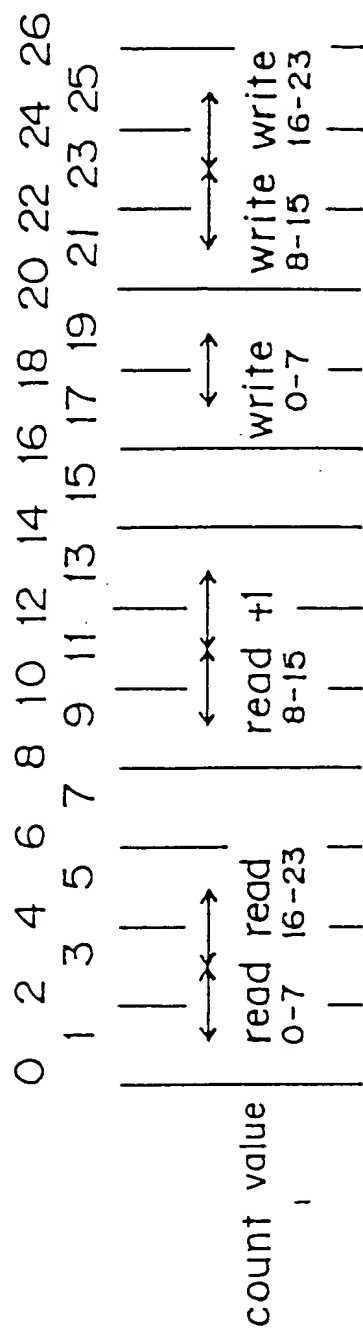


FIG. 390

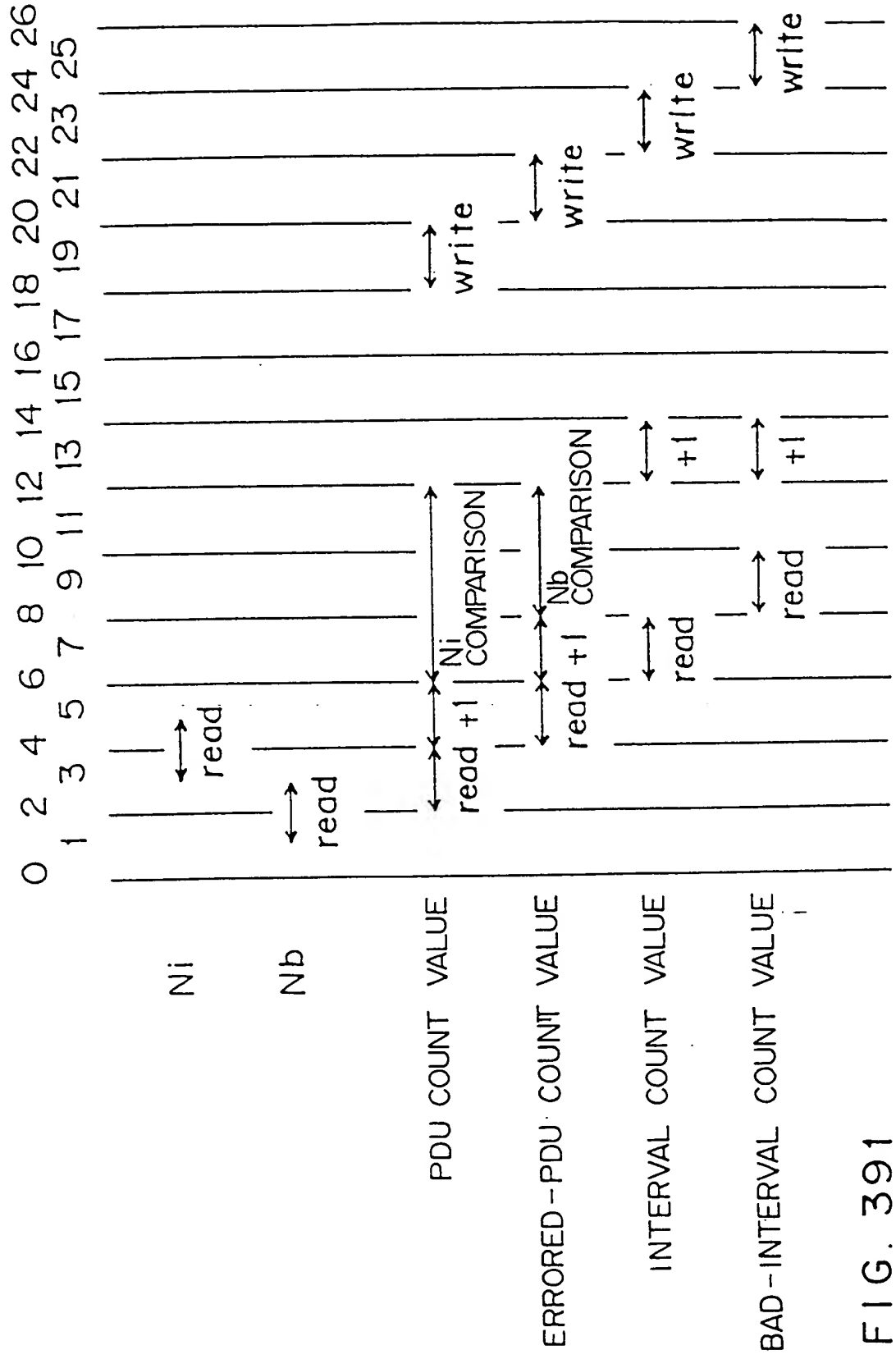


FIG. 391

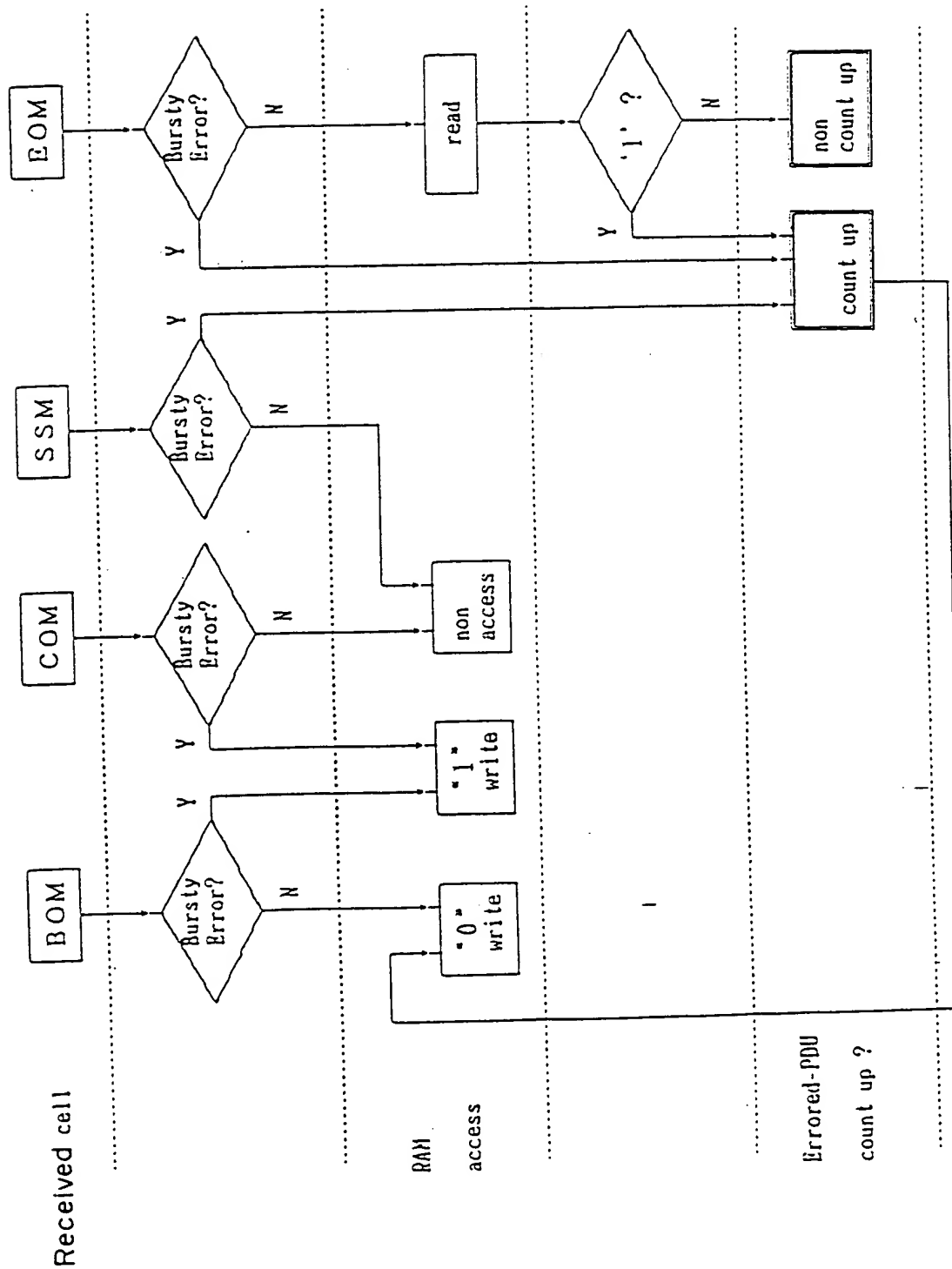


FIG. 392

GROUP	ITEM	SOURCE	LEVEL	CHECK	ACTION	NO
A	1	UNIQUE SPECIFICATION	L3	MRI TIME OUT	COUNT	1
	2	UNIQUE SPECIFICATION	DEST. EQUAL TO ORG. SNI	—	2
B	1	UNIQUE SPECIFICATION	L2	PAYLOAD CRC VIOLATION	STOP COUNT	3
C	1	UNIQUE SPECIFICATION	L2	MID CURRENTLY ACTIVE	STOP COUNT	4
D	1	UNIQUE SPECIFICATION	L2	INVALID SEQUENCE NUMBER	STOP COUNT	5
E	1	NDC	L3	SA SCREENING VIOLATION	STOP COUNT LOG	6
	2	NDC	L3	DEST. SNI NOT AVAILABLE	STOP COUNT LOG	7
F	1	NDC	L3	EXCEED MAX. NUMBER OF CDU	STOP COUNT LOG	8
G	1	UNIQUE SPECIFICATION	L3	BETAG MISMATCH	STOP COUNT	9
H	1	UNIQUE SPECIFICATION	MID ASSIGNED ERROR	COUNT	10
I	1	UNIQUE SPECIFICATION	ENCAPSULATION ERROR	COUNT	11

FIG. 393

669660-612260

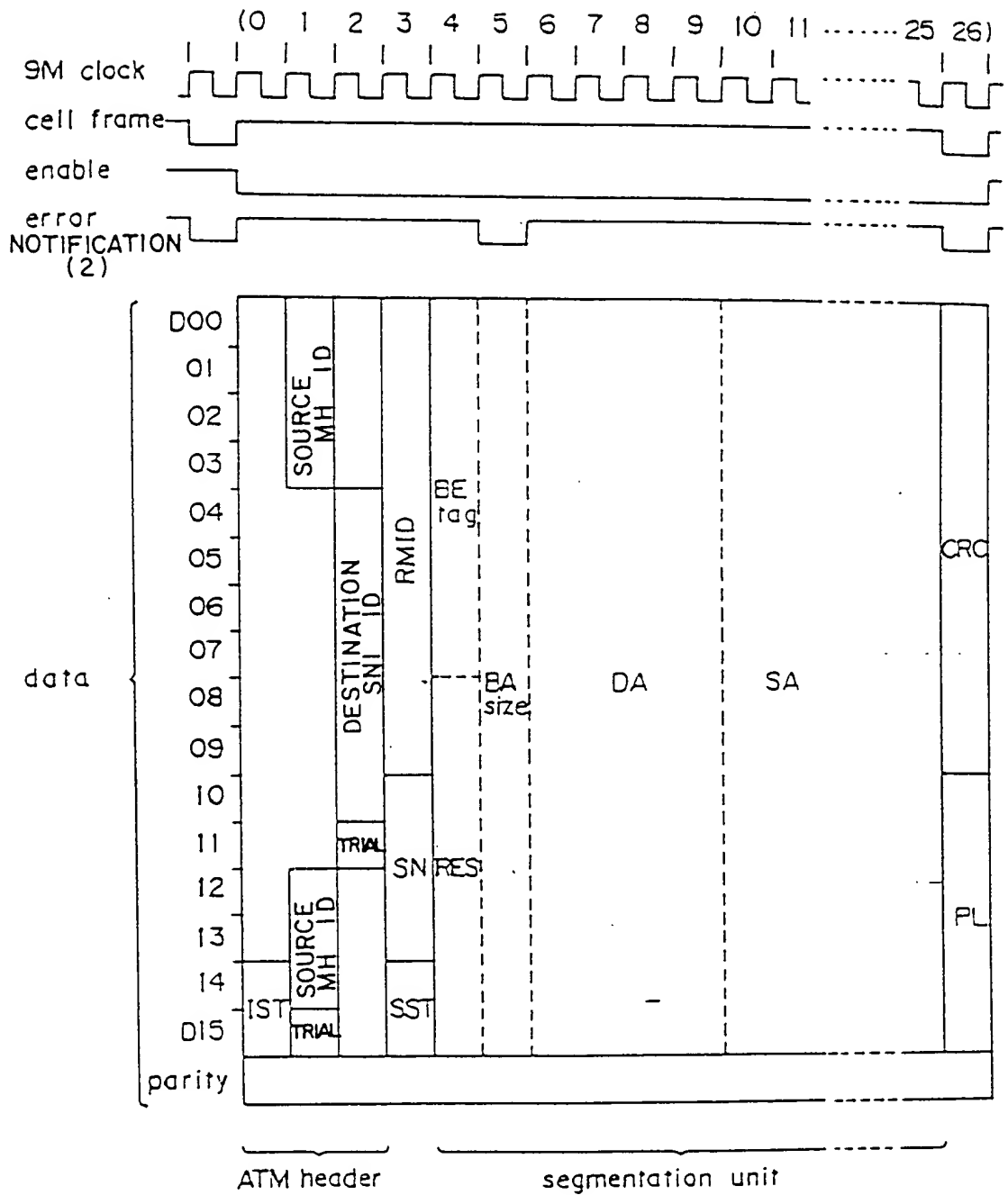


FIG. 394

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	—	ALL SIGNALS OTHER THAN BASIC CLOCK CHANGE AT RISE OF THIS CLOCK
CELL FRAME	⇒	LAST 12 OF SIGNAL CELL INDICATING BOUNDARY OF CELL ONLY INDICATES L.
ENABLE	⇒	SIGNAL INDICATING VALID/INVALID OF CELL ENTIRE CELL AREA INDICATES L WHEN VALID.
ERROR NOTIFICATION	⇒	SIGNAL INDICATING ERROR TYPE DESCRIBED LATER IN DETAIL.
DATA	+	16 PARALLEL DATA + PARITY ODD PARITY IN TOTAL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE.

FIG. 395

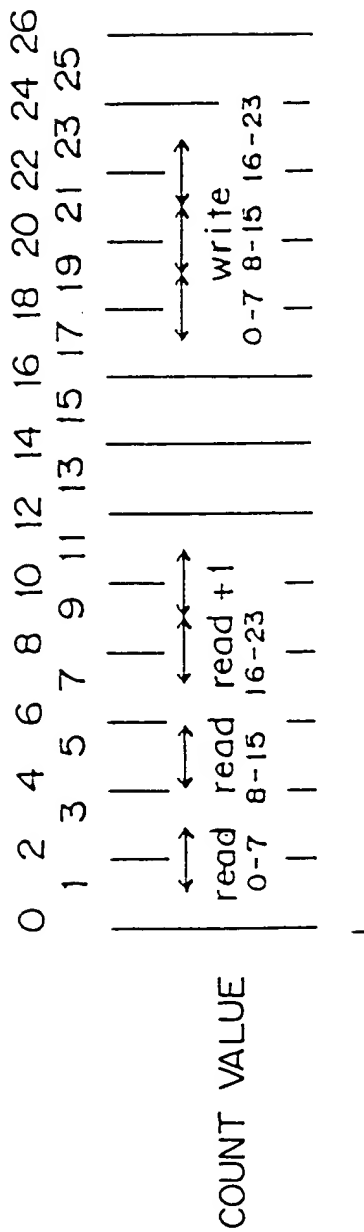


FIG. 397

66320-ETZ00

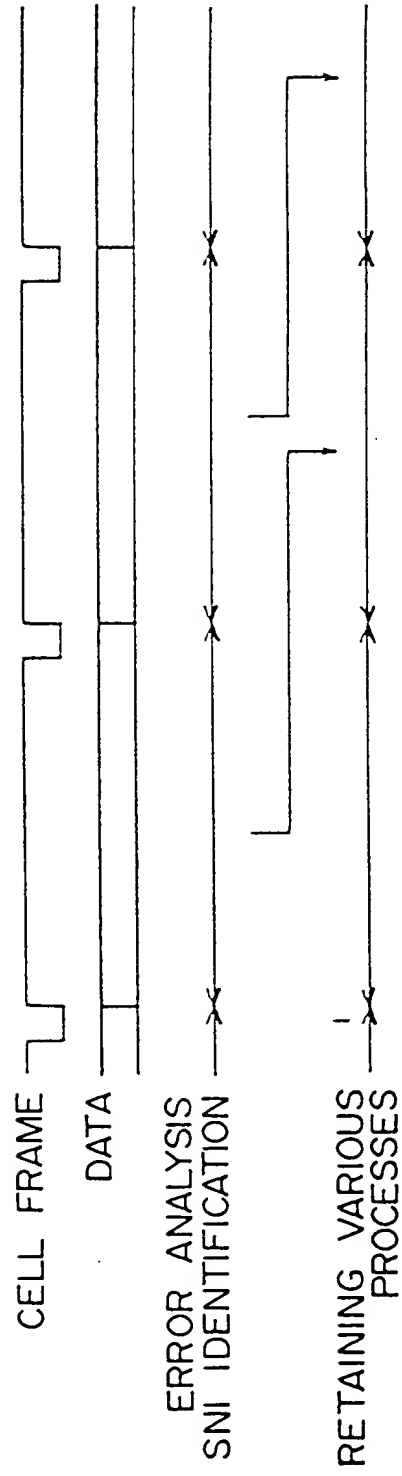


FIG. 398

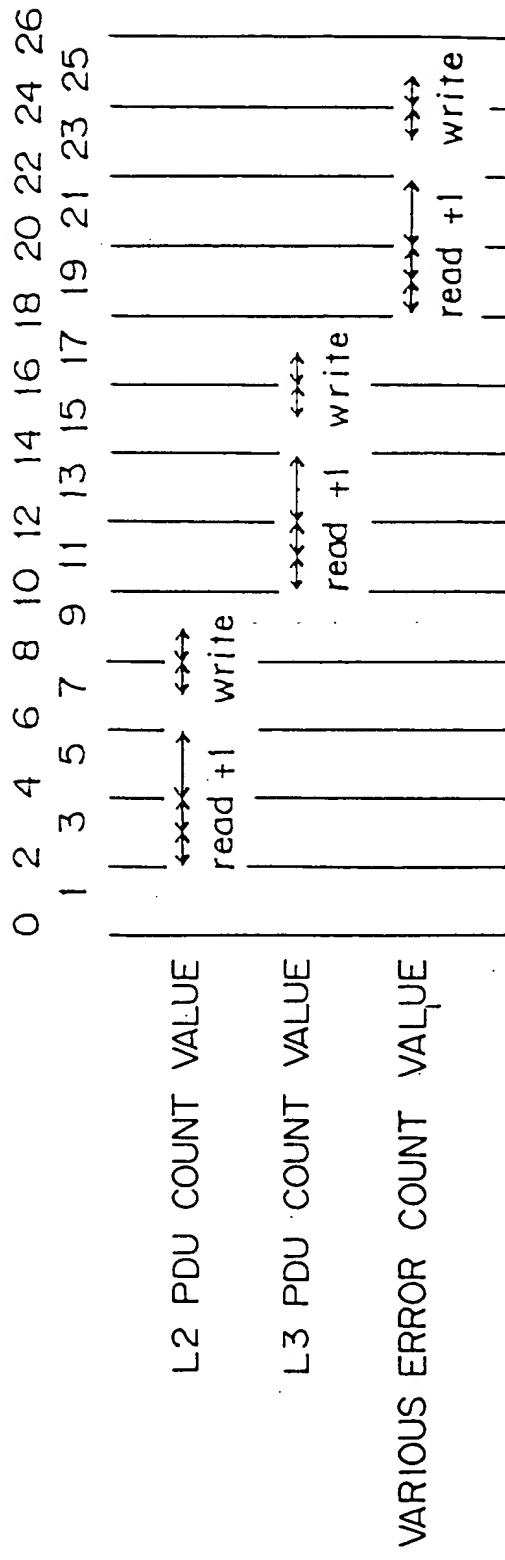


FIG. 399

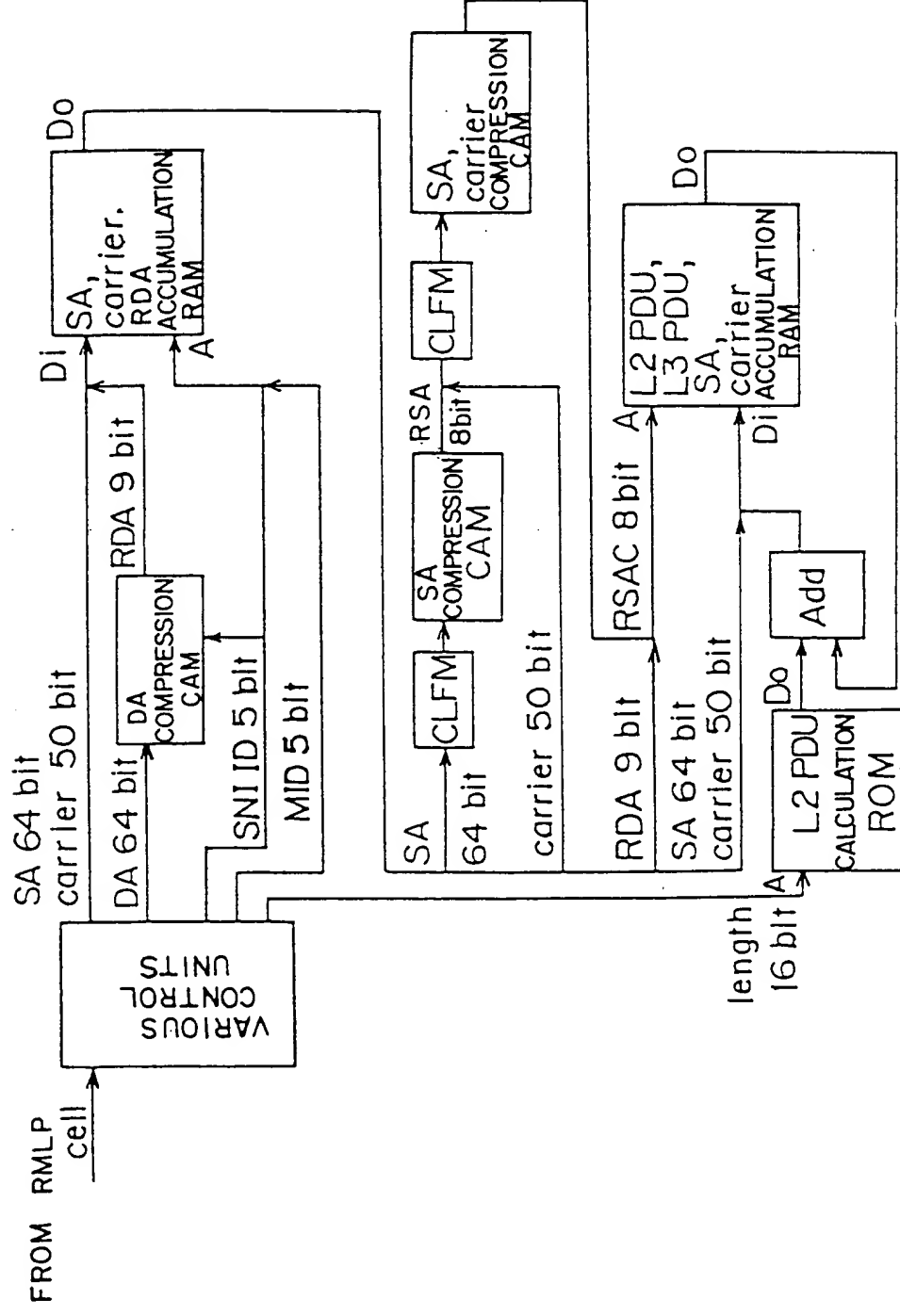
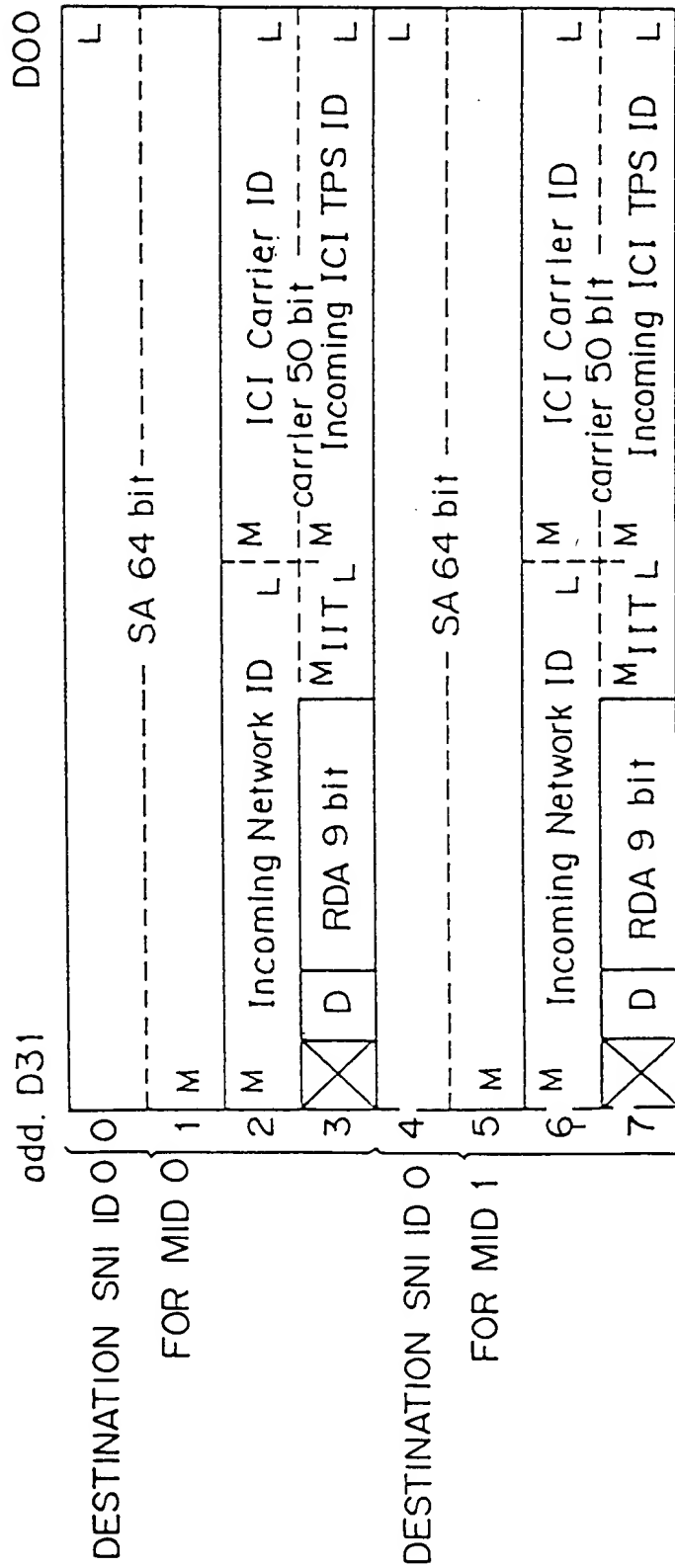


FIG. 400

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0													M	MID				L
1																		
2					M	SNI-ID								L				
3																		
4																		
5																		
6																		
7																		
8																		
9																		
10																		
11																		
12																		
13																		
14																		
15																		
16																		
17																		
18																		
19																		
20																		
21																		
22					M	IIT				L								
23					M	ICI Carrier ID											L	
24					M	Incoming Network ID											L	
25					M	Incoming ICI TPS ID											L	
26																		

—



OMITTED FOR SUBSEQUENT DATA (HIGHER ORDER ADDRESS
FOR DESTINATION SNI ID, LOWER FOR MID)

FIG. 402

00000000000000000000000000000000

RDA	
SNI ID 0	0 ← DA 64 bit (IA 1) →
	1 ← DA 64 bit (IA 2) →
	7 ← DA 64 bit (IA 8) →
	8 ← DA 64 bit (GA 1) →
	9 ← DA 64 bit (GA 2) →
	F ← DA 64 bit (GA 8) →
SNI ID F	F0 ← DA 64 bit (IA 1) →
	F1 ← DA 64 bit (IA 2) →
	F7 ← DA 64 bit (IA 8) →
	F8 ← DA 64 bit (GA 1) →
	F9 ← DA 64 bit (GA 2) →
	FF ← DA 64 bit (GA 8) →
SNI ID 10	100 ← DA 64 bit (IA 1) →
	101 ← DA 64 bit (IA 2) →
	107 ← DA 64 bit (IA 8) →
	108 ← DA 64 bit (GA 1) →
	109 ← DA 64 bit (GA 2) →
	10F ← DA 64 bit (GA 8) →
SNI ID 1F	1F0 ← DA 64 bit (IA 1) →
	1F1 ← DA 64 bit (IA 2) →
	1F7 ← DA 64 bit (IA 8) →
	1F8 ← DA 64 bit (GA 1) →
	1F9 ← DA 64 bit (GA 2) →
	1FF ← DA 64 bit (GA 8) →

FIG. 403

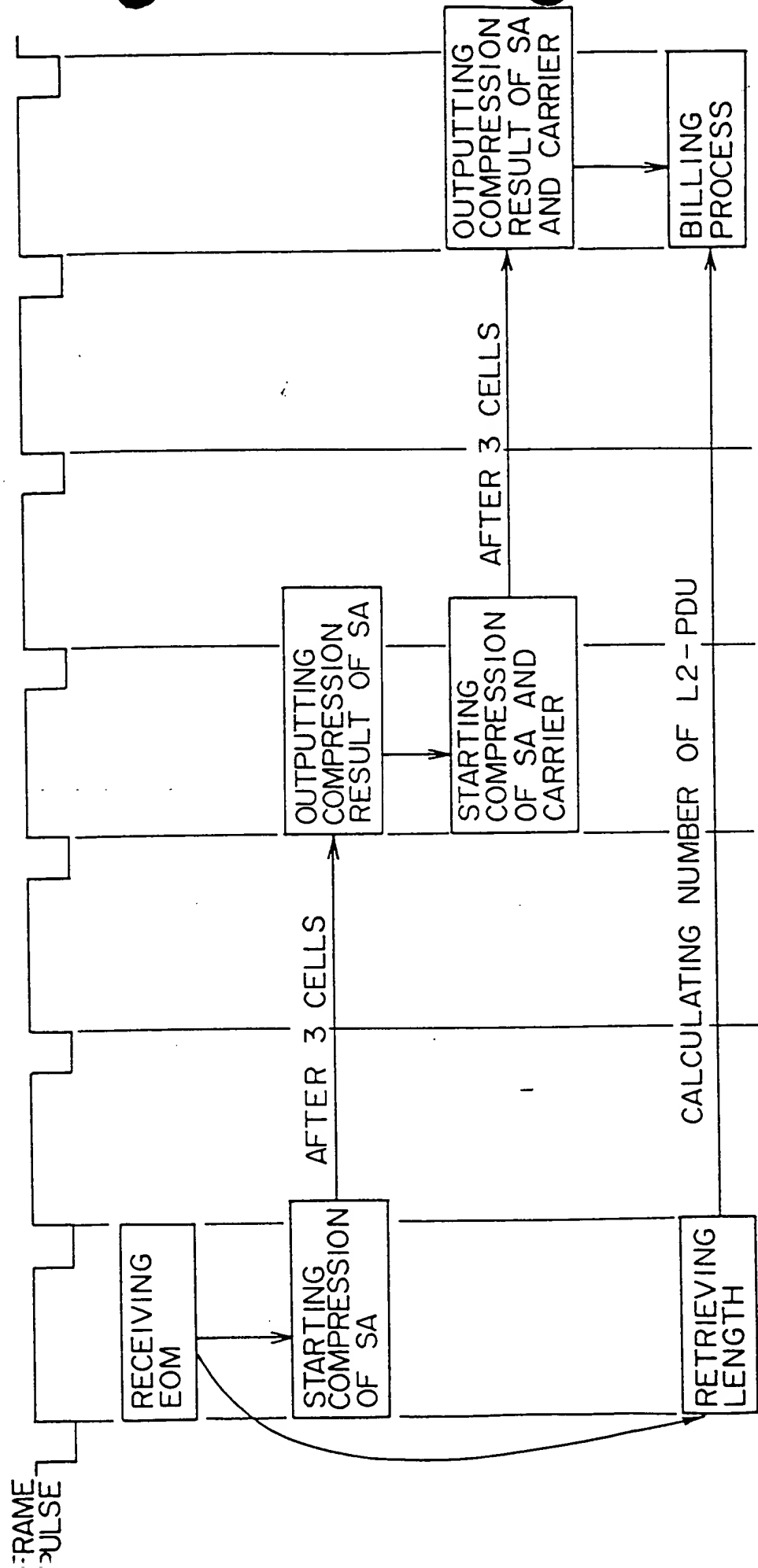


FIG. 404

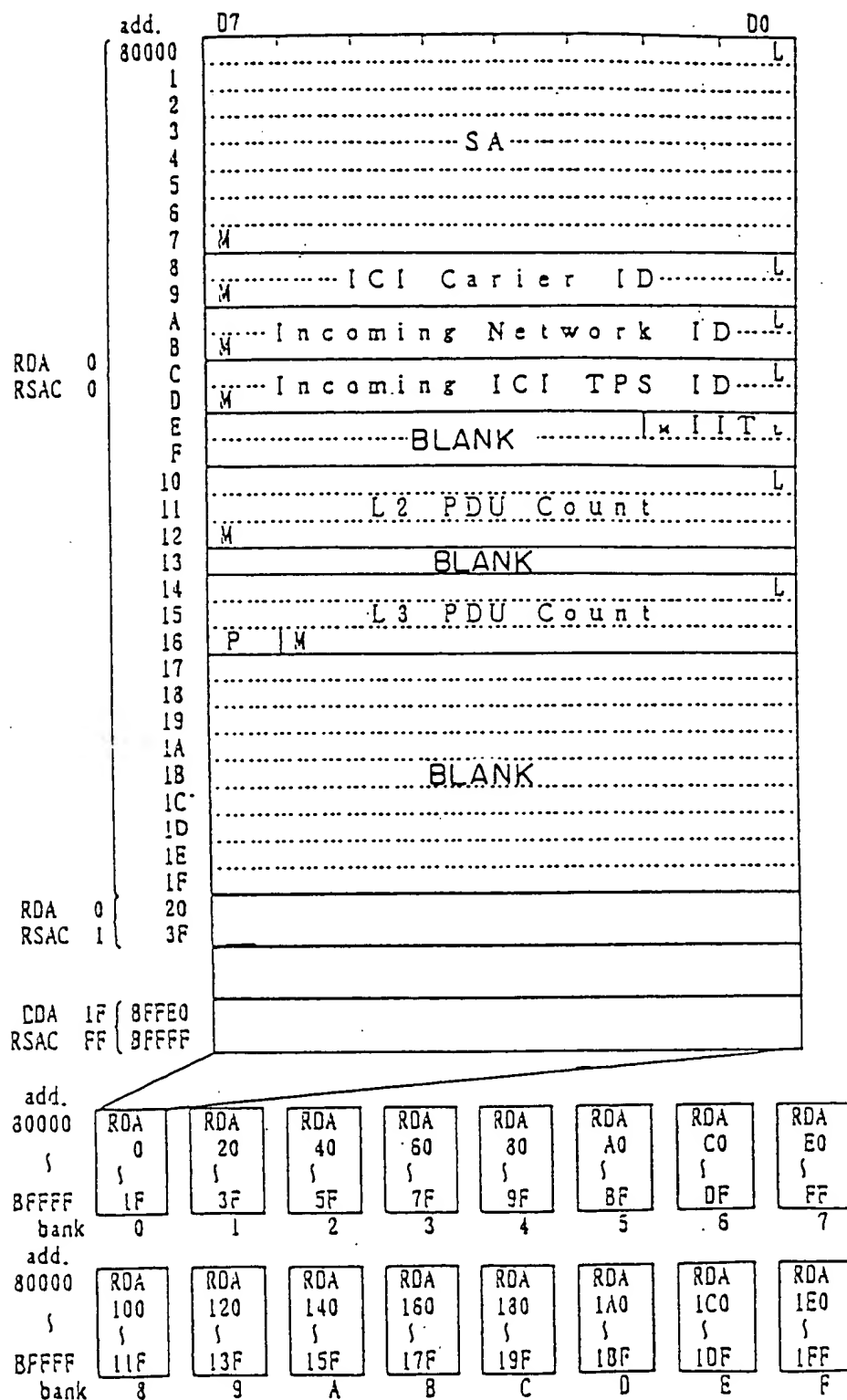
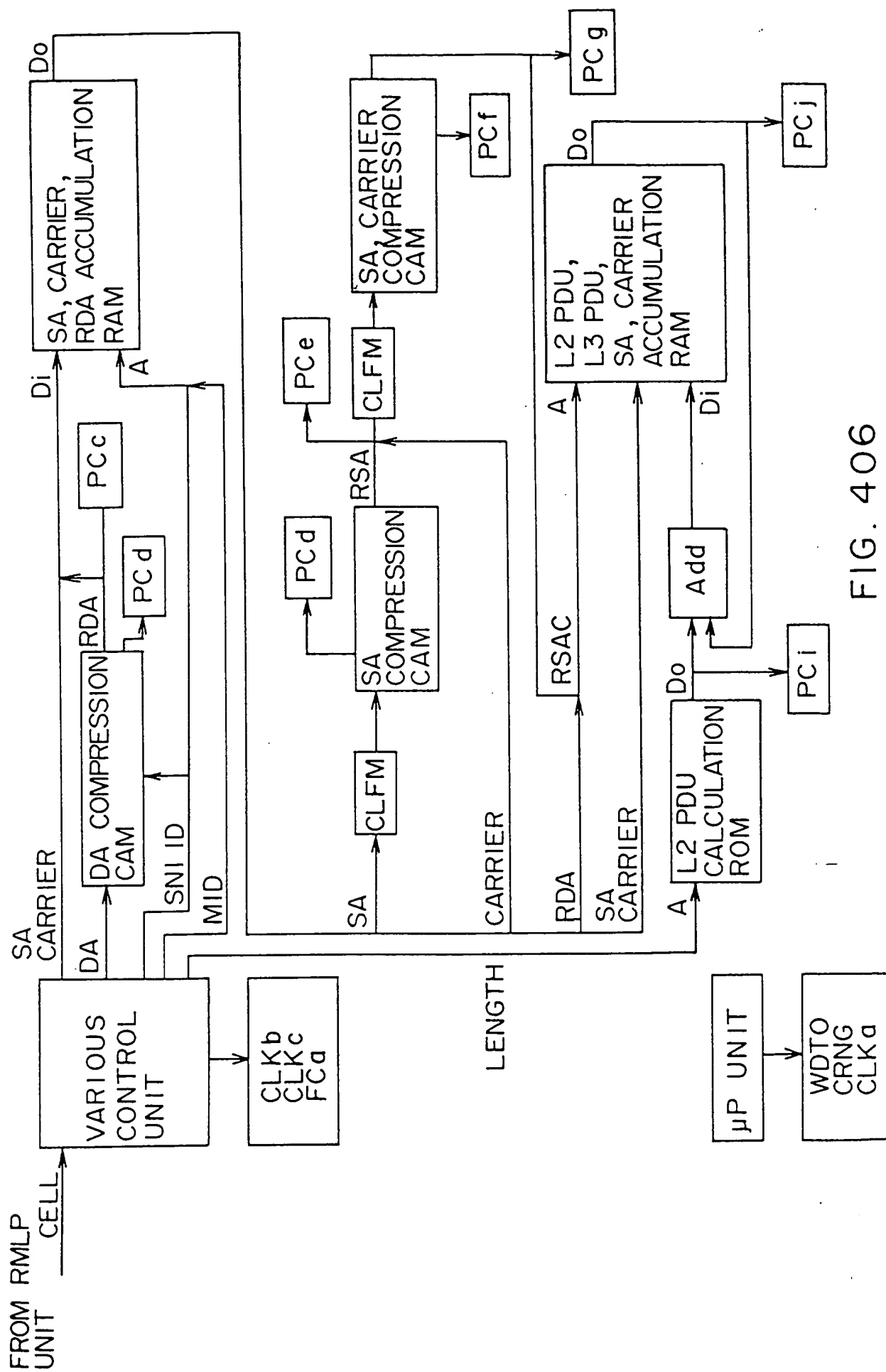


FIG. 405



[illegible]

FIG. 407

BLOCK NAME	FUNCTION
16M	GENERATING 16 MHZ CLOCK FOR MICROPROCESSOR
MPU	μP (80C186)
ROM	STORING FIRMWARE FOR MPU
FOR SENDING T-CELL	TEST CELL SENDING MEMORY
FOR RECEIVING T-CELL	TEST CELL RECEIVING MEMORY
T-CELL LCA	SENDING TEST CELL FOR HMH01A AND 03A (ASSIGNING ODD PARITY AND ADJUSTING TIMIGN), RECEIVING TEST CELL, MAKING PARITY CHECK, ETC.
SRAM	WORK MEMORY FOR MPU
2-PORT SENDING SRAM MNG \rightarrow MSR	DATA SENDING MEMORY FOR MSR-FIRM
2-PORT RECEIVING SRAM MNG \leftarrow MSR	DATA RECEIVING MEMORY FROM MSR-FIRM
2-PORT SENDING SRAM MNG \rightarrow ACC	DATA SENDING MEMORY FOR ACC-FIRM
2-PORT RECEIVING SRAM MNG \leftarrow ACC	DATA RECEIVING MEMORY FROM ACC-FIRM
PIF inf	CONTROLLING INTERFACE WITH PIF (SBIF-LSI)
FOR COMMAND MEMORY	SRAM FOR SENDING COMMAND
FOR RESPONSE MEMORY	SRAM FOR RECEIVING RESPONSE
S-CTL LCA	COMMAND AND RESPONSE CONTROL FOR LP
STATE CONTROL	CONTROLLING ACT, INHBIT, ETC. OUS CONTROL TO MATE SYSTEM
SEL	SELECTING 64 KHZ CLOCK FROM MH-COM OF HOME AND MATE SYSTEMS
PLO	GENERATING 155 MHZ CLOCK IN SYNCHRONISM WITH 64 KHZ CLOCK
TMG	GENERATING 78 MHZ AND 19 MHZ CLOCKS FROM 155 MHZ CLOCK

FIG. 408

7	6	5	4	3	2	1	0
0	0	0	TAGA			0	0
UL	TAGC		TAGB			COM	SIG
VPI							
VPI				VCI			
VCI							
VCI							

FIG. 410

7 6 5 4 3 2 1 0

	0	
VPI		
VPI	VCI	
VCI		
VCI		
ST	SN	MID
MID		

FIG. 411

7 6 5 4 3 2 1 0

	0	
VPI		
VPI	VCI	
VCI		
VCI		
ST	SN	MID
MID		

FIG. 412

663620-6744660

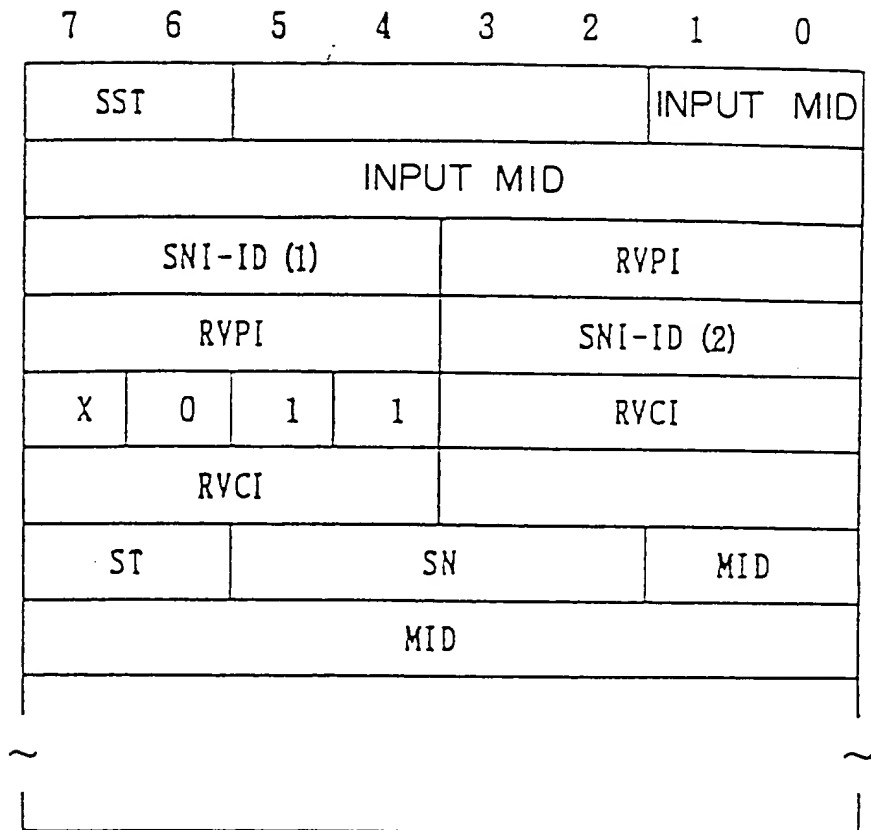


FIG. 413

669360-672260

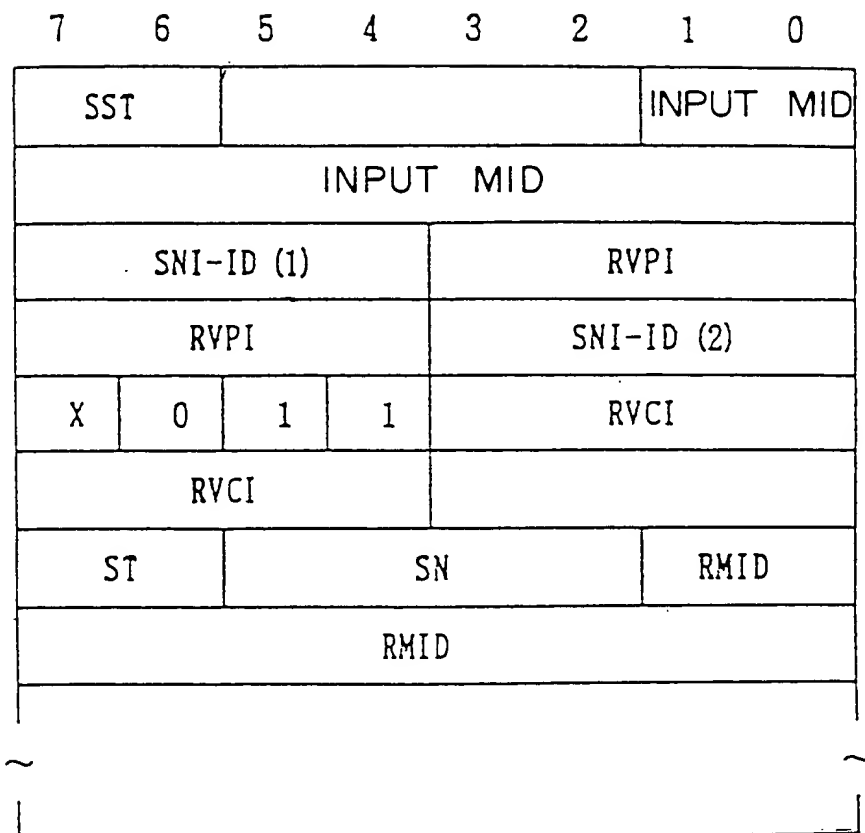


FIG. 414

669620-ET22260

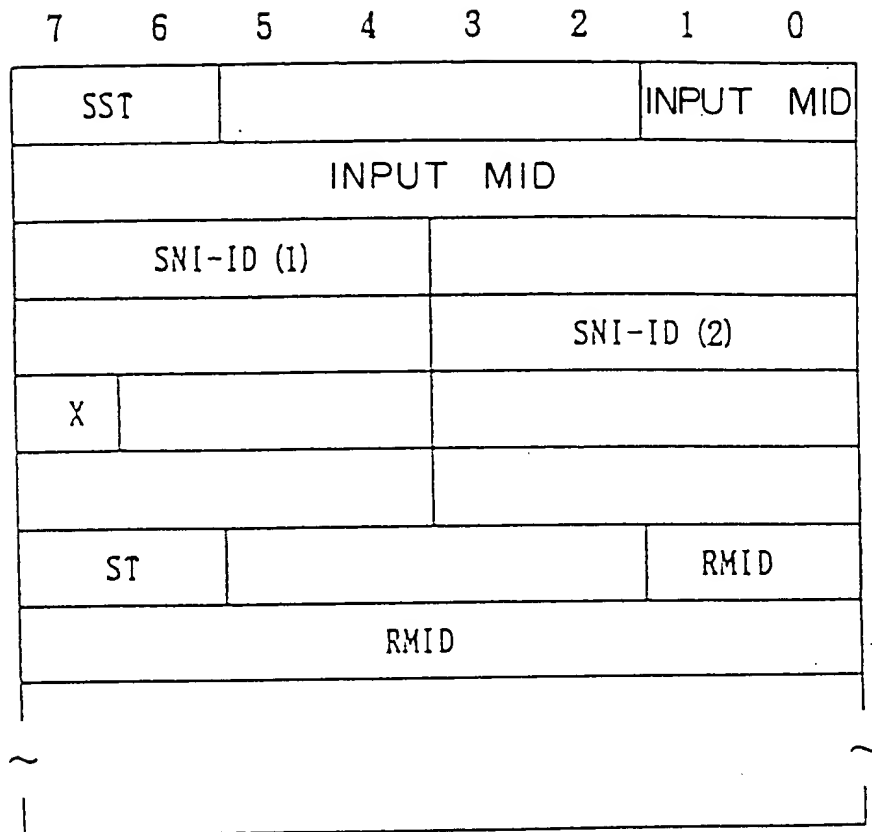


FIG. 415-

7	6	5	4	3	2	1	0
SST						INPUT MID	
INPUT MID							
SNI-ID (1)				RVPI			
RVPI				SNI-ID (2)			
X		BC		RVCI'			
RVCI'							
IST		SN			RMID		
RMID							

FIG. 416

7	6	5	4	3	2	1	0
00	SST					INPUT MID	
01	INPUT MID						
02	SNI-ID (1)				RVPI		
03	RVPI				SNI-ID (2)		
04	X		BC		RVCI'		
05	RVCI'						
06	IST		SN			RMID	
07	RMID						
08							
43							
44	IIT						
45	ES	RV					
46	carrier						
47	carrier_						
48	INID						
49	INID						
50	IITPS						
51	IITPS						
52							
53							

FIG. 417

7 6 5 4 3 2 1 0

SST						INPUT MID	
INPUT MID							
0	0	0	0	RVPI			
RVPI				0	0	0	0
0	0	1	1	RVCI''			
RVCI''							
IST		SN				OUTPUT MID	
OUTPUT MID							

FIG. 418

7 6 5 4 3 2 1 0

SST				INPUT MID	
INPUT MID					
TRIAL	CP	SNI-ID (1)		RVPI	
RVPI				SNI-ID (2)	
X		BC		RVCI''	
RVCI''					
IST		SN			OUTPUT MID
OUTPUT MID					

FIG. 419

7 6 5 4 3 2 1 0

0	0	0	TAGA		0	0
UL	TAGC		TAGB		COM	SIG
VPI						
VPI			VCI			
VCI						
VCI						

FIG. 420

7 6 5 4 3 2 1 0

0	0	0	TAGA		0	0
UL	TAGC		TAGB		COM	SIG
VPI						
VPI			VCI			
VCI						
VCI						

FIG. 421

0000000000000000

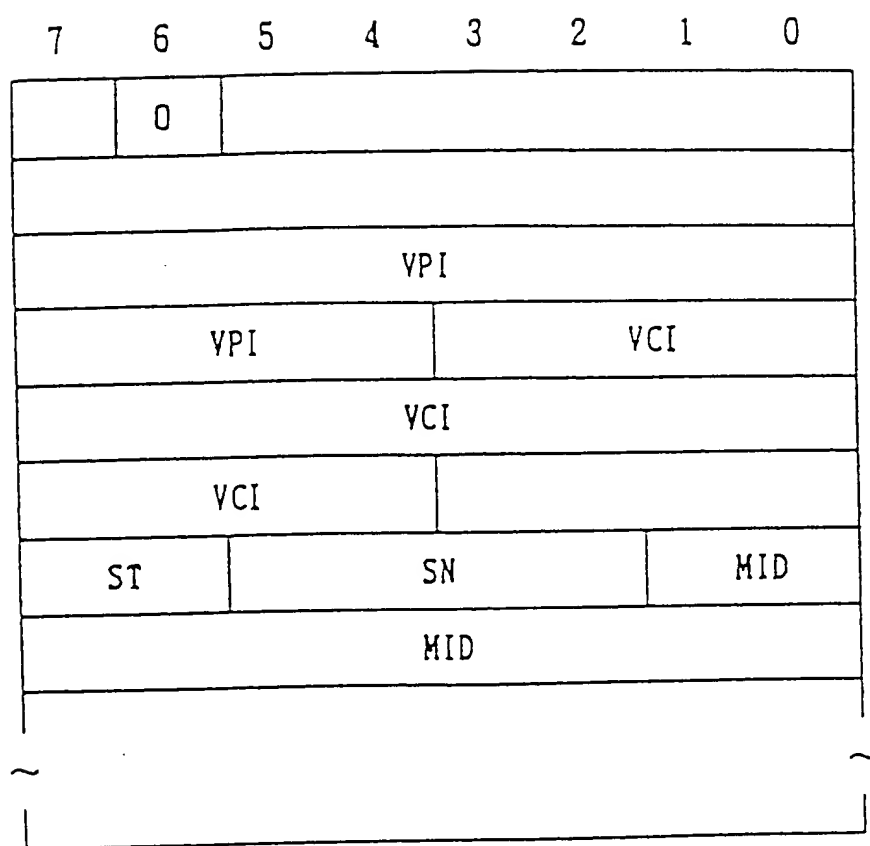


FIG. 422

7 6 5 4 3 2 1 0

IST	DM	0	0	0	RDA
RDA					
VPI					
VPI			VCI		
VCI					
VCI					
ST	SN				MID
MID					

FIG. 423

7	6	5	4	3	2	1	0
IST		DM				RDA	
RDA							
VPI							
VPI				VCI			
VCI							
VCI							
ST		SN				MID	
MID							

100

7	6	5	4	3	2	1	0
IST		DM	PL				RDA'
RDA							
SOURCE MH ID (1)				BRLC			
BRLC				SOURCE MH ID (2)			
0	0	1	1	RVC1			
RVC1							
SST		SN			RMID		
RMID							

—

0000000000000000

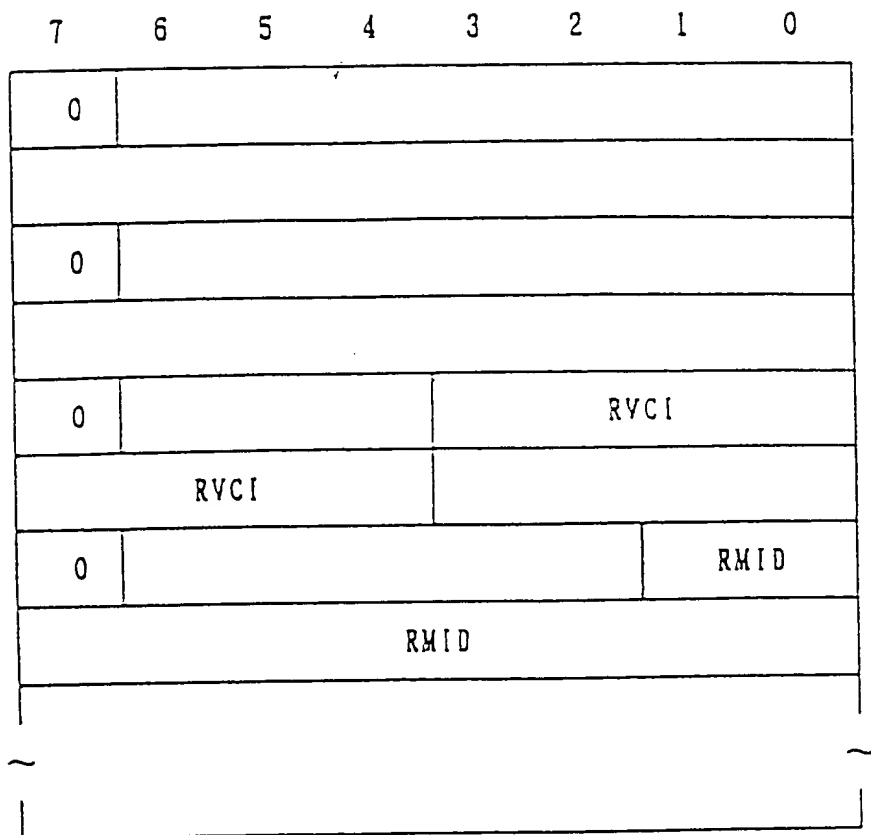


FIG. 426

7 6 5 4 3 2 1 0

IST		DM		PL		RDA	
RDA							
SOURCE MH ID (1)				BRLC			
BRLC				SOURCE MH ID (2)			
0	0	1	1	RVCI			
RVCI							
SST		SN				RMID	
RMID							

FIG. 427

7	6	5	4	3	2	1	0
IST		DM	PL				
			OUTPUT MID				
SOURCE MH ID (1)				BRLC			
BRLC				SOURCE MH ID (2)			
0	0	1	1	RVCI			
RVCI							
SST		SN			OUTPUT MID		
OUTPUT MID							

FIG. 428

7 6 5 4 3 2 1 0

IST		DM		PL		RDA	
RDA							
SOURCE MH ID (1)				BRLC			
BRLC				SOURCE MH ID (2)			
0	0	1	1	RVCI			
RVCI							
SST		SN			RMID		
RMID							

FIG. 429

66320 66320

7	6	5	4	3	2	1	0
IST							
			OUTPUT MID				
0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0
0	0	1	1	RVC I			
RVC I							
SST		SN				OUTPUT MID	
OUTPUT MID							

FIG. 430

7	6	5	4	3	2	1	0
0	0	0	TAGA			0	0
UL	TAGC			TAGB		COM	SIG
VPI							
VPI				VCI			
VCI							
VCI							

FIG. 431

10.24 ERROR FLAG (IN SMLP)

CP																											
cell	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
EP1	MS				IM	MA																					
EP2	MT	CC	PL	IM	MA	SN	ST	DT	AT	DA	DP	SP	BA	AC	HE	CS	VE	EM	SA	DS	BE	IL	LE	MH	EB		

[EP1]

MS : master
IM : COM with MID=0
MA : MID not active (COM)

[EP2]

MT : MFI time out
CC : Payload CRC violation
PL : Payload length error
IM : BOM/SSM with invalid MID
MA : MID currently active or BOM with unapproved MID
SN : Invalid sequence number
ST : Invalid SA type
DT : Invalid DA type
AT : Invalid SMDS address type
DA : Individual DA assigned to originating SNI
DF : DA field format error
SP : SA field format error

BA : Invalid BAsize field value
AC : Access class violation
HE : Invalid HE length field value
CS : Invalid HE carrier selection
VE : Invalid HE version
EM : Exceed maximum number of CDU
SA : SA not assigned to originating SNI
DS : DA screening violation
BE : BEtag mismatch
IL : Incorrect length
LE : BAsize field not equal to length field
MH : MID assigned error
EB : End-user blocking

10.25 ERROR FLAG (IN RMLP)

CP																													
cell		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
EP1										CA	ED		MD	EE															
EP2																													

[EP1]

MS : master
MC : COM MID active error
CA : CA active error
ED : CDU active error
MD : RMID active error
BE : Encapsulation D.C.

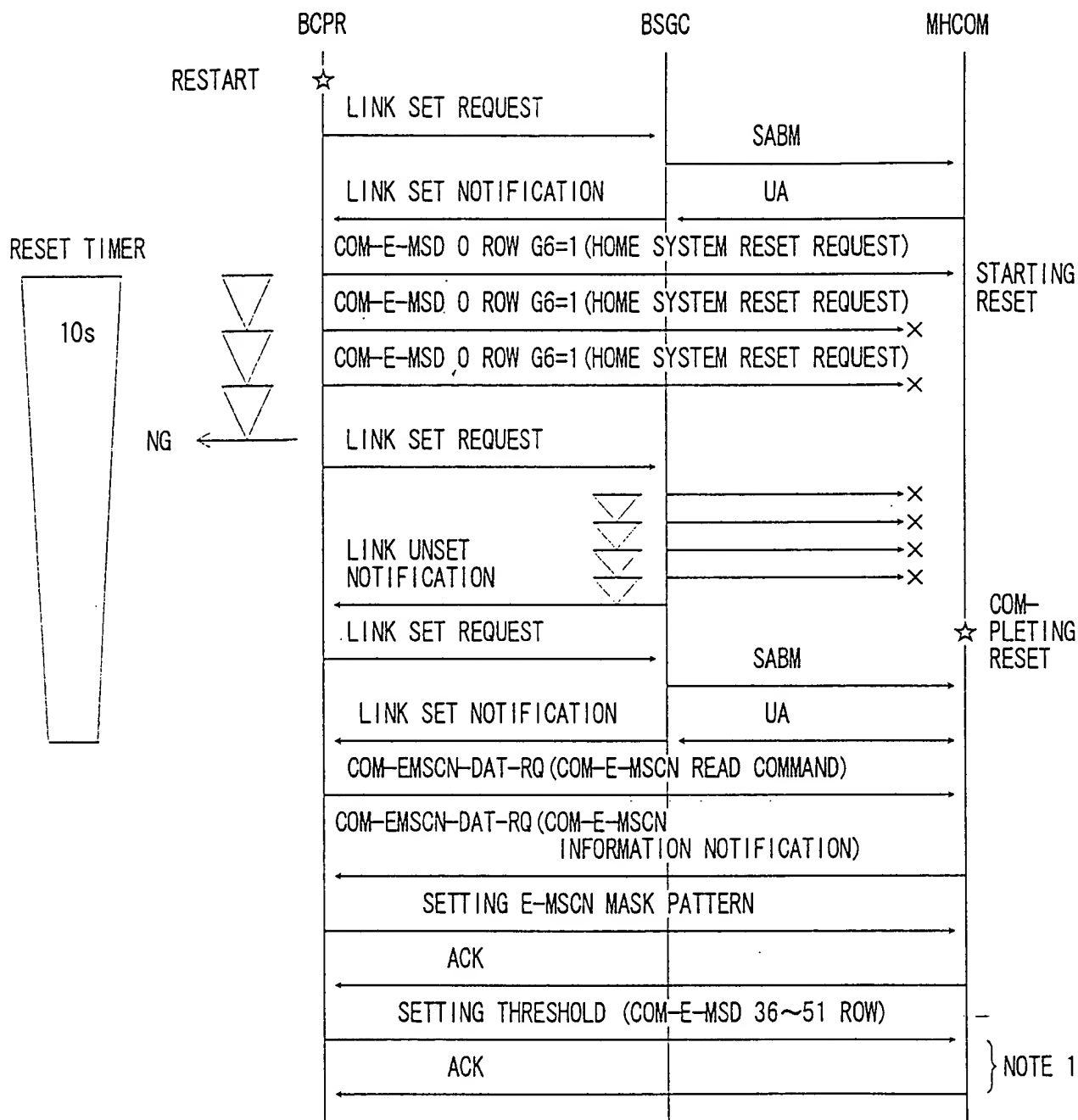
[EP2]

MT : MTI time out
DO : Destination equal to
 originating SHI
CC : Payload CRC violation
MA : MID active error
SH : Invalid sequence number

SS : SA screening violation
DA : Destination SHI not available
EM : Exceed maximum number of CDU
BE : BEtag mismatch
MN : RMID assigned error
EH : Encapsulation error

FIG. 433

66920-72250

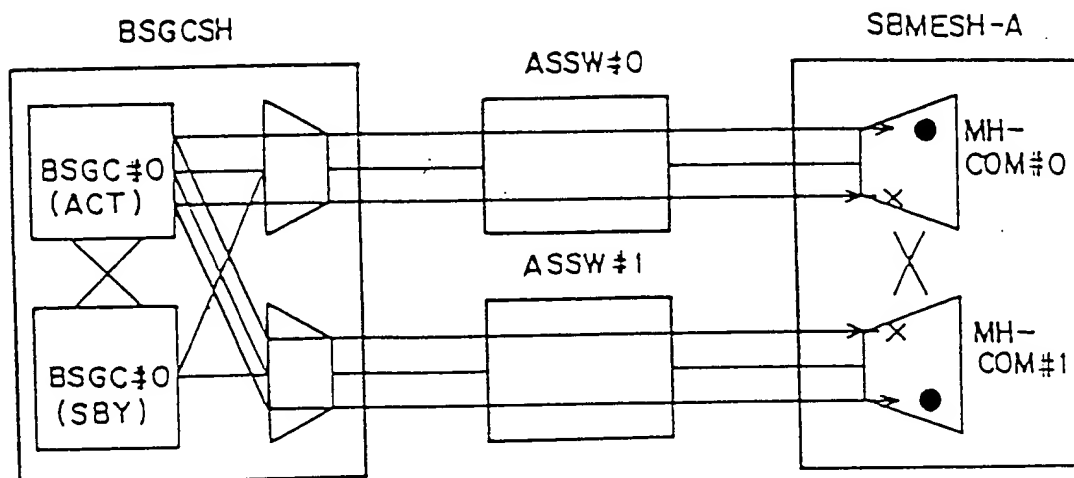


NOTE 1 : NOT NECESSARY TO SET THRESHOLD WHEN HARDWARE DEFAULT VALUE IS USED.
SINGLE COMMAND CAN SET THRESHOLD OF 1MUX OR 1DMUX ONLY.

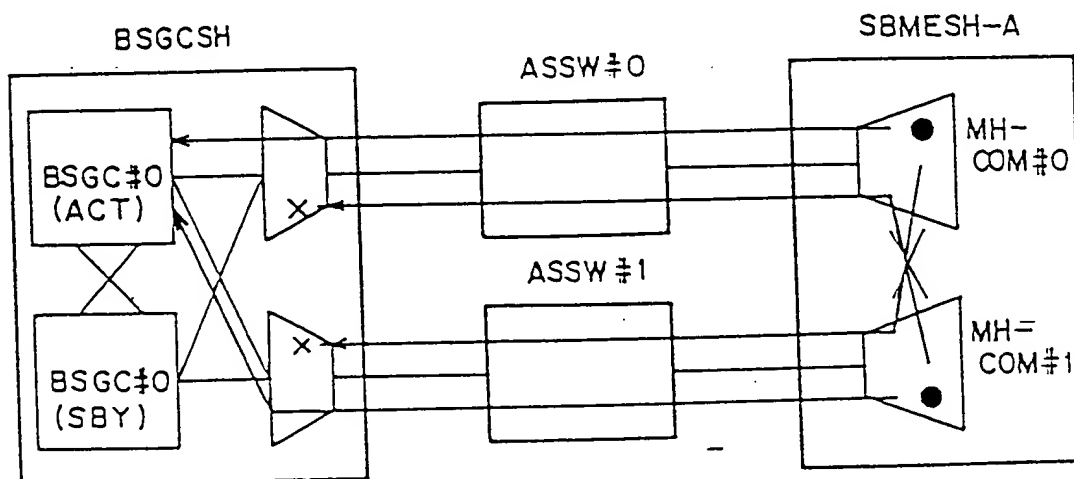
FIG. 434

00000-00000-00000

(BSGC → MH-COM DIRECTION)



(MH-COM → BSGC DIRECTION)



●... ENDING POINT

×... DISCARDING POINT

FIG. 435

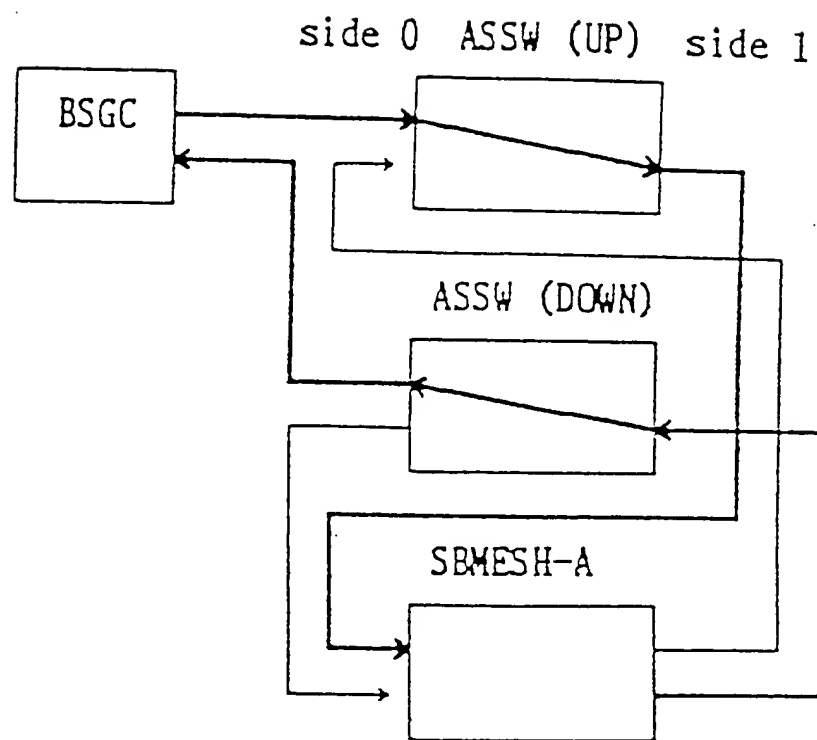


FIG. 437

66920-22250

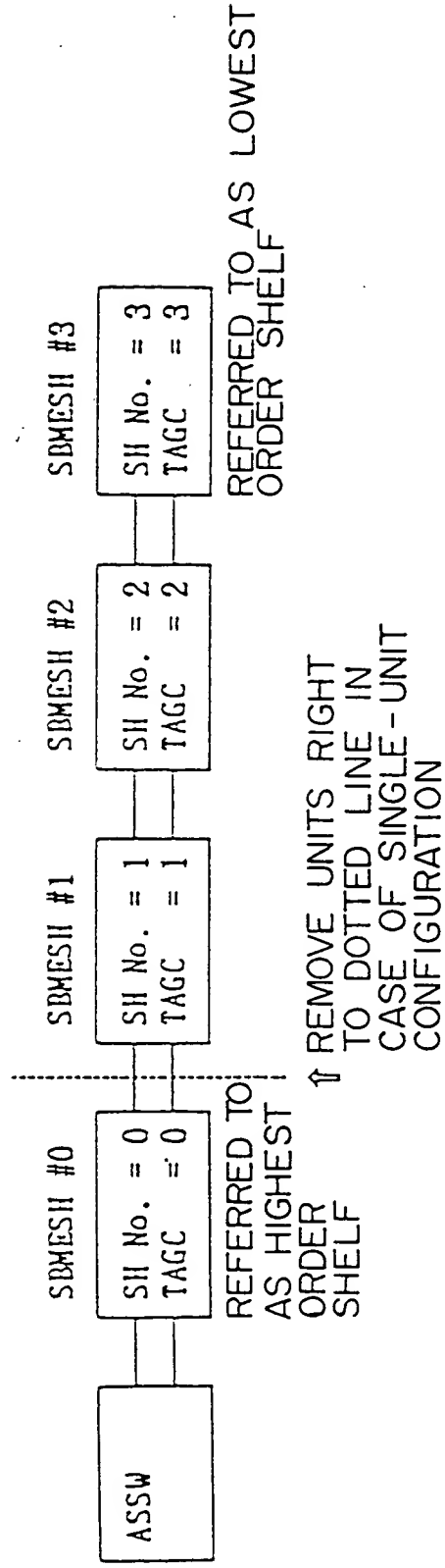


FIG. 438

0092E0 E F E 2 2 50

shelf No.	UL	TAGC	COM	SIG	O
0	0	0	0	0	0
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	0

FIG. 440

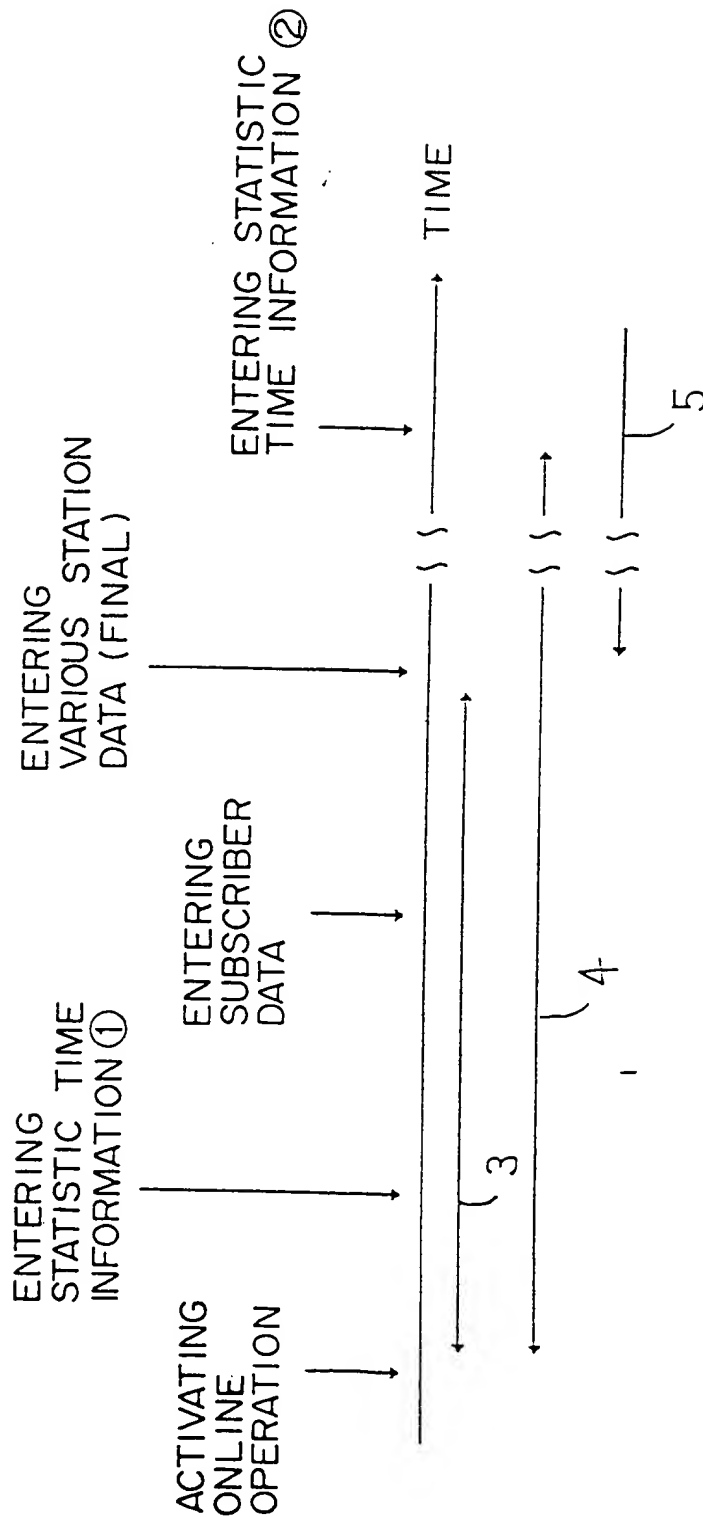


FIG. 441

A
B
C
D

A

B

all O

D

[illegible]

0927243-032699

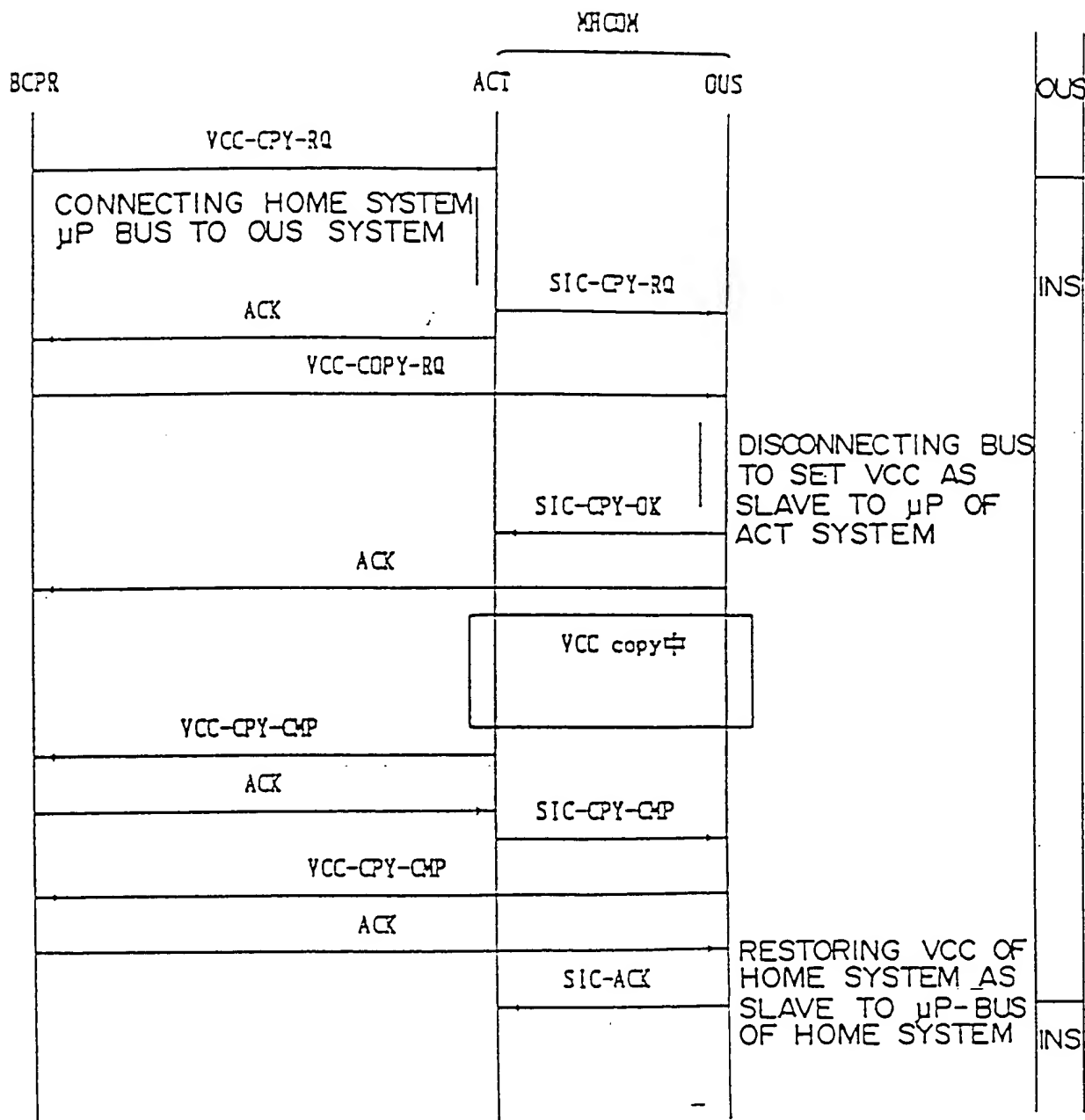


FIG. 443

ITEM	FAULT TYPE	NOTIFICATION METHOD	NOTIFYING SYSTEM	SUSPECT UNIT	ACTION					REMARKS
					ASSW SYSTEM SWITCH	FAULT BLOCK	FAULT MESSAGE	ALM LIGHTED	MAKING DIAGNOSIS	
1	HARDWARE FAULT (EXCEPT SIGNALLING UNIT AND RNUX UNIT)	HOME SYSTEM E-MSCN	ACT	ACT WHCOM	O	O	O	O	O PREVIOUS ACT	ACTIVATING DIAGNOSIS FROM MATE SYSTEM
			SBY	SBY WHCOM	—	O	O	O	O SBY	
2	HARDWARE FAULT (SIGNALLING UNIT AND RNUX UNIT)	MATE SYSTEM E-MSCN	ACT	SBY WHCOM	—	O	O	O	O SBY	
			SBY	ACT WHCOM	O	O	O	O	O PREVIOUS ACT	
3	OBP FAULT	MATE SYSTEM E-MSCN	ACT	SBY WHCOM	—	O	O	O	O SBY	
			SBY	ACT WHCOM	O	O	O	O	O PREVIOUS ACT	
4	MATE POWER PWCB FAULT (DISCONNECTION OF FUSE)	MATE SYSTEM E-MSCN	ACT	SBY SYSTEM POWER PWCB	—	O	O	O	O SBY	POWER SUPPLIED BY POWER PWCB CLOSING WHCOM ↓ BLOCKING ASSW OF CORRESPONDING SYSTEM
			SBY	ACT SYSTEM POWER PWCB	O	O	O	O	O PREVIOUS ACT	

FIG. 444


```

sequenceDiagram
    participant ACT1 as ACT
    participant BCPR as BCPR
    participant SBY1 as SBY
    participant ACT2 as ACT
    participant MHCOM as MHCOM
    participant SBY2 as SBY

    ACT1->>BCPR: E-MSCN (FAULT)
    BCPR->>SBY1: ACK
    SBY1->>ACT2: REPORTING MASK PATTERN
    ACT2->>SBY1: ACK
    SBY1->>MHCOM: LIGHTING MATE SYSTEM OUS
    MHCOM->>SBY2: MATE SYSTEM RESET REQUEST
    SBY2->>ACT2: ACK
    ACT2->>MHCOM: RESET REQUEST
    MHCOM->>SBY2: RESET COMPLETION
    SBY2->>ACT2: REPORTING MATE SYSTEM RESET COMPLETION
    ACT2->>SBY1: ACK
    SBY1->>ACT2: SABM
    ACT2->>SBY1: UA
    SBY1->>ACT2: ACTIVATING DIAGNOSTICS
    ACT2->>SBY1: SABM
    SBY1->>ACT2: UA
    ACT2->>SBY1: READING DIAGNOSTICS RESULT (READING EMSCN)
    SBY1->>ACT2: ACK
    ACT2->>SBY1: REPORTING DIAGNOSTICS RESULT
    SBY1->>ACT2: ACK
    
```

The diagram illustrates a sequence of events between several entities: ACT, BCPR, SBY, ACT, MHCOM, and SBY. The sequence is divided into two main phases: 'DISPLAYING FAULT MESSAGE' and 'DISPLAYING DIAGNOSTICS RESULT'. The first phase involves the transmission of 'E-MSCN (FAULT)' from ACT to BCPR, followed by an 'ACK' from BCPR to SBY. SBY then sends 'REPORTING MASK PATTERN' to ACT, which responds with 'ACK'. SBY sends 'LIGHTING MATE SYSTEM OUS' to MHCOM, which then sends 'MATE SYSTEM RESET REQUEST' to SBY. SBY responds with 'ACK' to ACT, which then sends 'RESET REQUEST' to MHCOM. MHCOM responds with 'RESET COMPLETION' to SBY, who then sends 'REPORTING MATE SYSTEM RESET COMPLETION' to ACT. ACT responds with 'ACK' to SBY. The second phase begins with SBY sending 'SABM' to ACT, who responds with 'UA'. SBY then sends 'ACTIVATING DIAGNOSTICS' to ACT, who responds with 'SABM'. SBY sends 'UA' to ACT, who then sends 'READING DIAGNOSTICS RESULT (READING EMSCN)' to SBY. SBY responds with 'ACK' to ACT, who then sends 'REPORTING DIAGNOSTICS RESULT' to SBY. Finally, SBY sends 'ACK' to ACT. A star symbol marks the end of the sequence.

FIG. 446

```

sequenceDiagram
    participant ACT
    participant BCPR
    participant SBY
    participant MHCOM

    SBY->>MHCOM: FAULT REPORT
    SBY->>ACT: ☆
    ACT->>BCPR: DISPLAYING FAULT MESSAGE
    BCPR->>SBY: COM-E-MSCN (MATE SYSTEM FAULT)
    SBY->>BCPR: ACK
    BCPR->>SBY: REPORTING MASK PATTERN
    SBY->>BCPR: ACK
    BCPR->>SBY: LIGHTING MATE SYSTEM OUS
    SBY->>BCPR: ACK
    BCPR->>SBY: MATE SYSTEM RESET REQUEST
    SBY->>BCPR: ACK
    BCPR->>SBY: REPORTING MATE SYSTEM RESET COMPLETION
    SBY->>BCPR: ACK
    BCPR->>MHCOM: RESET REQUEST
    MHCOM->>SBY: RESET COMPLETION
    SBY->>ACT: ☆
    BCPR->>SBY: LINK ESTABLISHMENT
    SBY->>BCPR: NG
    BCPR->>SBY: N-TIME RETRIAL
    SBY->>BCPR: NG
    BCPR->>SBY: ACTIVATING MATE SYSTEM DIAGNOSTICS
    SBY->>MHCOM: ACTIVATING DIAGNOSTICS
    MHCOM->>SBY: RESULT REPORT
    SBY->>ACT: DISPLAYING DIAGNOSTICS RESULT
    
```

FIG. 447

[illegible]

FIG. 448

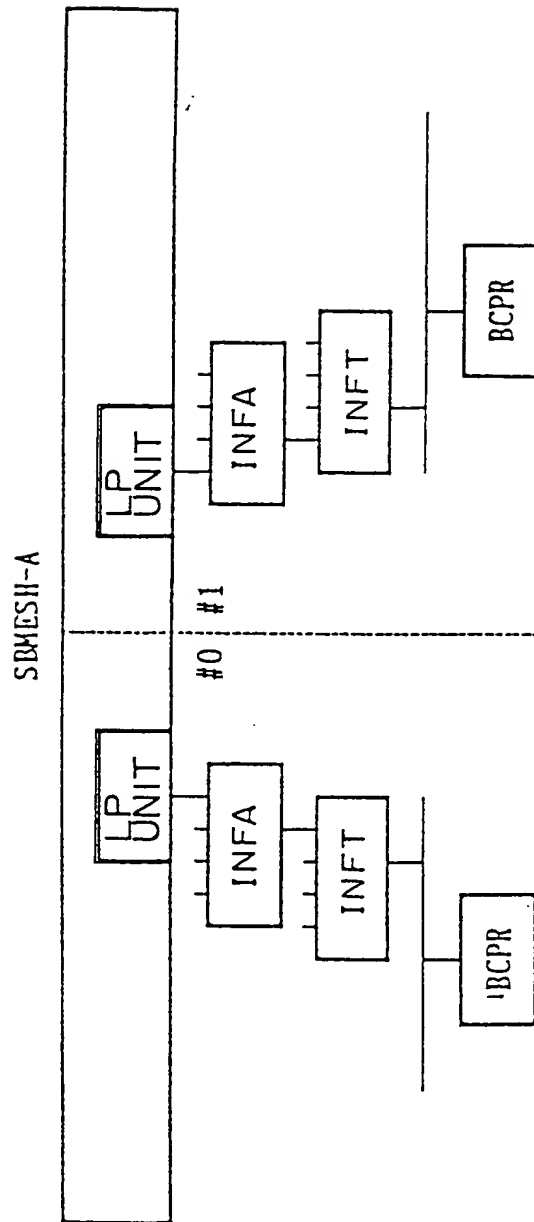


FIG. 449

BIT	CONTENTS	POLARITY
31	DISPLAYING RESET COMPLETION	1 WHEN RESET COMPLETION
30	DON' T CARE	_____
29	LP UNIT FAULT	1 WHEN FAULT OCCURS
28	DMA ACCESS ERROR 1	1 WHEN ERROR OCCURS
27	DMA ACCESS ERROR 2	1 WHEN ERROR OCCURS
26	DMA PARITY ERROR	1 WHEN ERROR OCCURS
25	DMA TIME OVER	1 AT TIME OVER
24	DON' T CARE	_____
23	MPAL : MATE LP UNIT FAULT	1 WHEN FAULT OCCURS
22	MFAL : MATE FUSE ALARM	1 WHEN ALARM IS OUTPUT
21	HOME SDMX ⇒ SMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
20	HOME SDMX ⇒ SMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
19	MATE SDMX ⇒ SMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
18	MATE SDMX ⇒ SMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
17	SMLP ⇒ HOME SMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
16	SMLP ⇒ HOME SMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
15	SMLP ⇒ MATE SMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
14	SMLP ⇒ MATE SMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
13	HOME RDMX ⇒ RMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
12	HOME RDMX ⇒ RMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
11	MATE RDMX ⇒ RMLP CROSS-CONNECTION FAULT PARITY NG	1 AT NG
10	MATE RDMX ⇒ RMLP CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
09	RMLP ⇒ HOME RMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
08	RMLP ⇒ HOME RMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
07	RMLP ⇒ MATE RMUX CROSS-CONNECTION FAULT PARITY NG	1 AT NG
06	RMLP ⇒ MATE RMUX CROSS-CONNECTION FAULT CF NG OR CLOCK NG	1 AT NG
05	DON' T CARE	_____
04	DON' T CARE	_____
03	DON' T CARE	_____
02	DON' T CARE	_____
01	HOME MH-COM ⇒ LP CROSS-CONNECTION FAULT SOURCE CLOCK NG	1 AT NG
00	MATE MH-COM ⇒ LP CROSS-CONNECTION FAULT SOURCE CLOCK NG	1 AT NG

F I G. 4 5 0

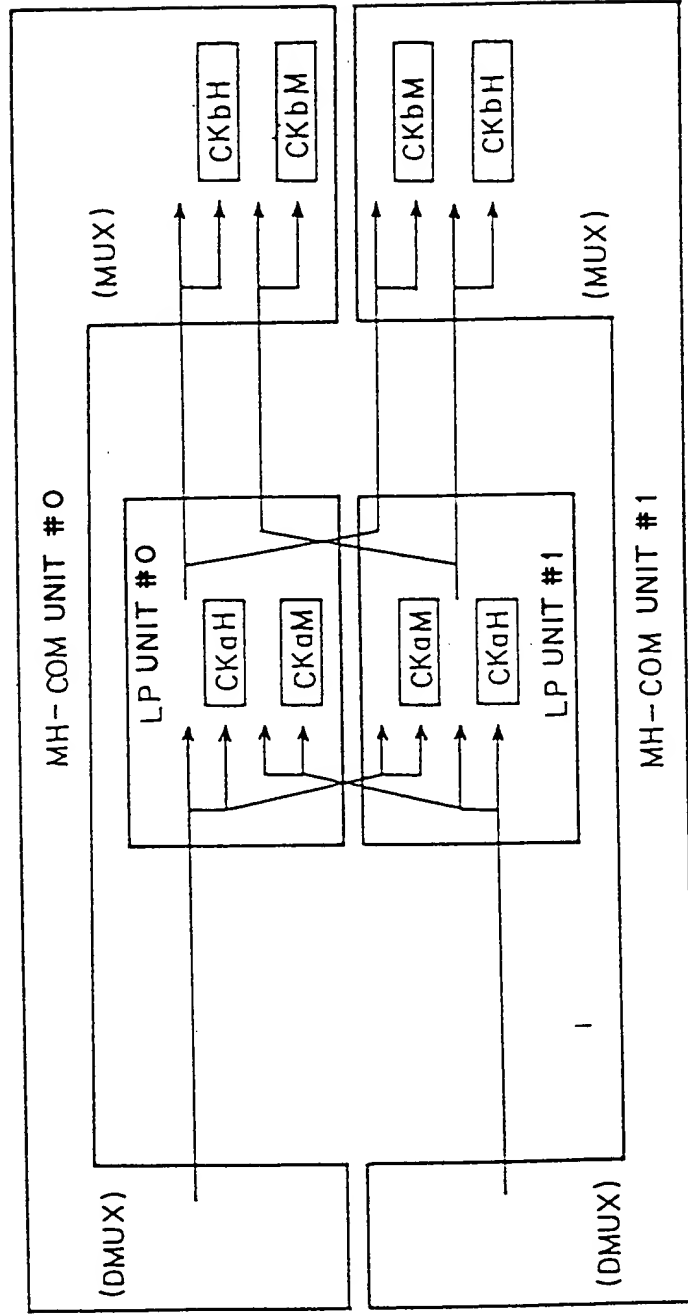


FIG. 451

(a)

LP UNIT #0	bit 17 NG	bit 15 OK
bit 15 NG	bit 17 OK	LP UNIT #1

Connections:

- LP UNIT #0 bit 17 NG → MH-COM UNIT #0 CKbH NG
- LP UNIT #0 bit 15 OK → MH-COM UNIT #0 CKbM NG
- LP UNIT #1 bit 15 NG → MH-COM UNIT #1 CKbM OK
- LP UNIT #1 bit 17 OK → MH-COM UNIT #1 CKbH OK

MH-COM UNIT #0

MH-COM UNIT #1

(b)

LP UNIT #0	MH-COM UNIT #0
bit 17 NG	CKbH NG
bit 15 NG	CKbM OK

LP UNIT #1	MH-COM UNIT #1
bit 15 OK	CKbM NG
bit 17 OK	CKbH OK

(C)

LP UNIT #0	MH-COM UNIT #0
bit 17 NG	СКБН NG
bit 15 OK	СКБМ OK

LP UNIT #1	MH-COM UNIT #1
bit 15 OK	СКБМ OK
bit 17 OK	СКБН OK

FIG. 452

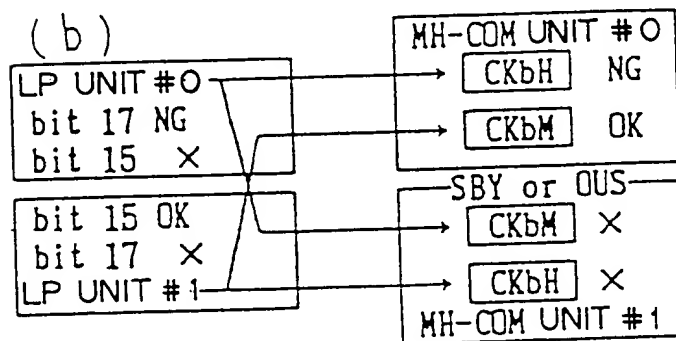
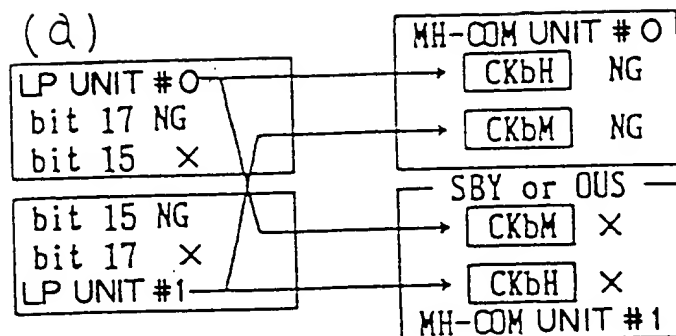
[illegible]

FIG. 453

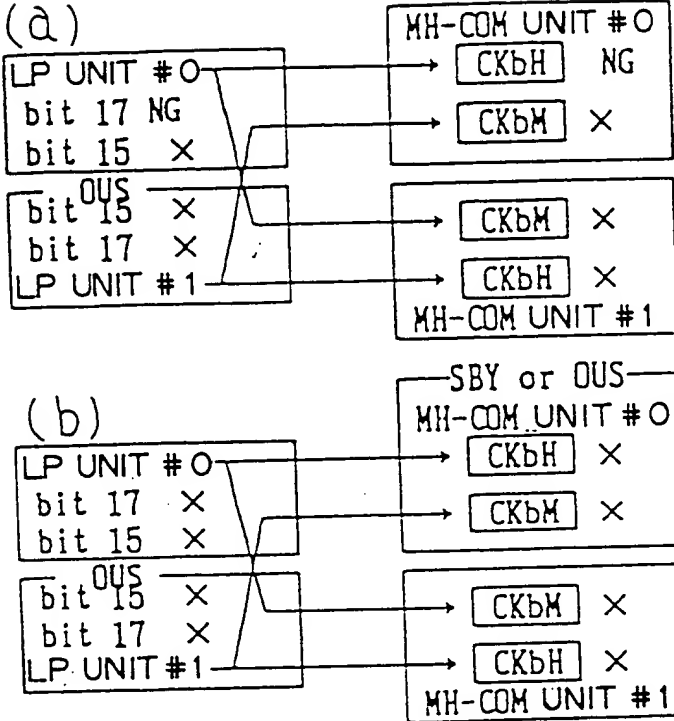
[illegible]

FIG. 454

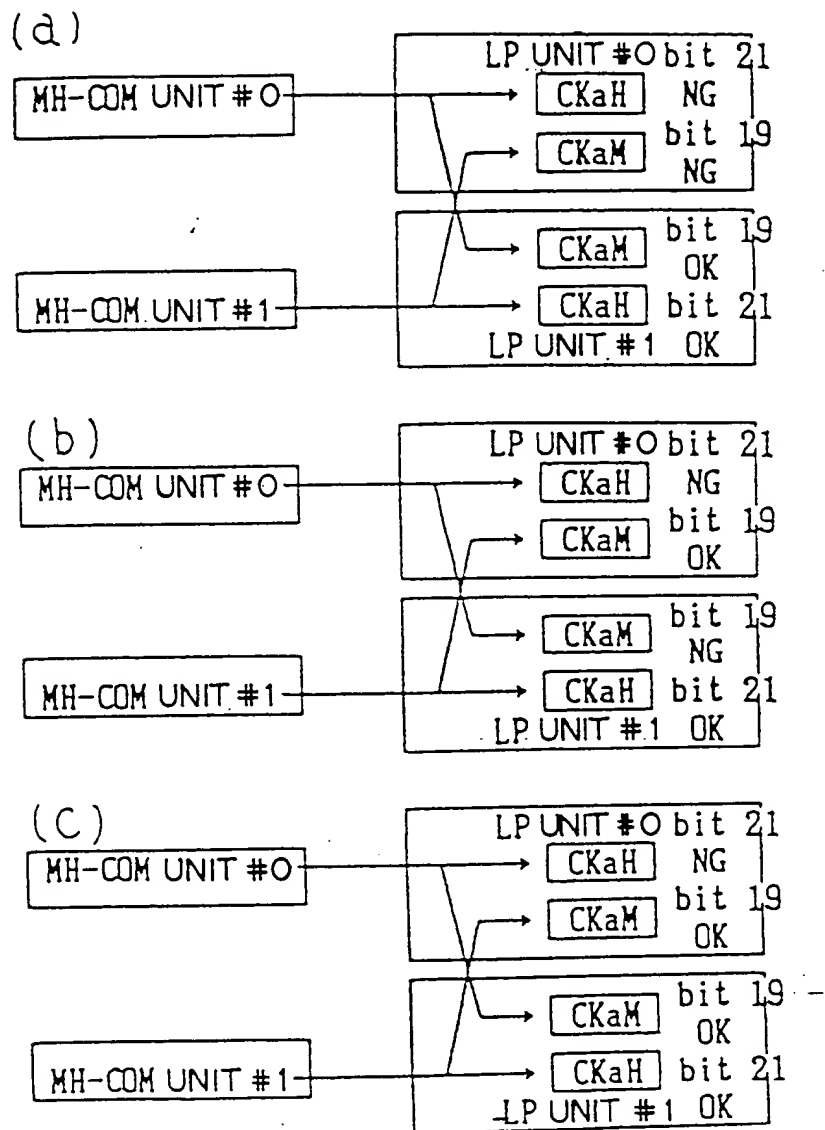


FIG. 455

(a)

Unit	LP UNIT #0	bit 21
MH-COM UNIT #0	CKaH	NG
	CKaM	bit 19 ×

Unit	LP UNIT #1	bit 21
MH-COM UNIT #1	CKaM	bit 19 ×
	CKaH	bit 21 ×

(b)

Unit	LP UNIT #0	bit 21
MH-COM UNIT #0	CKaH	NG
	CKaM	bit 19 ×

Unit	LP UNIT #1	bit 21
OUS MH-COM UNIT #1	CKaM	bit 19 NG
	CKaH	bit 21 ×

(c)

Unit	LP UNIT #0	bit 21
MH-COM UNIT #0	CKaH	NG
	CKaM	bit 19 ×

Unit	LP UNIT #1	bit 21
OUS MH-COM UNIT #1	CKaM	bit 19 OK
	CKaH	bit 21 ×

(d)

Unit	LP UNIT #0	bit 21
MH-COM UNIT #0	CKaH	×
	CKaM	bit 19 ×

Unit	LP UNIT #1	bit 21
OUS MH-COM UNIT #1	CKaM	bit 19 ×
	CKaH	bit 21 ×

FIG. 456

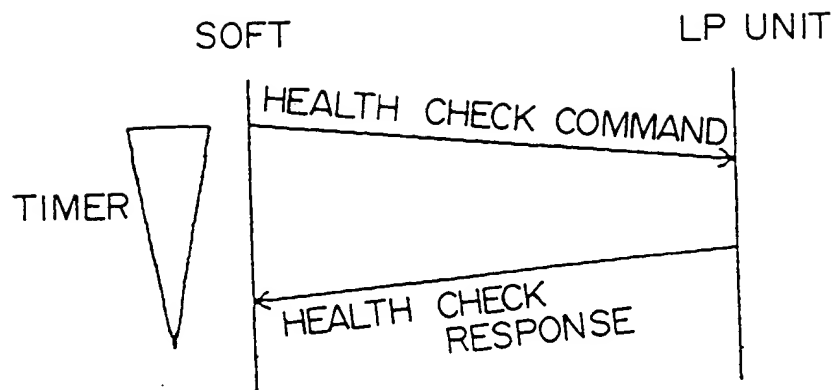


FIG. 457

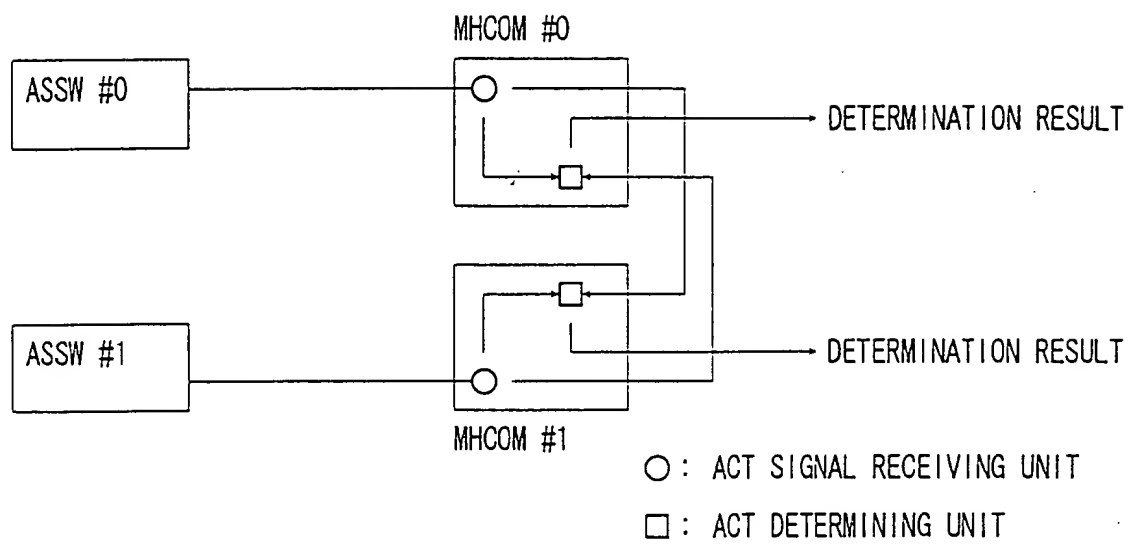
[illegible]

FIG. 458

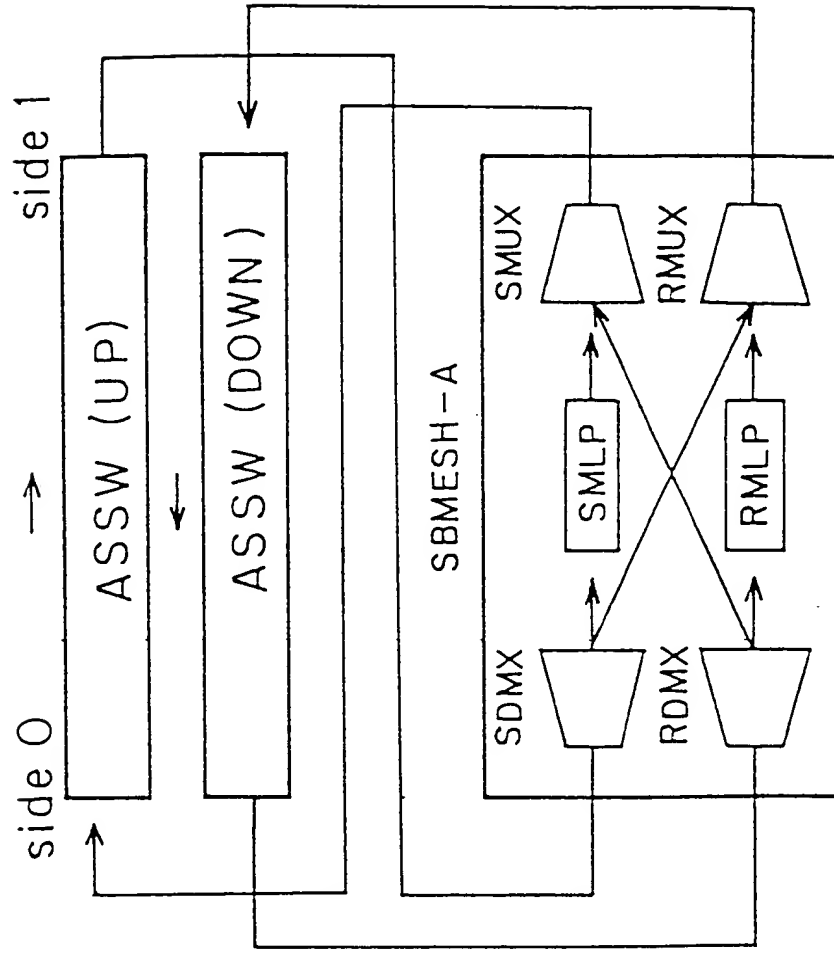
[illegible]

FIG. 459

The diagram illustrates a multi-channel system architecture. On the left, three rectangular boxes represent individual units, labeled "INDIVIDUAL UNIT 0", "INDIVIDUAL UNIT 1", and "INDIVIDUAL UNIT 7". A bracket groups these units. Each unit has a horizontal output line that terminates in an arrow pointing towards a central vertical bus. Below the "INDIVIDUAL UNIT 7" box, an upward-pointing arrow is labeled "LOOPBACK". To the right of the bus is a large, vertical, trapezoidal shape representing a common bus or switch. A double-headed horizontal arrow connects this bus to the label "ASSW" on the far right.

1

shelf 0

LP UNIT

shelf 1

LP UNIT

shelf 3

LP UNIT

ASSW

DAISY CHAIN

FIG. 461

shelf No.	UL	TAGC	COM	SIG	0
0	0	0	0	0	1
1	0	1	0	0	1
2	0	2	0	0	1
3	0	3	0	0	1

—

66960-01-0000

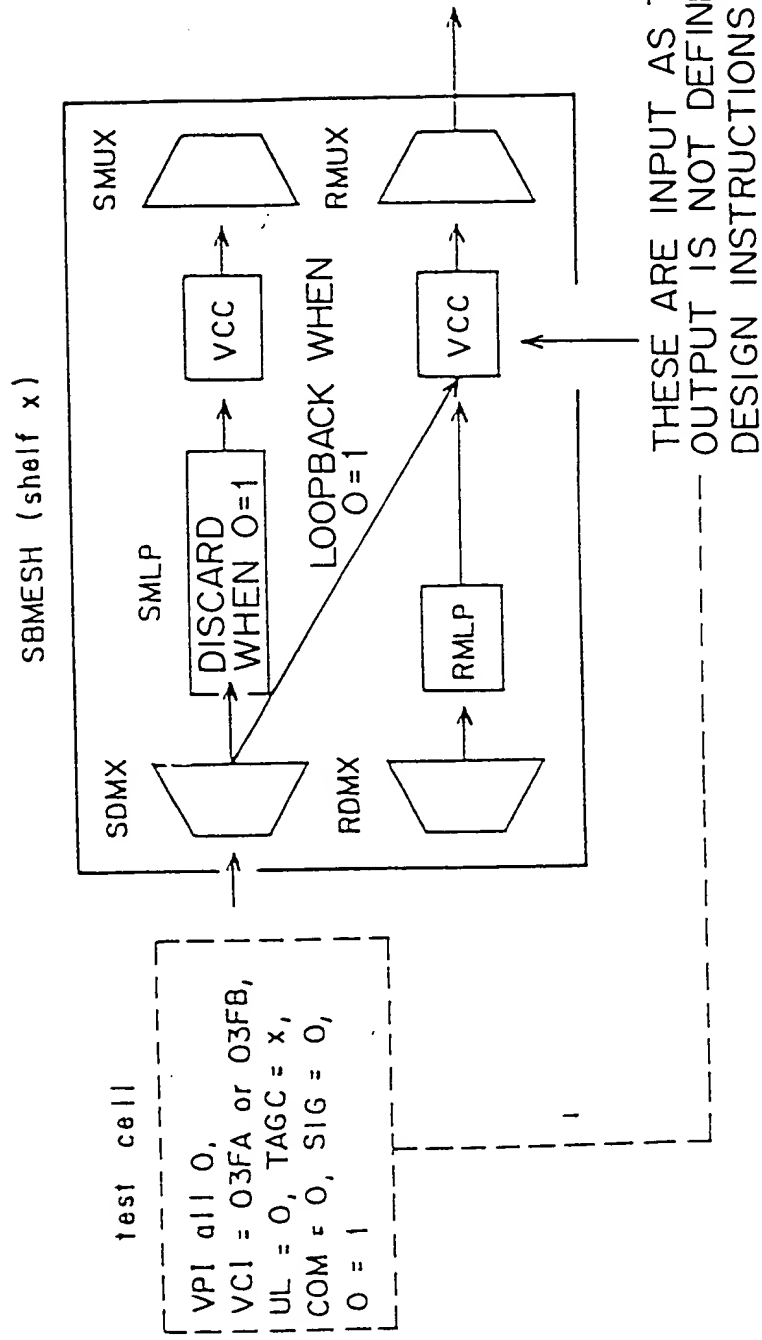
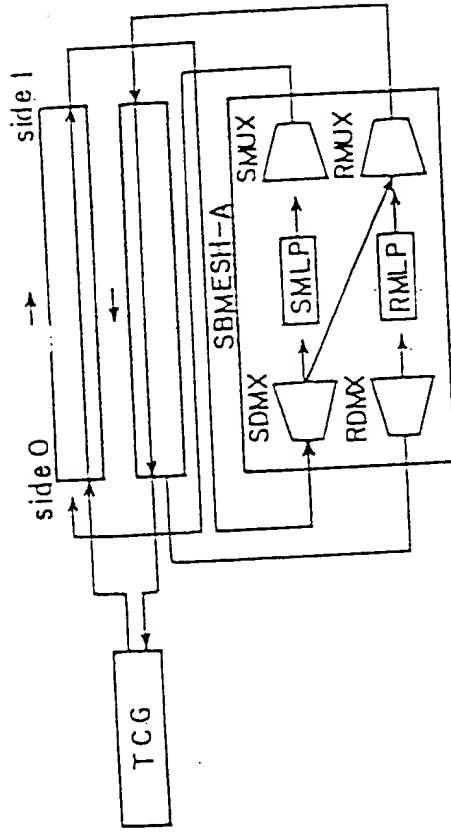
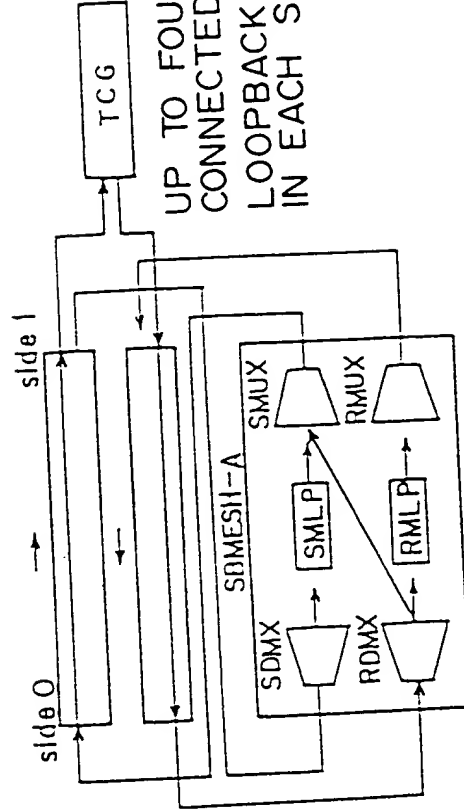


FIG. 463

669200-ET2260



UP TO FOUR SBMESHs ARE
CONNECTED AS DAISY CHAIN.
LOOPBACK TEST IS CONDUCTED
IN EACH SHELF.



UP TO FOUR SBMESHs ARE
CONNECTED AS DAISY CHAIN.
LOOPBACK TEST IS CONDUCTED
IN EACH SHELF.

FIG. 464

669607E2260

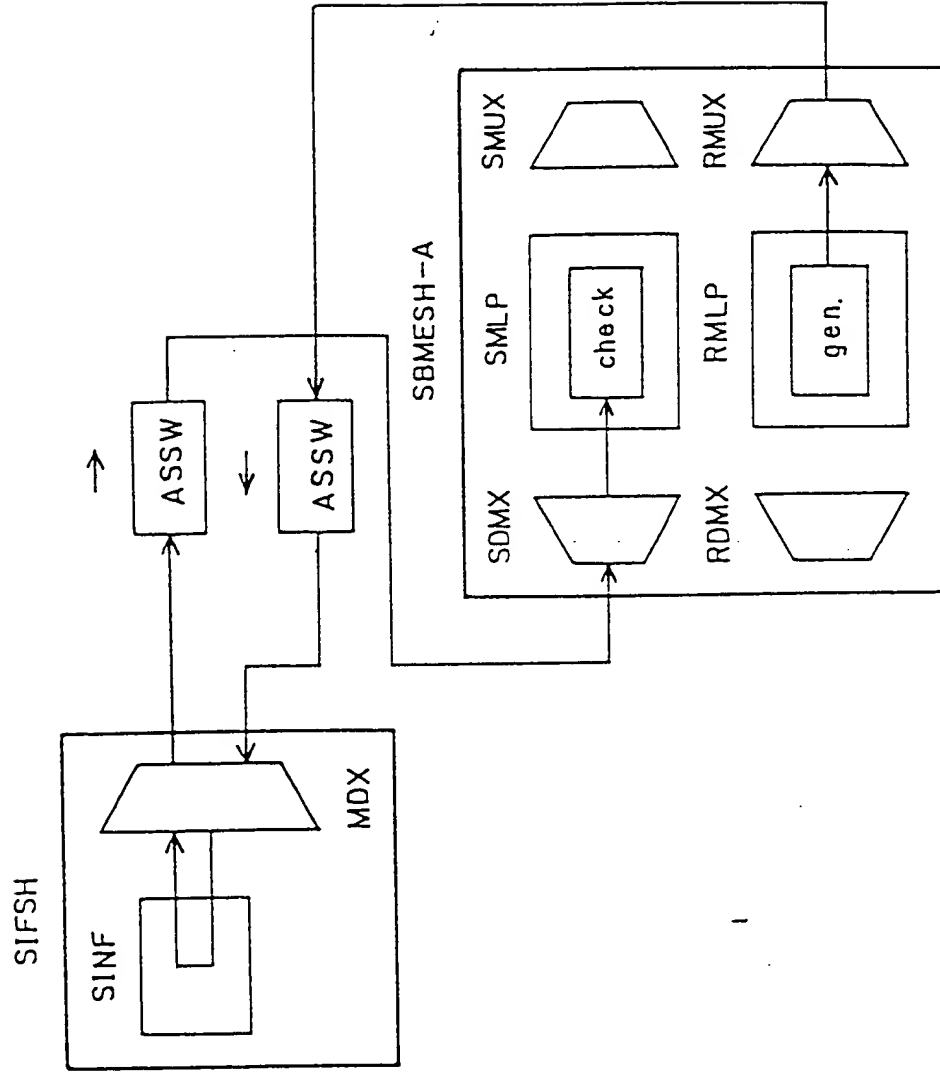


FIG. 465

TEST OBJECT	EXISTENCE OF BLOCK	LOOPBACK
SMDS DS1 DT SMDS DS3 DT	BLOCKED	USING LOOP FUNCTION OF LINE (ALL CELLS ARE LOOPED BACK)
ATM DS1 DT ATM DS3 DT SINF UMBILICAL DS3 DT	NOT BLOCKED	USING SPECIFIED VPI/VCI LOOPBACK FUNCTION (TEST CELLS ARE LOOPED BACK)

FIG. 466

Figure 1 illustrates the SBMESH-A architecture, showing three sub-figures (a), (b), and (c) within a dashed boundary labeled MH 1. Above the sub-figures, two ASSW blocks are connected by a bidirectional arrow.

Sub-figure (a) shows a 2x3 grid of components: SDM, SMLP (containing 'gen.'), SMUX, RDM, RMLP, and RMUX. Arrows indicate data flow from the ASSW block to the SMLP and RMLP blocks, and from the SMLP block to the SMUX block.

Sub-figure (b) shows a 2x3 grid of components: SDM, SMLP (containing 'check'), SMUX, RDM, RMLP (containing 'check'), and RMUX. Arrows indicate data flow from the ASSW block to the SMLP and RMLP blocks, and from the SMLP block to the SMUX block.

Sub-figure (c) shows a 2x3 grid of components: SDM, SMLP, SMUX, RDM, RMLP (containing 'check'), and RMUX. Arrows indicate data flow from the ASSW block to the SMLP and RMLP blocks, and from the RMLP block to the RMUX block.

MH 1

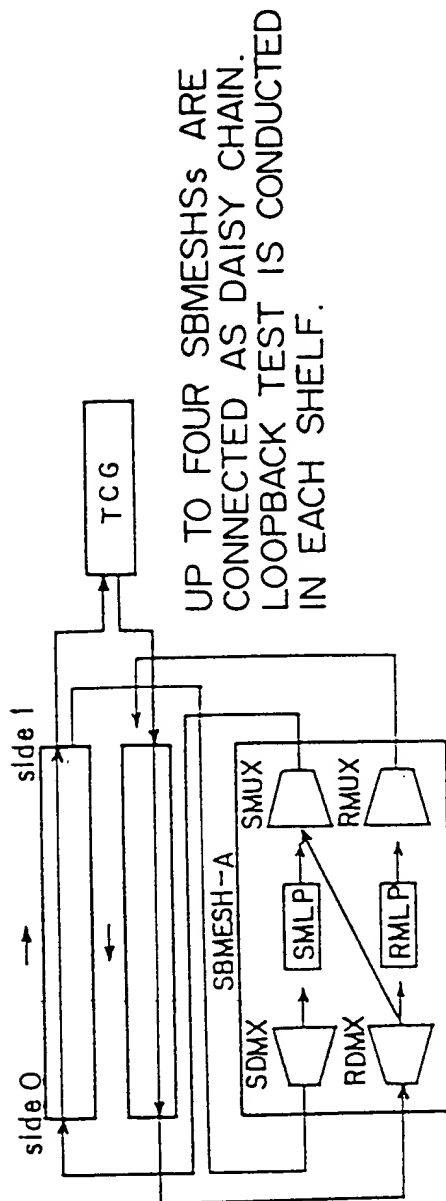
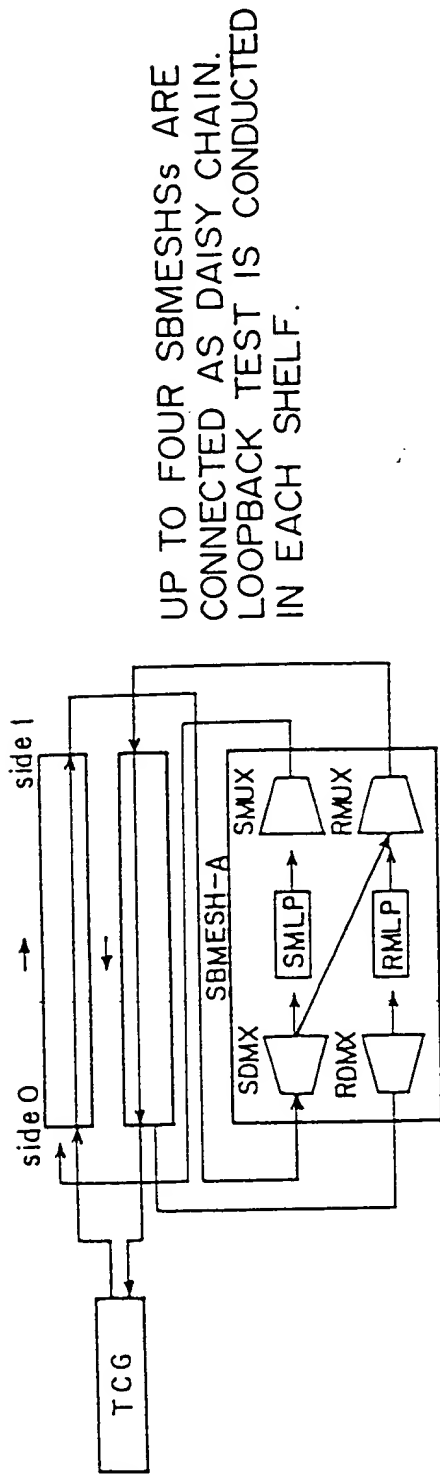


FIG. 468

0				8				16				24				31															
TEST CELL SENDING UNIT FAULT DISPLAY AREA								TEST CELL RECEIVING UNIT FAULT DISPLAY AREA																							
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0	CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8	CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16	CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24
																SNI-SBMESH PVC TEST RESULT DISPLAY AREA															
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0	CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8	CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16	CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24
																MESH-MH PVC TEST RESULT DISPLAY AREA (WHEN SPECIFIC TEST DA IS USED)															
CELL 7	CELL 6	CELL 5	CELL 4	CELL 3	CELL 2	CELL 1	CELL 0	CELL 15	CELL 14	CELL 13	CELL 12	CELL 11	CELL 10	CELL 9	CELL 8	CELL 23	CELL 22	CELL 21	CELL 20	CELL 19	CELL 18	CELL 17	CELL 16	CELL 31	CELL 30	CELL 29	CELL 28	CELL 27	CELL 26	CELL 25	CELL 24
																MESH-MH PVC TEST RESULT DISPLAY AREA (WHEN ALLOCATED DA IS USED)															

0000000000000000

00																15
																A

A : HLP02A I/O add. 0296 D0
B : HLP02A I/O add. 0300 D0
BLANK : 0 ,

FIG. 470

[illegible]

FIG. 471

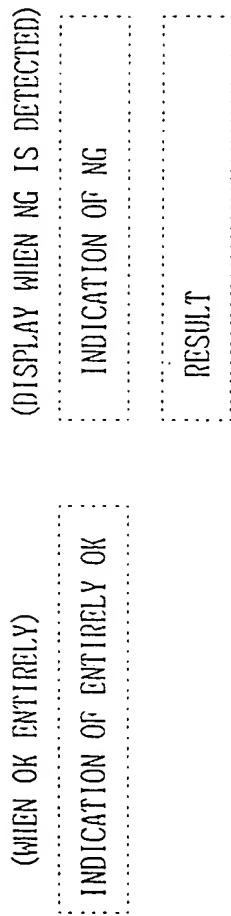


FIG. 472

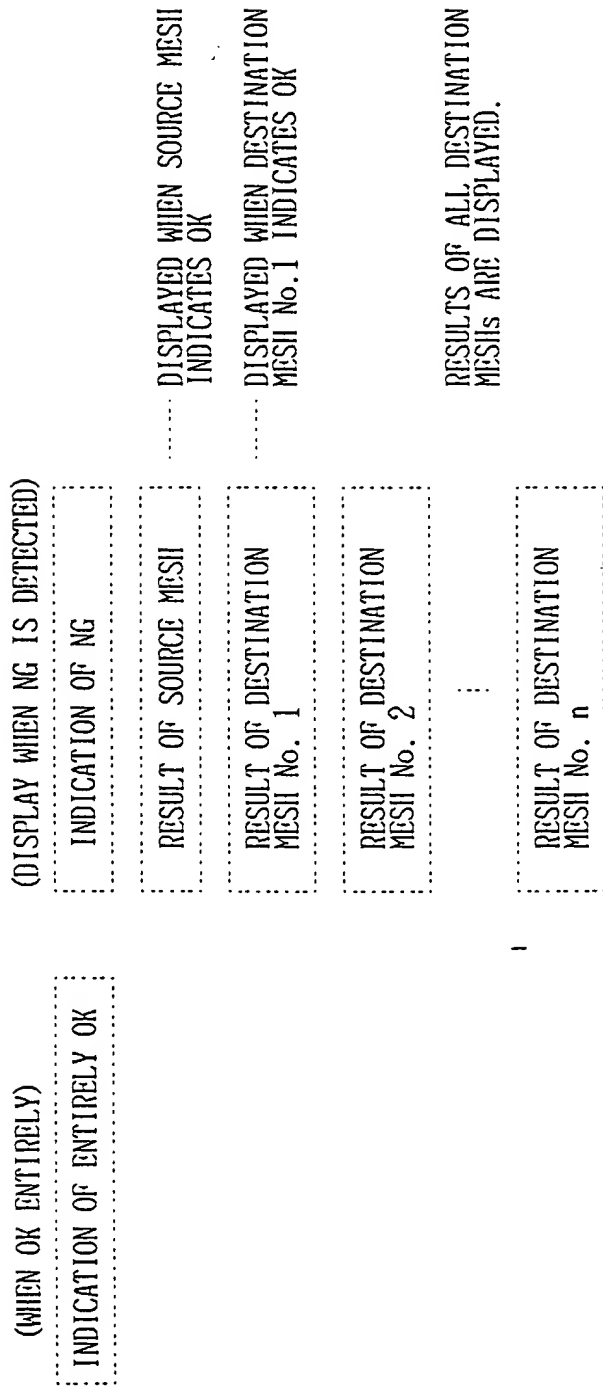


FIG. 473

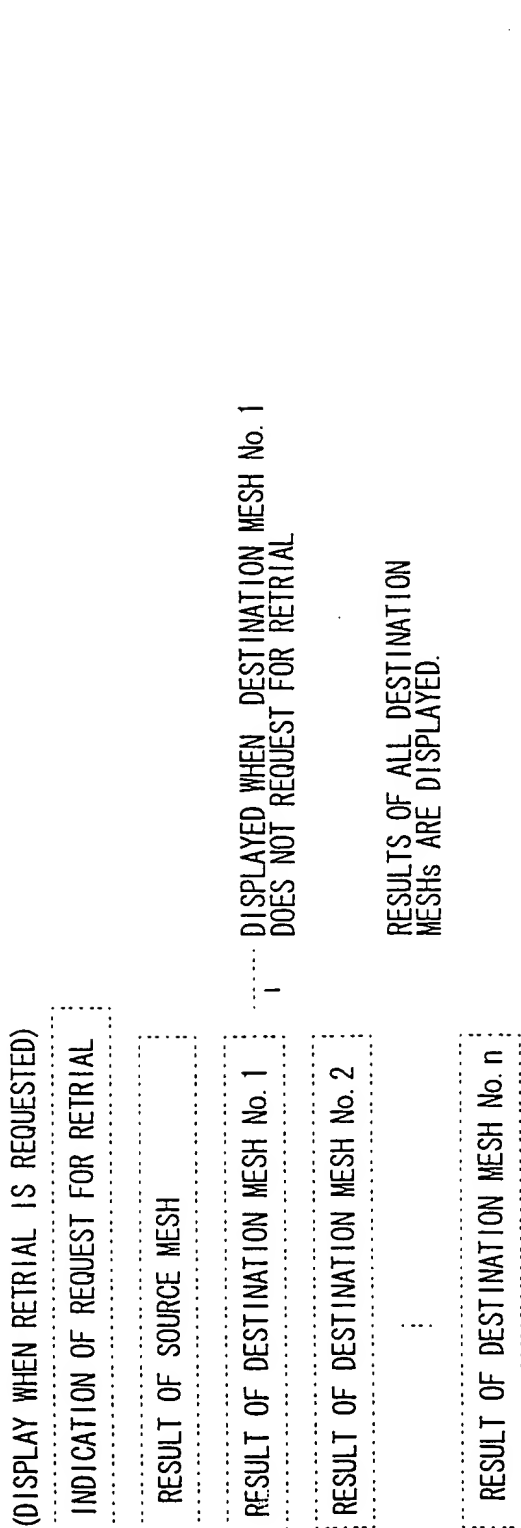
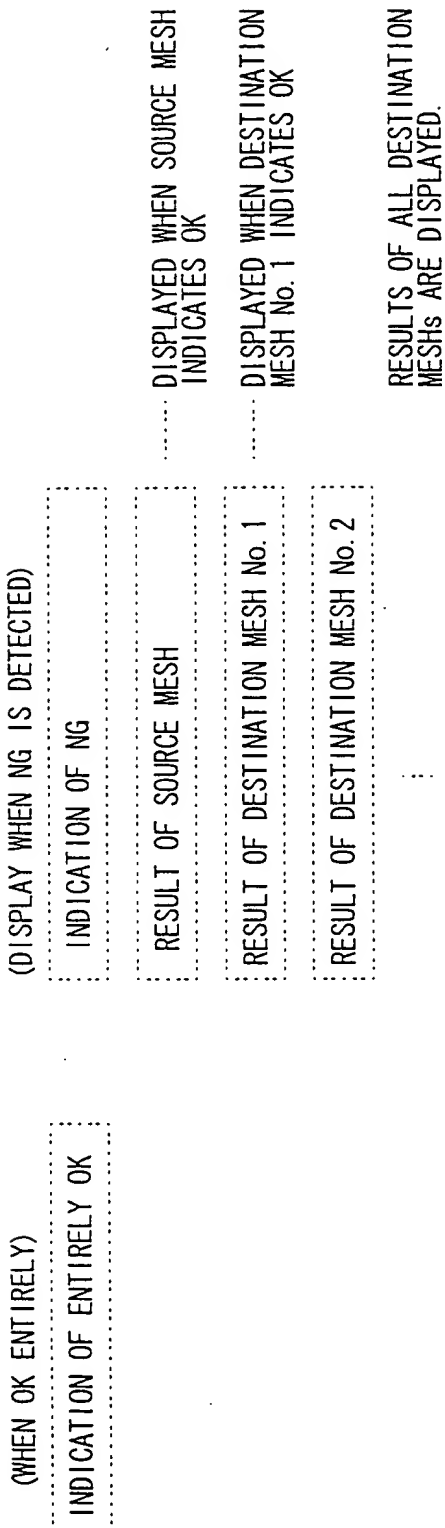


FIG. 474

	PURPOSE	USE	STORAGE POSITION	ACTIVATION METHOD	REPORT OF RESULT
CONSTRUCTION TP	CONFIRMING NORMALITY OF HARDWARE AFTER COMPLETION OF CONSTRUCTION	FOR ACTUAL CONSTRUCTION	BUILT IN ROM OF HSF05A	AT POWER SUPPLY (INSERTING PWCB INTO SBMESH)	OK/NG INDICATION ON 7 SEG LED
FIRST TEST OF TP	HSF05A CONFIRMING UNIT OPERATION	FIRST TEST UNIT TEST		DIP-SW 01 = ON DIP-SW 02 = ON + ① AT POWER SUPPLY ② RESET SW ON	OK/NG INDICATION ON 7 SEG LED
THIRD TEST OF TP	FOR DEVICE TEST AT DELIVERY FROM FACTORY	MHCOM DELIVERY TEST		DIP-SW 01 = ON DIP-SW 02 = OFF + ① AT POWER SUPPLY ② RESET SW ON	OK/NG INDICATION ON 7 SEG LED
DP	FOR ONLINE DIAGNOSTICS	ON-LINE		AUTOMATIC DIAG- NOSTICS WHEN FAULT OCCURS COMMAND DIAGNOS- TICS	OK/NG INDICATION ON 7 SEG LED REPORT DIAGNOS- TICS RESULT TO COM-E-MSCN

FIG. 475

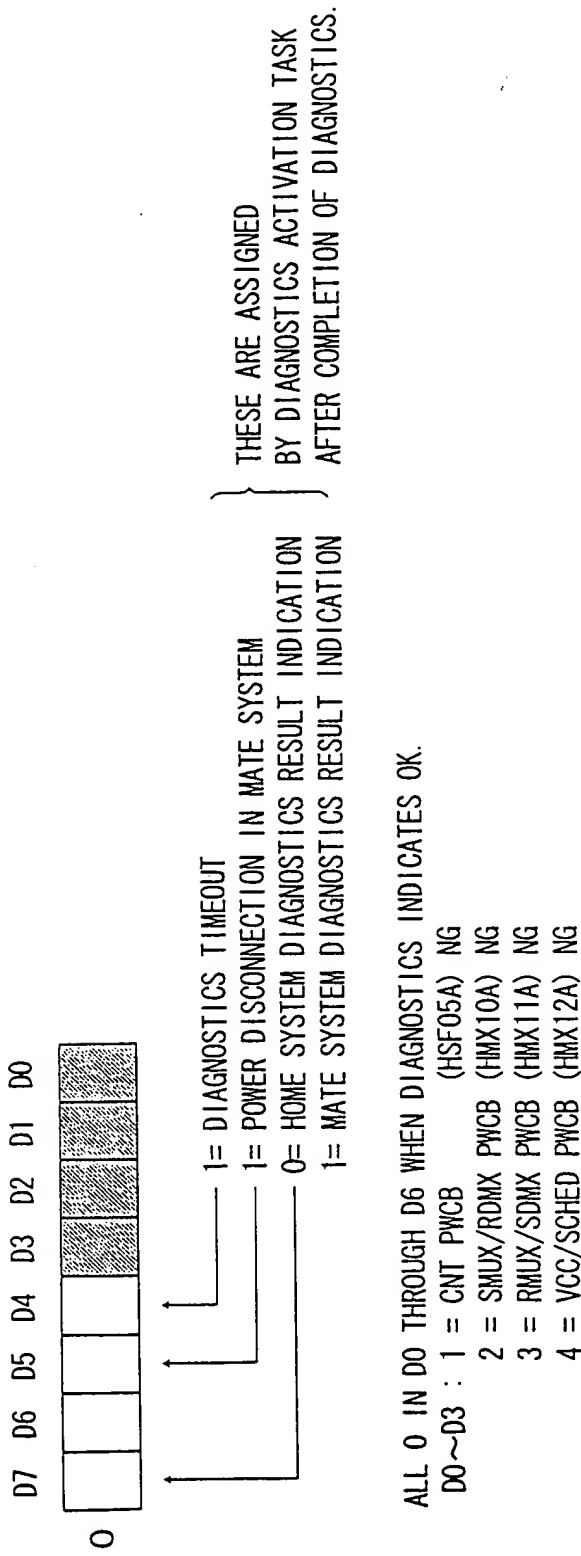


FIG. 477

0090000000000000

D7 D6 D5 D4 D3 D2 D1 D0

--	--	--	--	--	--	--	--

1

FIG. 478

D7

D0

2	D _i LOWER ORDER BYTE (D7~D0)
3	D _i HIGHER ORDER BYTE (D15~D8)
4	A _x LOWER ORDER BYTE (D7~D0)
5	A _x HIGHER ORDER BYTE (D15~D8)
6	B _x LOWER ORDER BYTE (D7~D0)
7	B _x HIGHER ORDER BYTE (D15~D8)
8	C _x LOWER ORDER BYTE (D7~D0)
9	C _x HIGHER ORDER BYTE (D15~D8)
~ Don' t care ~	
F	

FIG. 479

0	3	4	7	8	11	12	15	16	19	20	23	24	27	28	31
*1		don't care													
phase No. area		sub-phase No. area				test No. area									
HMX10A	HMX11A	HMX12A	HSF05A	HMH00A	HMH01A	HMH02A	HMH03A	SUSPECT PRIORITY DISPLAY AREA (HOME SYSTEM)							
HMH04A	HMH05A	HMH06A	HLP02A	HLM00A	HLM01A	HLM02A	HMH03A								
HMX10A	HMX11A	HMX12A	HSF05A	HMH00A	HMH01A	HMH02A	HMH03A								
HMH04A	HMH05A	HMH06A	HLP02A	HLM00A	HLM01A	HLP01A	HMH03A								

FIG. 480

0	MSCN area 64 bit	31	IMH00A area 128 bit
8	MSD echo-back area 64 bit		
10	MSCN area 64 bit		IMH01A area 128 bit
18	MSD echo-back area 64 bit		
20	MSCN area 64 bit		IMH02A area 128 bit
28	MSD echo-back area 64 bit		
30	MSCN area 64 bit		IMH03A area 128 bit
38	MSD echo-back area 64 bit		
40	MSCN area 64 bit		IMH04A area 128 bit
48	MSD echo-back area 64 bit		
50	MSCN area 64 bit		IMH05A area 128 bit
58	MSD echo-back area 64 bit		
60	MSCN area 64 bit		IMH06A area 128 bit
68	MSD echo-back area 64 bit		
70	MSCN area 64 bit		ILM00A area 128 bit
78	MSD echo-back area 64 bit		
80	MSCN area 64 bit		ILM01A area 128 bit
88	MSD echo-back area 64 bit		
90	MSCN area 64 bit		ILP02A area 128 bit
98	MSD echo-back area 64 bit		

FIG. 482

ROW	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	RESETTING MATE SYSTEM	RESETTING HOME SYSTEM						
1					PRESENT OS	MATE SYSTEM SHALM	MATE SYSTEM SHOS	MATE SYSTEM OS
2						SELECTING OL2B	HOME SYSTEM DIAGNOSTICS ACTIVATION	SELECTING OL2A MATE SYSTEM DIAGNOSTICS ACTIVATION
3								
4								
5	SPECIFYING INTRA-STATION LAP BAND							
6	(SPECIFYING VALUE n FOR 64 KBPS X n. VARIABLE 1~4075)							
7								LSB
23								
24					DEMUX START OF STATISTICS		15-MINUTE NOTIFICATION	MUX START OF STATISTICS
25							15-MINUTE NOTIFICATION	MUX START OF STATISTICS
26			1		DEMUX START OF STATISTICS			
27								
31								
32					DEMUX START OF STATISTICS		15-MINUTE NOTIFICATION	MUX START OF STATISTICS
33								
35								

h-SIG

R-TCG

RMLP

SMLP

FIG. 484

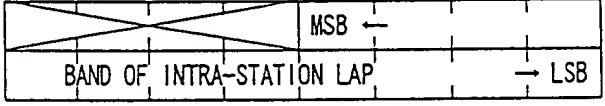
POINT NAME	STORAGE POSITION	EXPLANATION
RESETTING MATE SYSTEM	0 ROW D7	RESET INSTRUCTION POINT OF MATE SYSTEM MHCOM. AUTOMATIC RESET POINT. SETTING THIS POINT DISCONNECTS INTRA-STATION COMMUNICATIONS LAP.
RESETTING HOME SYSTEM	0 ROW D6	RESET INSTRUCTION POINT OF HOME SYSTEM MHCOM. AUTOMATIC RESET POINT. SETTING THIS POINT DISCONNECTS INTRA-STATION COMMUNICATIONS LAP.
PRESENT OS	1 ROW D3	LIGHTING LAMP INDICATING PRESENT OS BY SETTING THIS POINT.
MATE SYSTEM SHALM	1 ROW D2	LIGHTING LAMP (ACCOMMODATED IN HPT01A) INDICATING MATE SYSTEM SHELF ALM BY SETTING THIS POINT.
MATE SYSTEM SHOS	1 ROW D1	LIGHTING LAMP (ACCOMMODATED IN HPT01A) INDICATING MATE SYSTEM SHELF OS BY SETTING THIS POINT.
MATE SYSTEM SHOS	1 ROW D0	LIGHTING LAMP (ACCOMMODATED IN HSF05A) INDICATING MATE SYSTEM MHCOM OS BY SETTING THIS POINT.
SELECTING OL2B	2 ROW D1	COMPULSORILY SELECTING OPTICAL 8MCLK #1 BY CHANGING THIS POINT FROM RESET TO SET.
SELECTING OL2A	2 ROW D0	COMPULSORILY SELECTING OPTICAL 8MCLK #0 BY CHANGING THIS POINT FROM RESET TO SET.
HOME SYSTEM DIAGNOSTICS ACTIVATION	3 ROW D1	PERFORMING ONLINE DP IN HOME SYSTEM BY CHANGING THIS POINT FROM RESET TO SET. IF HOME SYSTEM IS ACT, IT IS NOT PERFORMED.
MATE SYSTEM DIAG- NOSTICS ACTIVATION FIFO FULL	3 ROW D0	REQUESTING MATE SYSTEM TO PERFORM ONLINE DP IN HOME SYSTEM BY CHANGING THIS POINT FROM RESET TO SET. IF MATE SYSTEM IS ACT, THE REQUEST IS IGNORED.
	5 ~6 ROW	<p>• SPECIFYING BAND OF INTRA-STATION LAP.</p> <p>D7 D0</p>  <p>SPECIFYING n FOR 64 Kbps $\times n$ ($n=1 \sim 4075$) DEFAULT IS $n = 1$</p>
SDMX 15-MINUTE NOTIFICATION	24 ROW D4	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF SDMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
SDMX START OF STATISTICS	24 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF SDMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
SMUX 15-MINUTE NOTIFICATION	24 ROW D1	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF SMUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
SMUX START OF STATISTICS	24 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF SMUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
RMUX 15-MINUTE NOTIFICATION	25 ROW D1	15-MINUTE NOTIFICATION FOR STATISTIC PROCESS OF RMUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
RMUX START OF STATISTICS	25 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF RMUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.

FIG. 485

POINT NAME	STORAGE POSITION	EXPLANATION
RTCG-DMX 15-MINUTE NOTIFICATION	26 ROW D4	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF RTCG-DMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
RTCG-MDX START OF STATISTICS	26 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF RTCG-DMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-DMX 15-MINUTE NOTIFICATION	32 ROW D4	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF HOME SIG-DMX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-DMX START OF STATISTICS	32 ROW D3	INSTRUCTING TO START STATISTIC PROCESS OF SIG-DMX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-MUX 15-MINUTE NOTIFICATION	32 ROW D1	15-MINUTE NOTIFICATION FOR STATISITC PROCESS OF HOME SIG-MUX. STATISTIC DATA IS COLLECTED BY CHANGING THIS POINT FROM RESET TO SET.
HOME SIG-MUX START OF STATISTICS	32 ROW D0	INSTRUCTING TO START STATISTIC PROCESS OF SIG-MUX. STATISTICS IS STARTED BY CHANGING THIS POINT FROM RESET TO SET.

F I G. 486

0927243 092909

0000000000000000

ROW	D7	D6	D5	D4	D3	D2	D1	D0
36								
37								
38			DMUX	MUX	Unit No.			
39					Q1			
40					QA			
41					QA'			
42					QB			
43					QB'			
44					QC			
45					QC'			
46					QD			
47					QD'			
48	0	0	0	0	SPECIFIC VCI			
49					SPECIFIC VCI			
50					SPECIFIC VCI			
51					SPECIFIC VCI			

FIG. 487

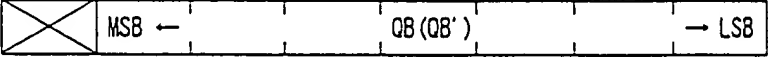
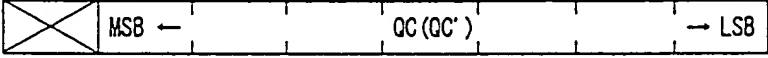
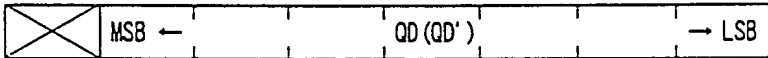

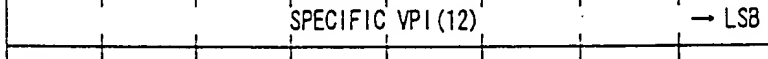

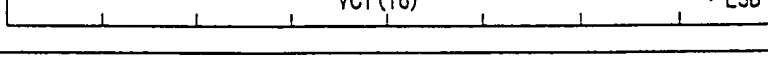
POINT NAME	STORAGE POSITION	EXPLANATION
QB, QB' (DISCARD START/RE- LEASE THRE- SHOLD FOR CELL OF P=0, CON=1.)	42, 43ROW	<p>• QB ... DISCARD START THRESHOLD FOR CELL OF P=0, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QB, DISCARD OF CELL OF P=0, CON=1 IS STARTED.</p> <p>• QB' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=0, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QB', DISCARD OF CELL OF P=0, CON=1 IS RELEASED.</p> <p>ROW D7 D0</p> <p>42 (43) </p> <p>※ DEFAULT IS MAXIMUM VALUE (112 CELLS). 0 < QB' ≤ QB</p>
QC, QC' (DISCARD START/RE- LEASE THRE- SHOLD FOR CELL OF P=1, CON=0.)	42, 43ROW	<p>• QC ... DISCARD START THRESHOLD FOR CELL OF P=1, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QC, DISCARD OF CELL OF P=1, CON=0 IS STARTED.</p> <p>• QC' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=1, CON=0 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QC', DISCARD OF CELL OF P=1, CON=0 IS RELEASED.</p> <p>ROW D7 D0</p> <p>44 (45) </p> <p>※ DEFAULT IS MAXIMUM VALUE (112 CELLS). 0 < QC' ≤ QC</p>
QD, QD' (DISCARD START/RE- LEASE THRE- SHOLD FOR CELL OF P=1, CON=1.)	42, 43ROW	<p>• QD ... DISCARD START THRESHOLD FOR CELL OF P=1, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER EXCEEDS QD, DISCARD OF CELL OF P=1, CON=1 IS STARTED.</p> <p>• QD' ... DISCARD RELEASE THRESHOLD FOR CELL OF P=1, CON=1 FOR POINT SPECIFIED BY 38 ROW. IF USE OF BUFFER DOES NOT EXCEEDS QD', DISCARD OF CELL OF P=1, CON=1 IS RELEASED.</p> <p>ROW D7 D0</p> <p>46 (47) </p> <p>※ DEFAULT IS MAXIMUM VALUE (112 CELLS). 0 < QD' ≤ QD</p>
SPECIFIC VPI/VCI	48 51 ROW	<p>• SPECIFYING SPECIFIC VPI/VCI TO MONITOR NUMBER OF PASSING CELLS IN POINT SPECIFIED BY 38ROW.</p> <p>ROW D7 D0</p> <p>48 </p> <p>49 </p> <p>50 </p> <p>51 </p>

FIG. 489

669220" E7C22250

POINT NAME	STORAGE POSITION	EXPLANATION																																																											
SPECIFYING MASK	180 { 195 ROW	· SPECIFYING MASK PATTERN OF COM-E- MSCN IN WORD UNIT.																																																											
		<table><tr><th>E-MSD ROW No.</th><th>BIT POSITION</th><th>ROW NO. OF MASKED E-MSCN</th></tr><tr><td>180</td><td>D0</td><td>0. 1</td></tr><tr><td></td><td>1</td><td>2. 3</td></tr><tr><td></td><td>2</td><td>4. 5</td></tr><tr><td></td><td>3</td><td>6. 7</td></tr><tr><td></td><td>4</td><td>8. 9</td></tr><tr><td></td><td>5</td><td>10. 11</td></tr><tr><td></td><td>6</td><td>12. 13</td></tr><tr><td></td><td>7</td><td>14. 15</td></tr><tr><td>181</td><td>D0</td><td>16. 17</td></tr><tr><td>194</td><td>D7</td><td>238. 239</td></tr><tr><td>195</td><td>D0</td><td>240. 241</td></tr><tr><td></td><td>1</td><td>242. 243</td></tr><tr><td></td><td>2</td><td>244. 245</td></tr><tr><td></td><td>3</td><td>246. 247</td></tr><tr><td></td><td>4</td><td>248. 249</td></tr><tr><td></td><td>5</td><td>250. 251</td></tr><tr><td></td><td>6</td><td>252. 253</td></tr><tr><td></td><td>7</td><td>254. 255</td></tr></table>	E-MSD ROW No.	BIT POSITION	ROW NO. OF MASKED E-MSCN	180	D0	0. 1		1	2. 3		2	4. 5		3	6. 7		4	8. 9		5	10. 11		6	12. 13		7	14. 15	181	D0	16. 17	194	D7	238. 239	195	D0	240. 241		1	242. 243		2	244. 245		3	246. 247		4	248. 249		5	250. 251		6	252. 253		7	254. 255		
E-MSD ROW No.	BIT POSITION	ROW NO. OF MASKED E-MSCN																																																											
180	D0	0. 1																																																											
	1	2. 3																																																											
	2	4. 5																																																											
	3	6. 7																																																											
	4	8. 9																																																											
	5	10. 11																																																											
	6	12. 13																																																											
	7	14. 15																																																											
181	D0	16. 17																																																											
194	D7	238. 239																																																											
195	D0	240. 241																																																											
	1	242. 243																																																											
	2	244. 245																																																											
	3	246. 247																																																											
	4	248. 249																																																											
	5	250. 251																																																											
	6	252. 253																																																											
	7	254. 255																																																											
		※ "1" INDICATES MASKING.																																																											

FIG. 491

MHCOM

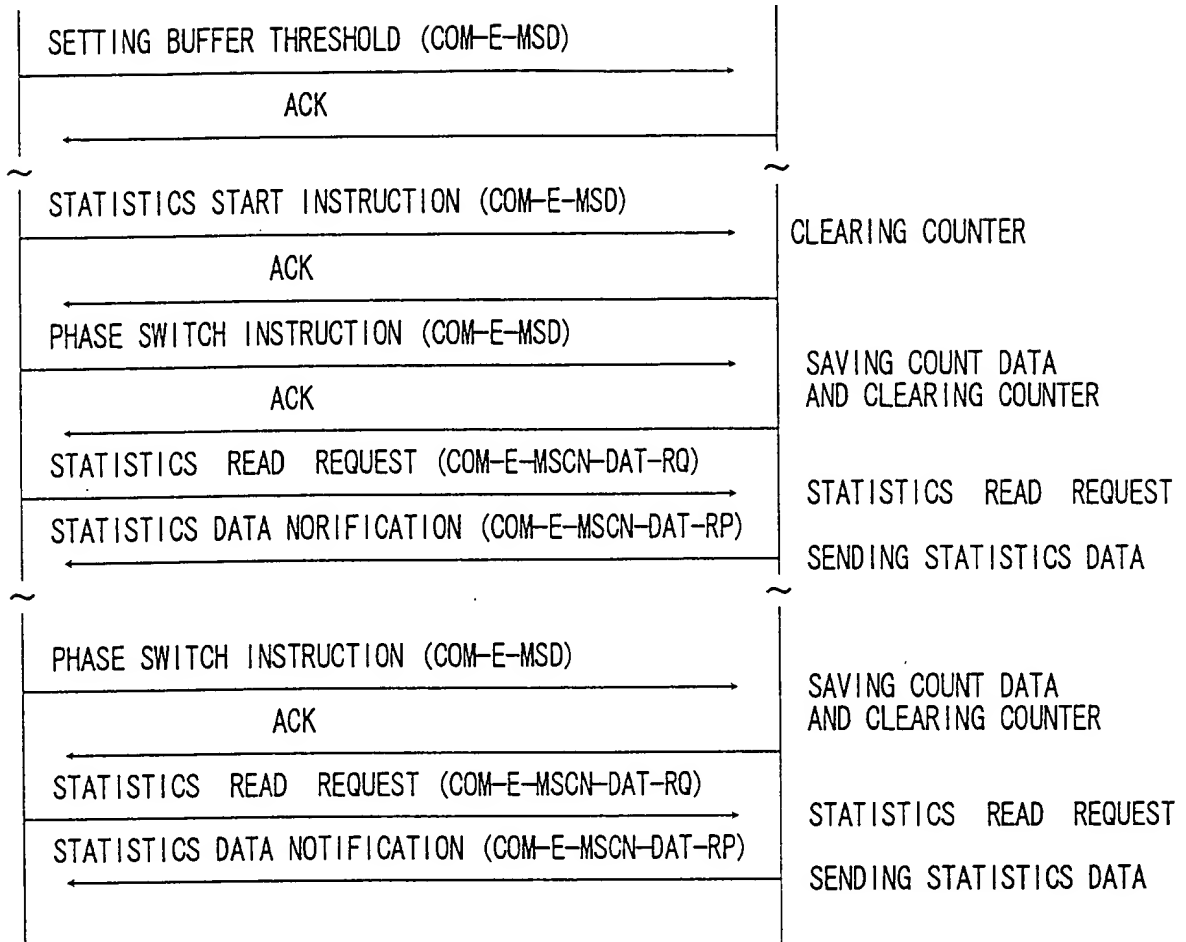


FIG. 492

[illegible]

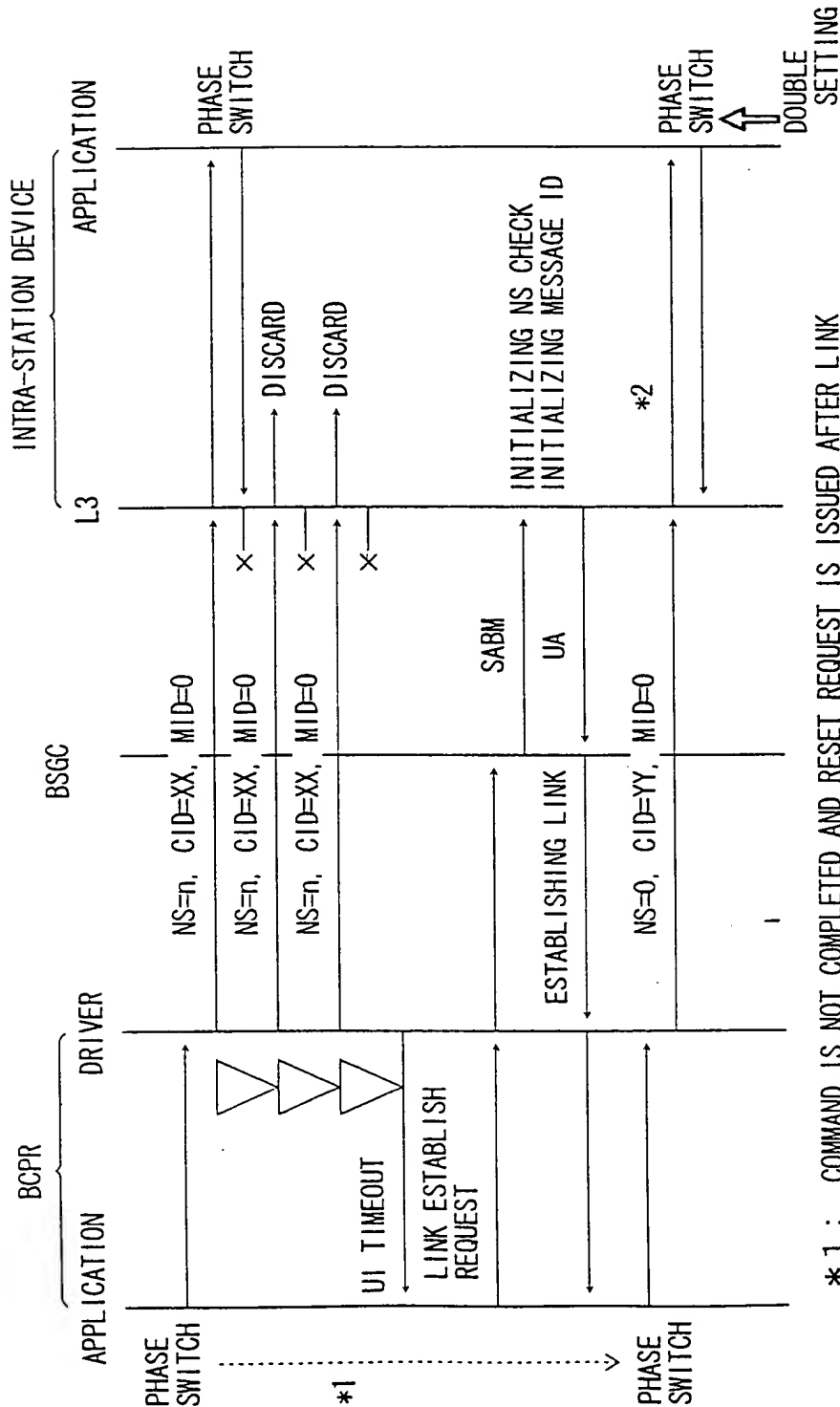
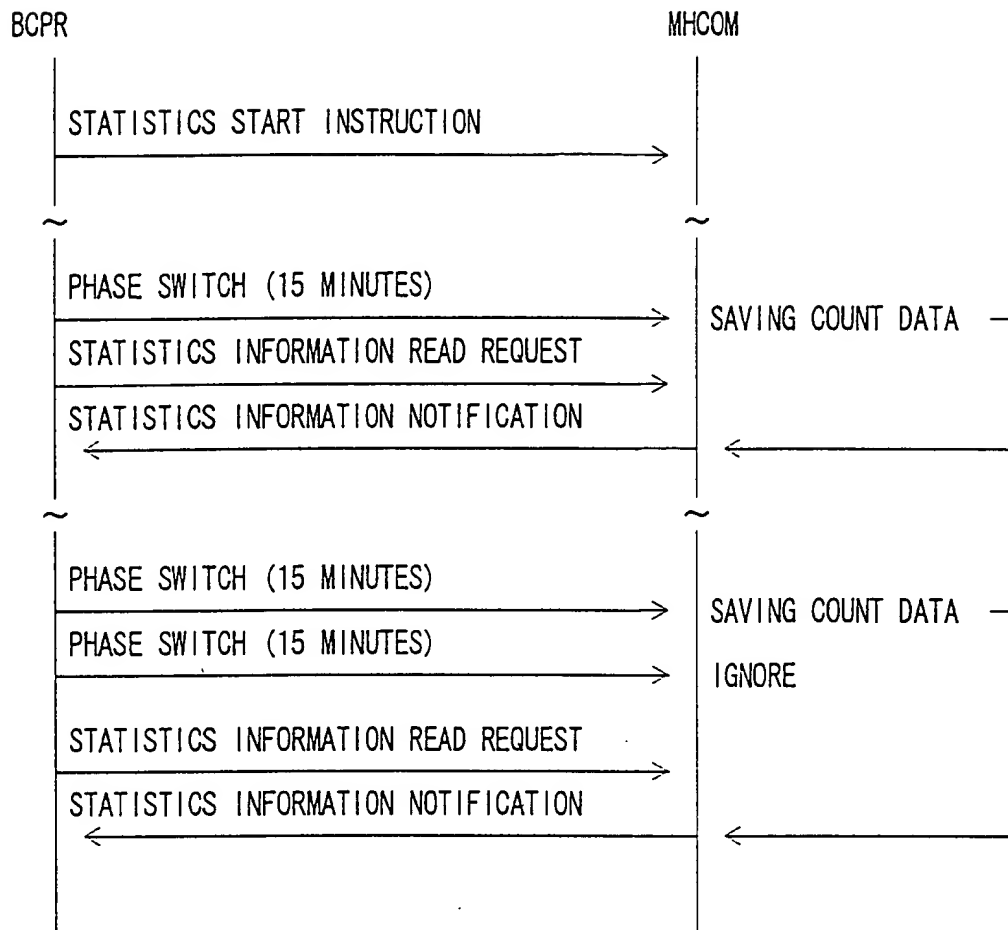


FIG. 493

009220" 6122260



F I G. 494

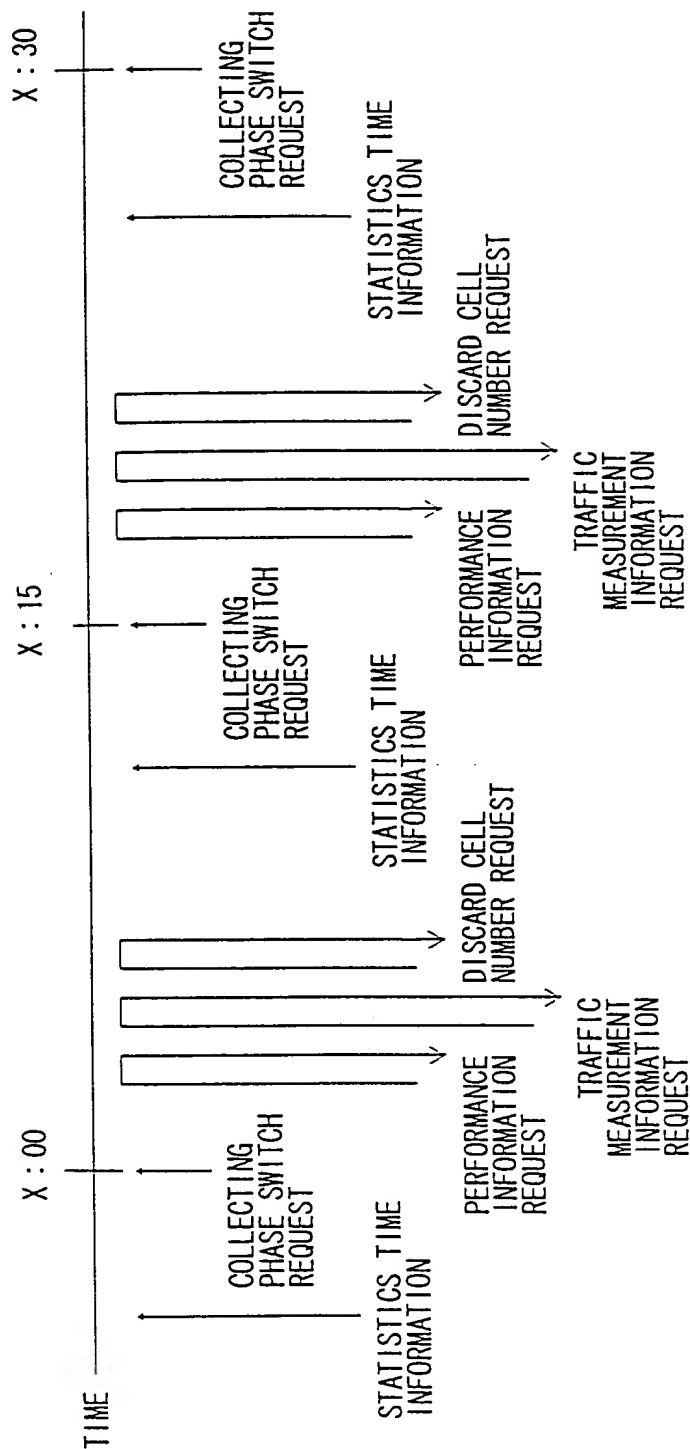


FIG. 495

669360-24260

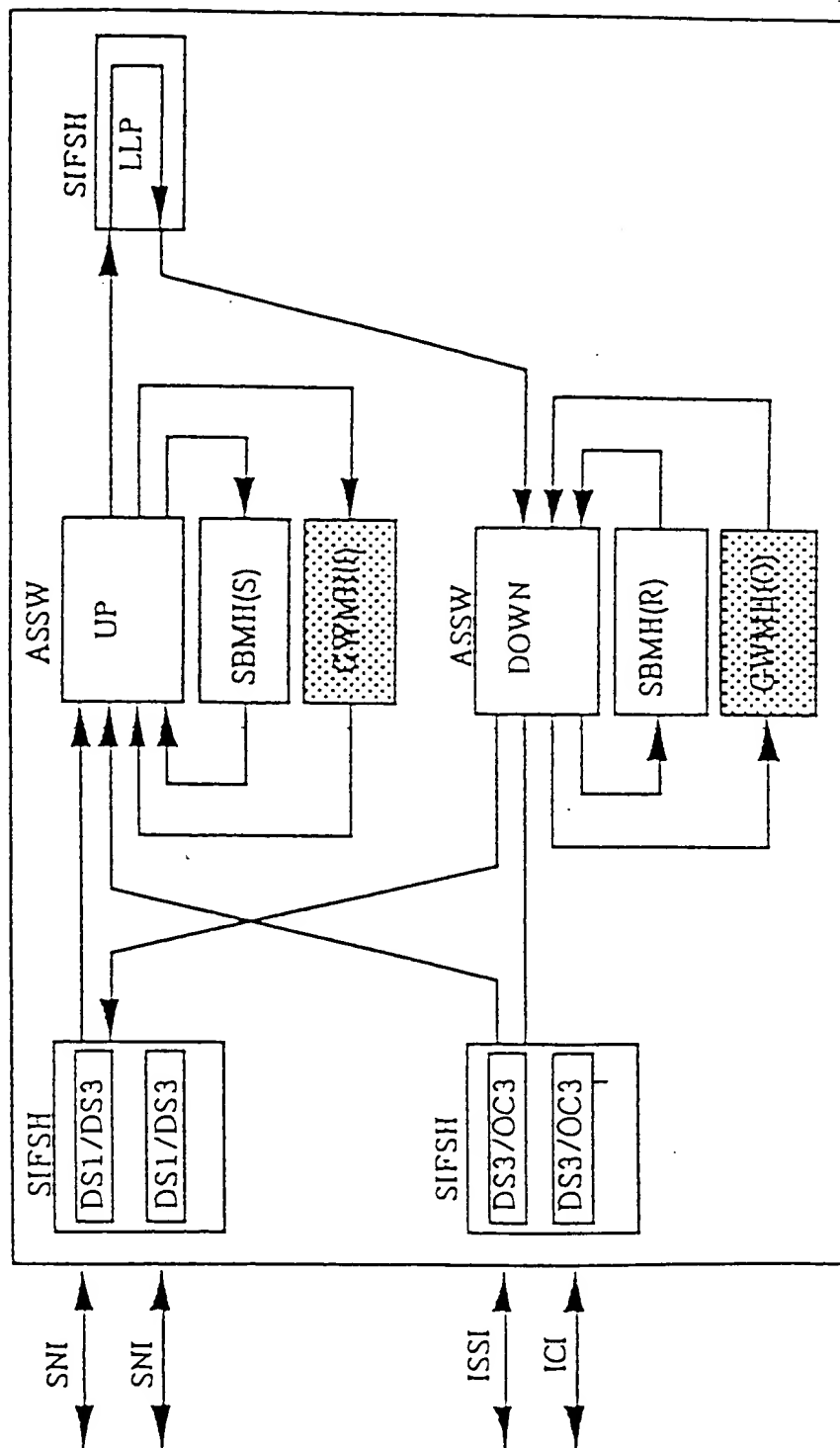


FIG. 496

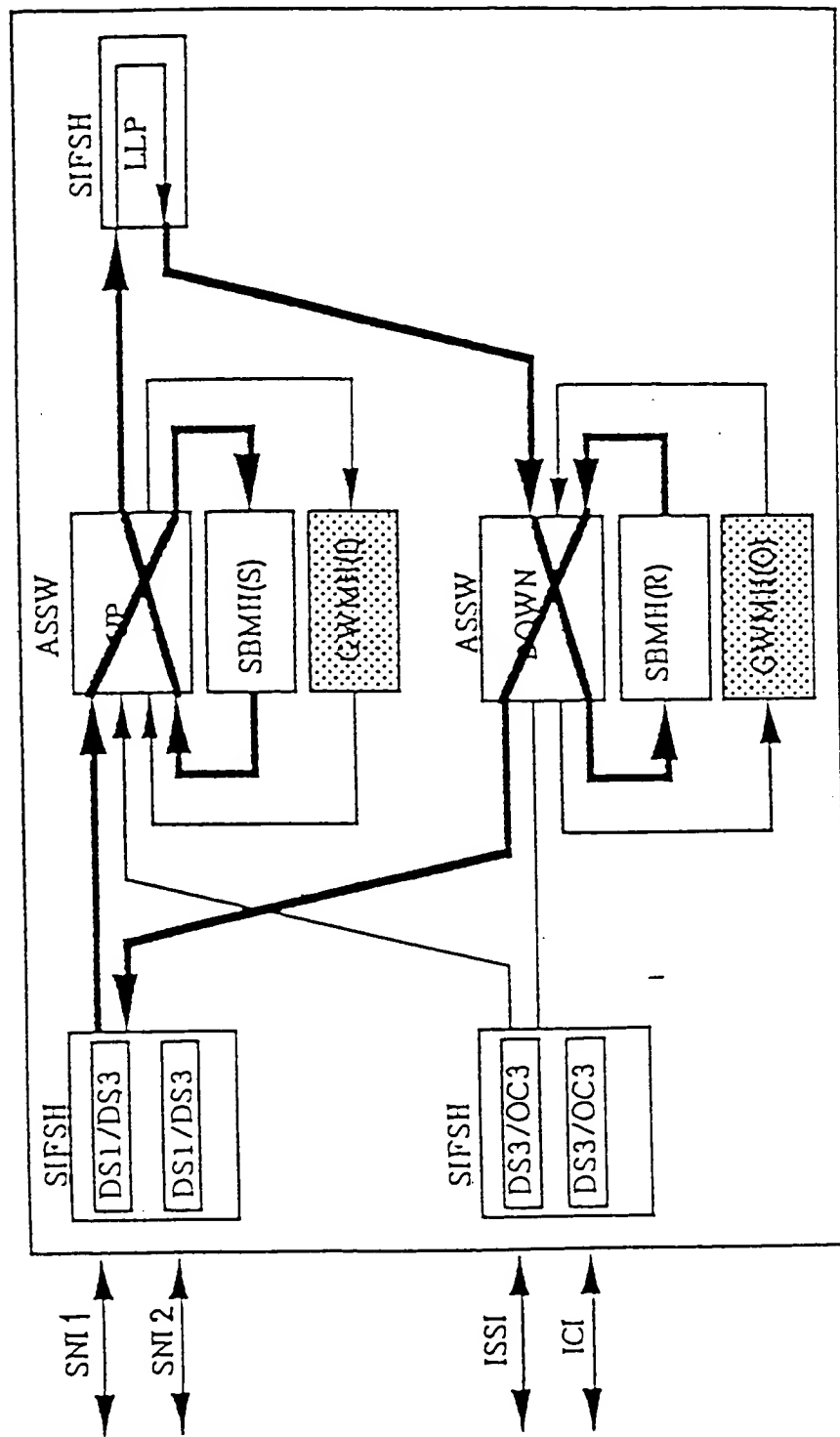


FIG. 497

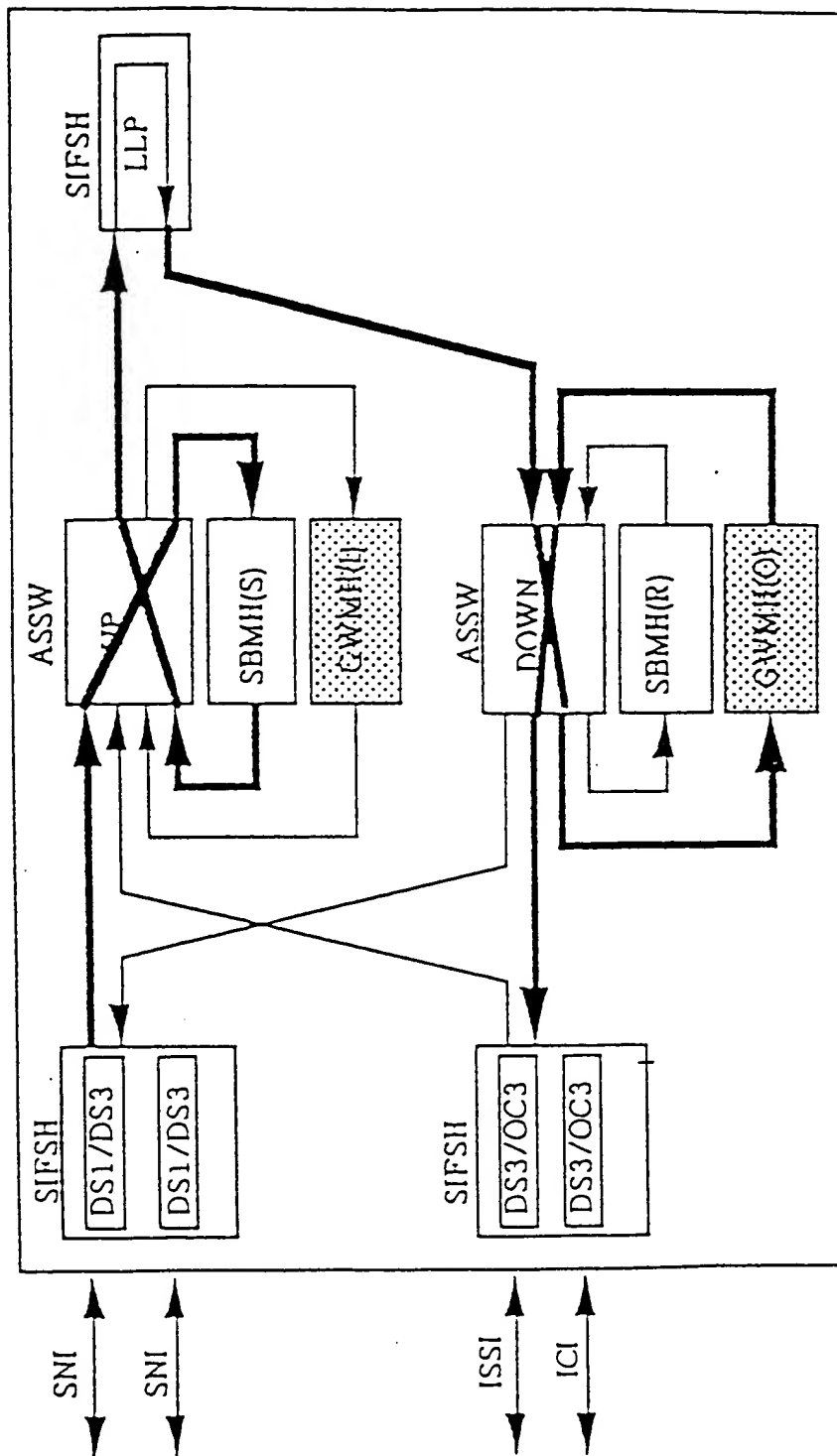


FIG. 498

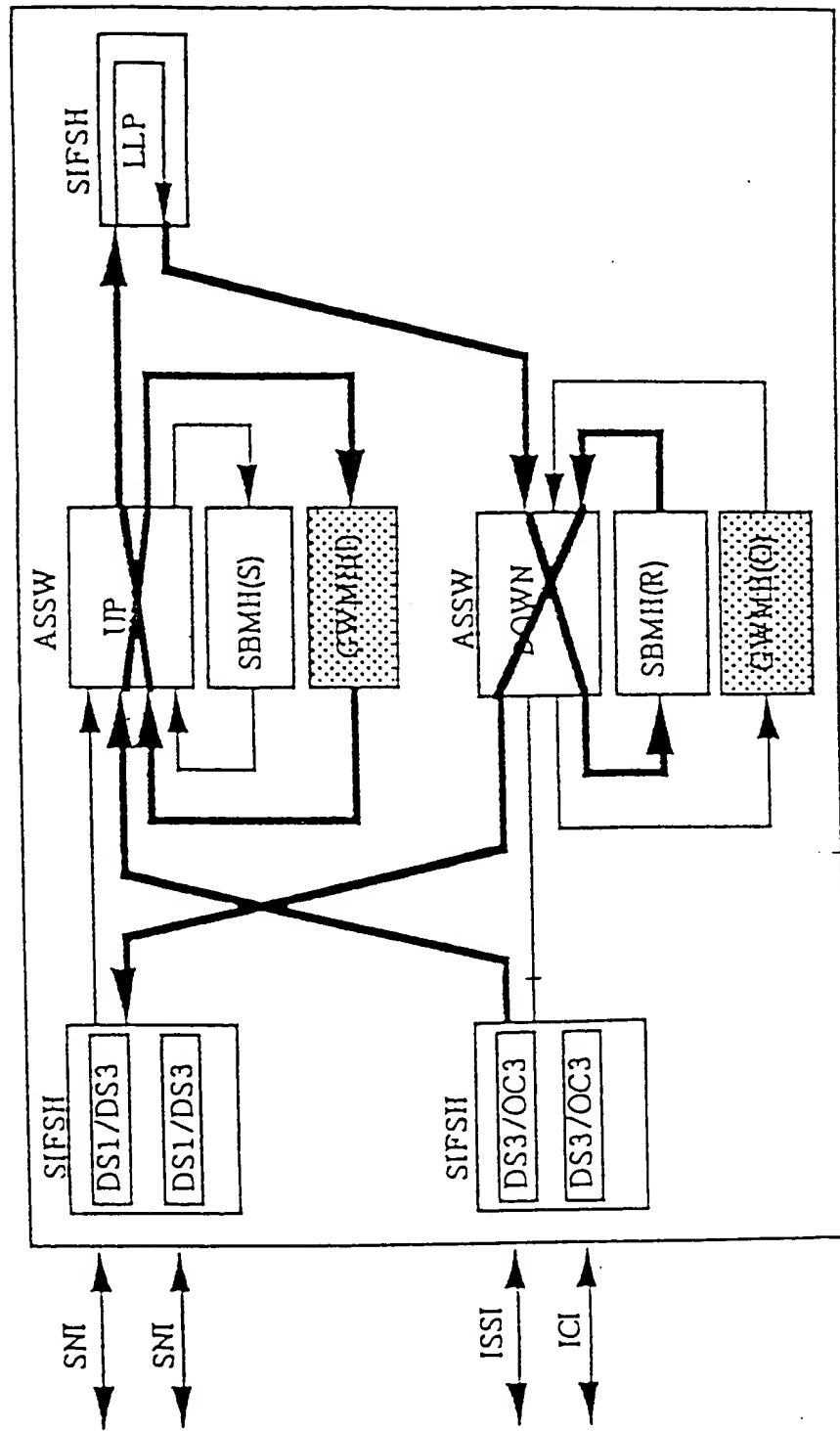


FIG. 499

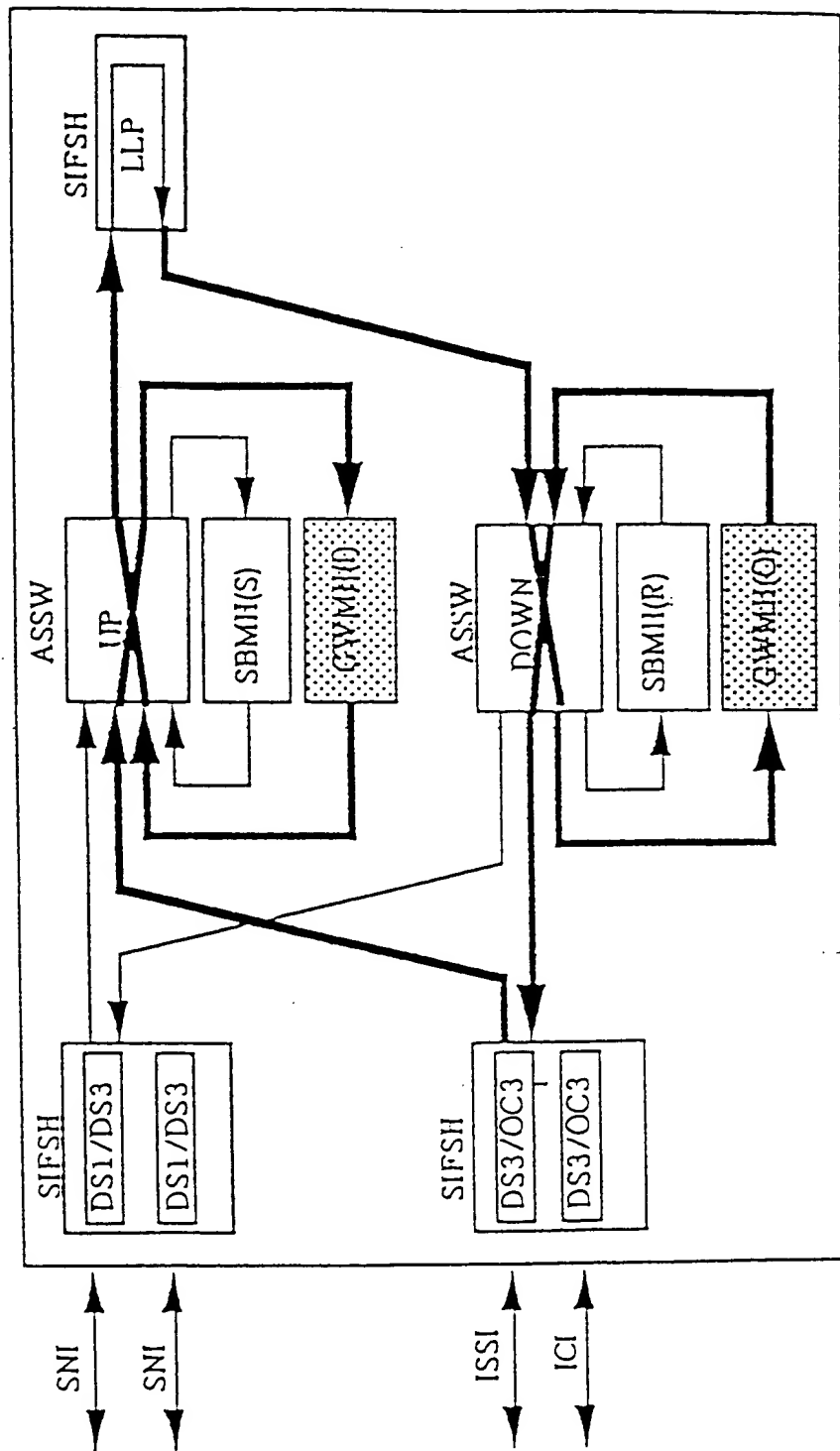


FIG. 500

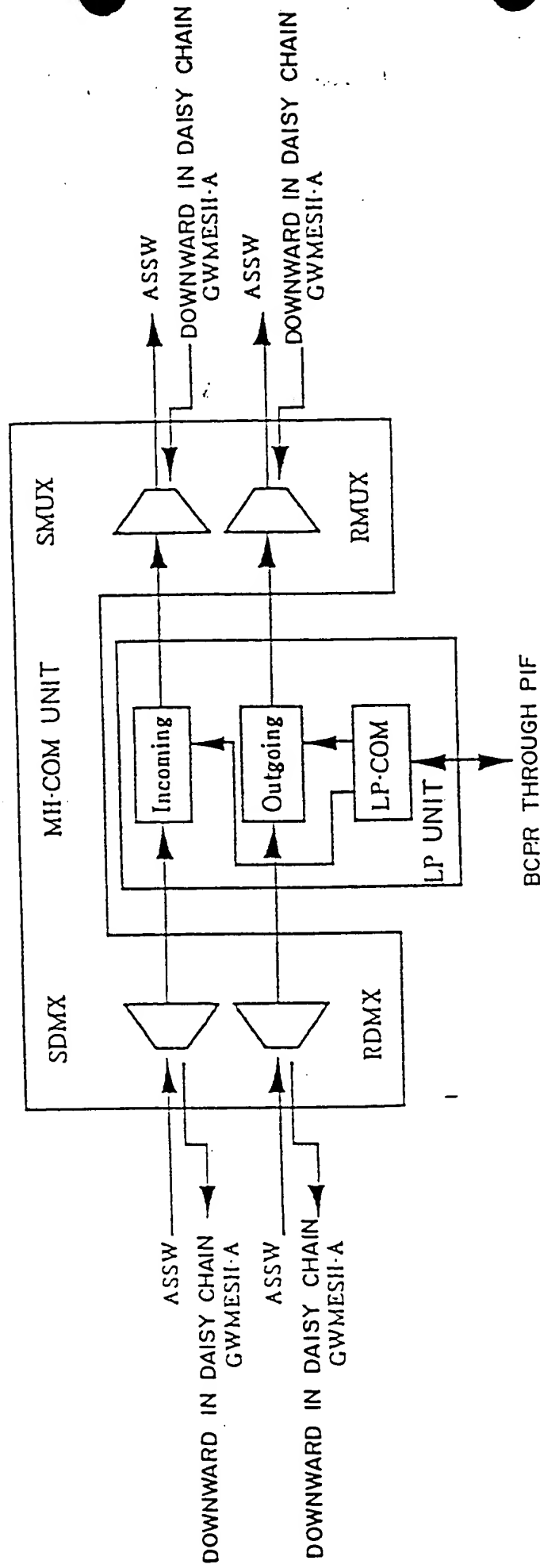


FIG. 501

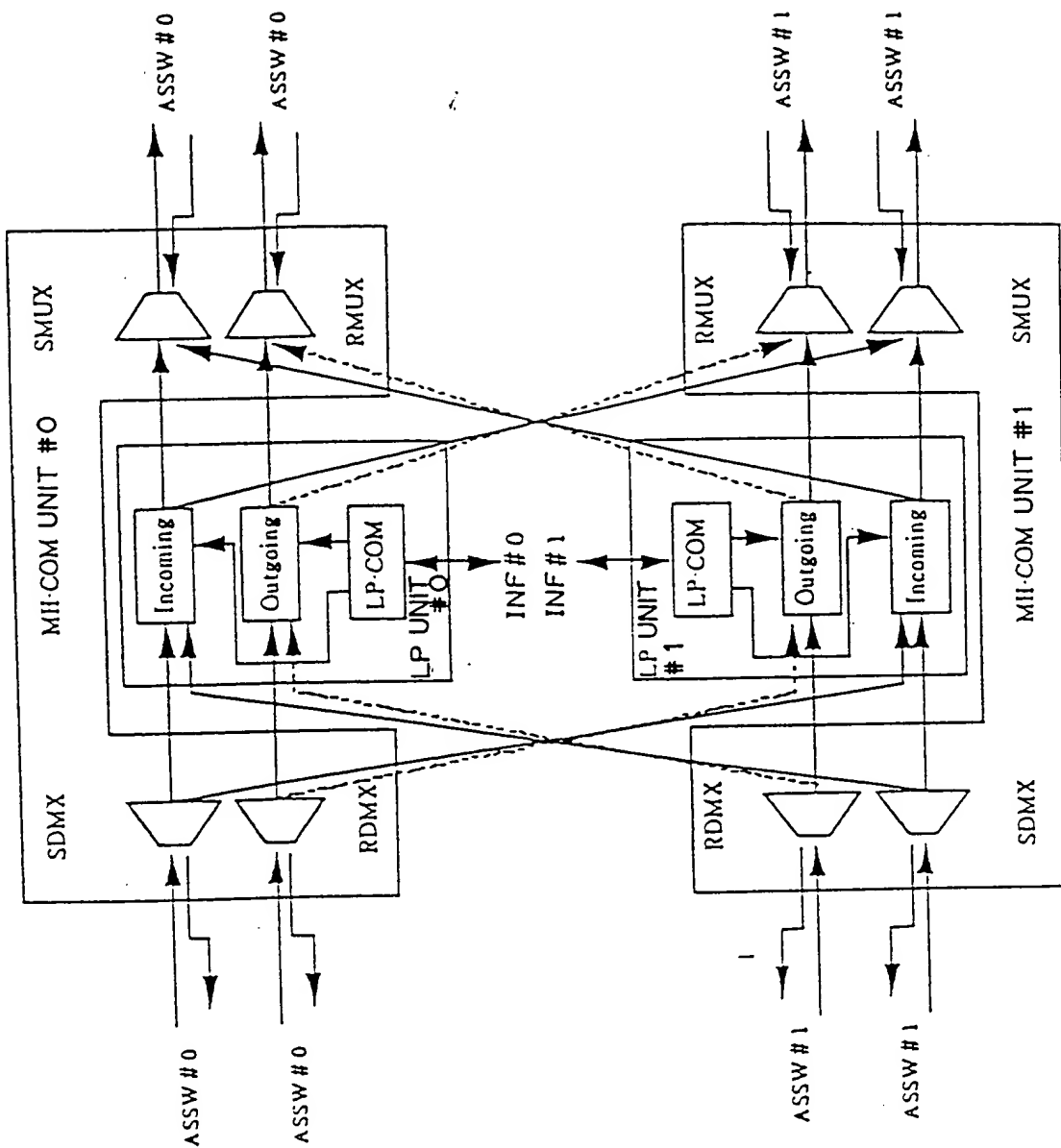
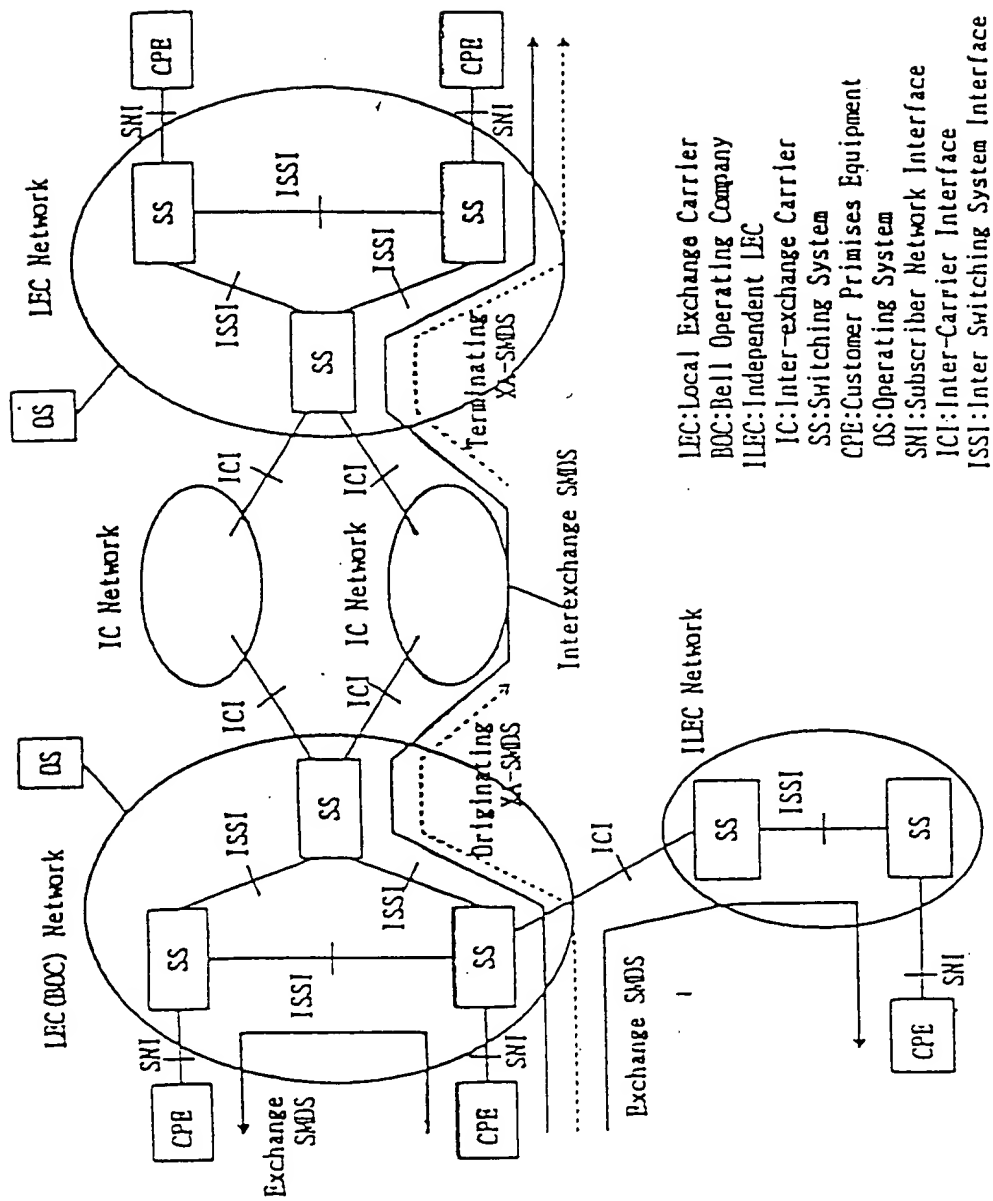


FIG. 502

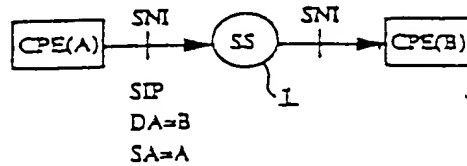


LEC: Local Exchange Carrier
 BOC: Bell Operating Company
 ILEC: Independent LEC
 IC: Inter-exchange Carrier
 SS: Switching System
 CPE: Customer Premises Equipment
 OS: Operating System
 SNI: Subscriber Network Interface
 ICI: Inter-carrier Interface
 ISSI: Inter-switching System Interface

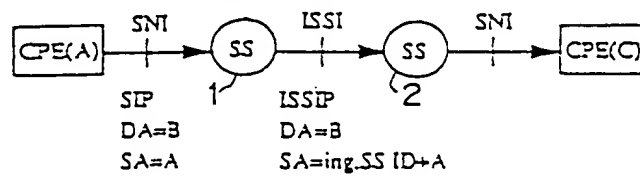
FIG. 503

Individual Address Routing (DATA IS TRANSMITTED AS BEING UNDIVIDED)

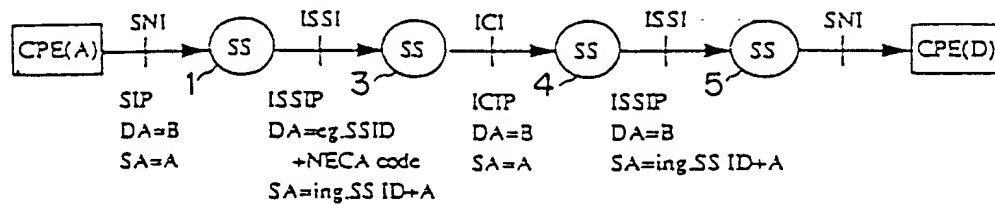
(1) COMMUNICATIONS IN SS



(2) COMMUNICATIONS IN LEC



(3) COMMUNICATIONS IN LATA EXTERNAL TO LEC



(4) COMMUNICATIONS EXTERNAL TO LATA

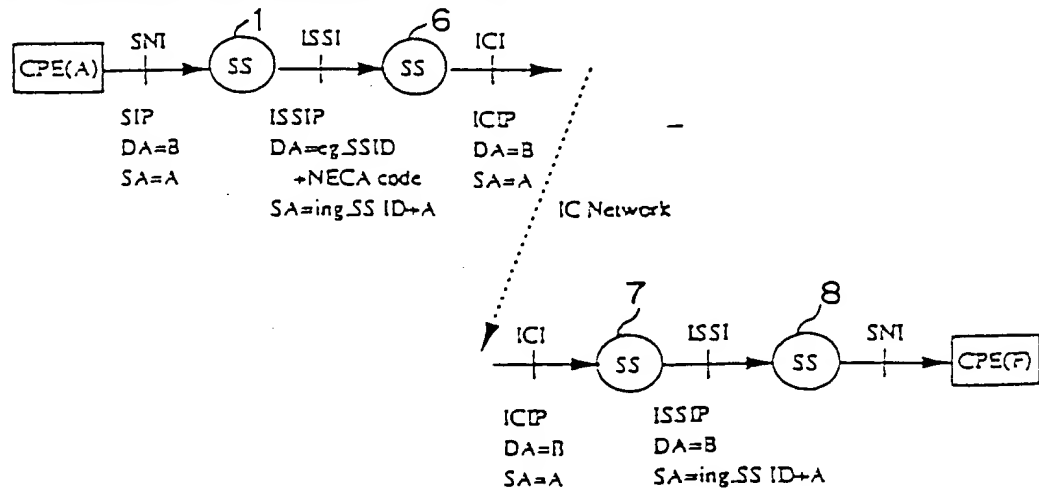


FIG. 504

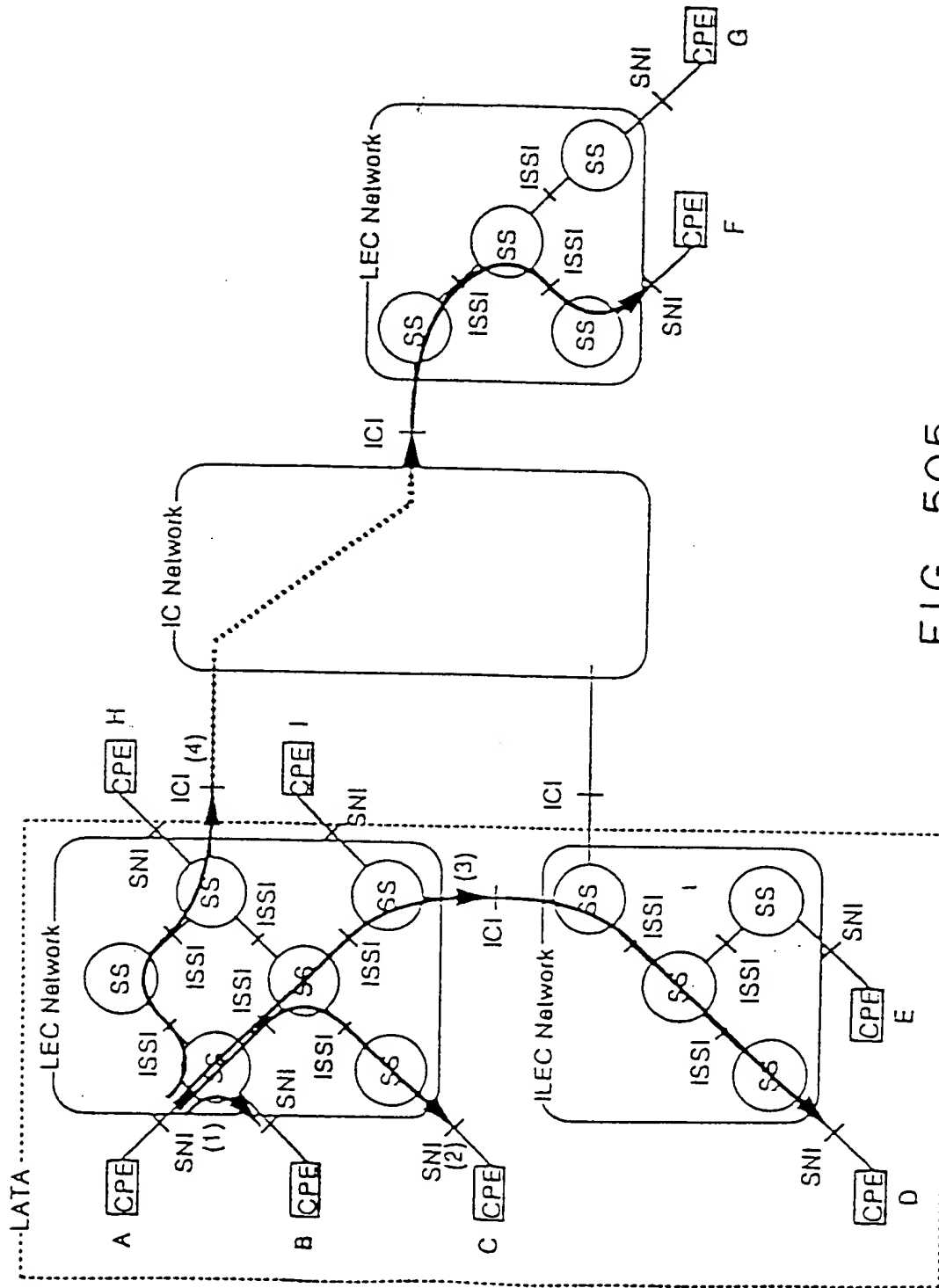
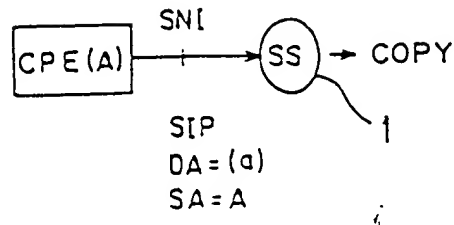
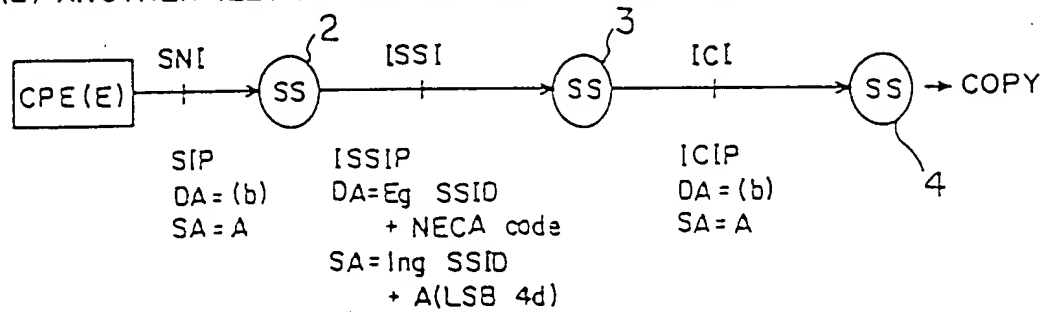


FIG. 505

(1) LEC OF HOME SYSTEM REFERS TO GAA GAA = (a)



(2) ANOTHER ILEC IN LATA REFERS TO GAA GAA = (b)



(3) GAA EXISTS IN OTHER THAN LATA GAA = (c)

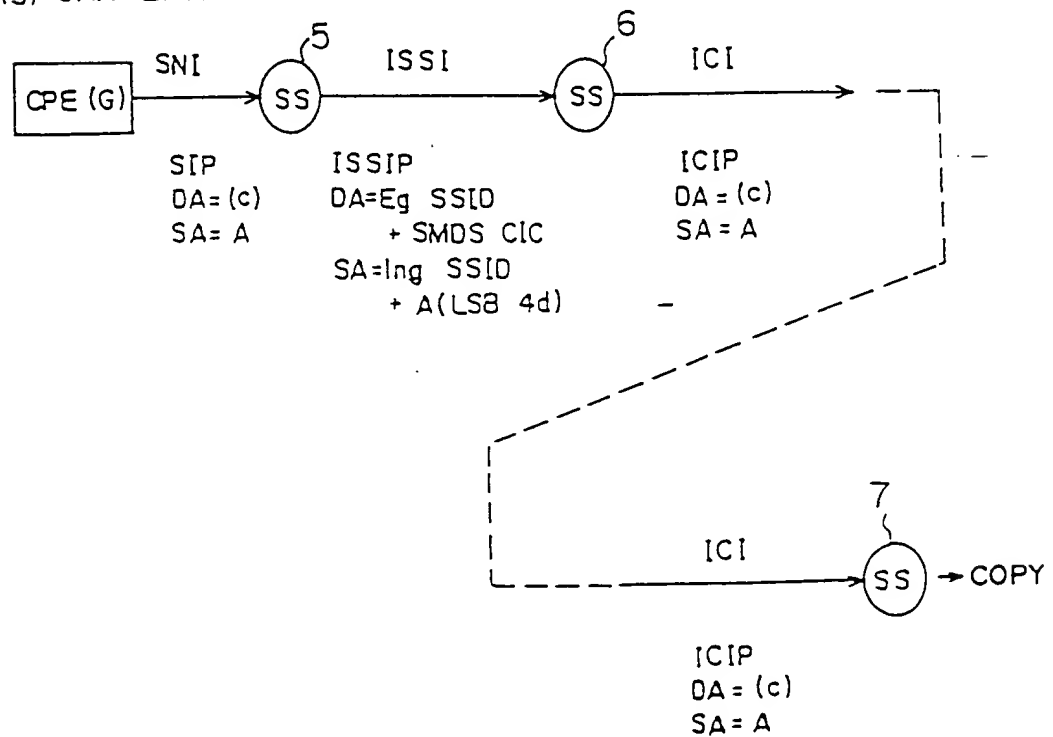


FIG. 506

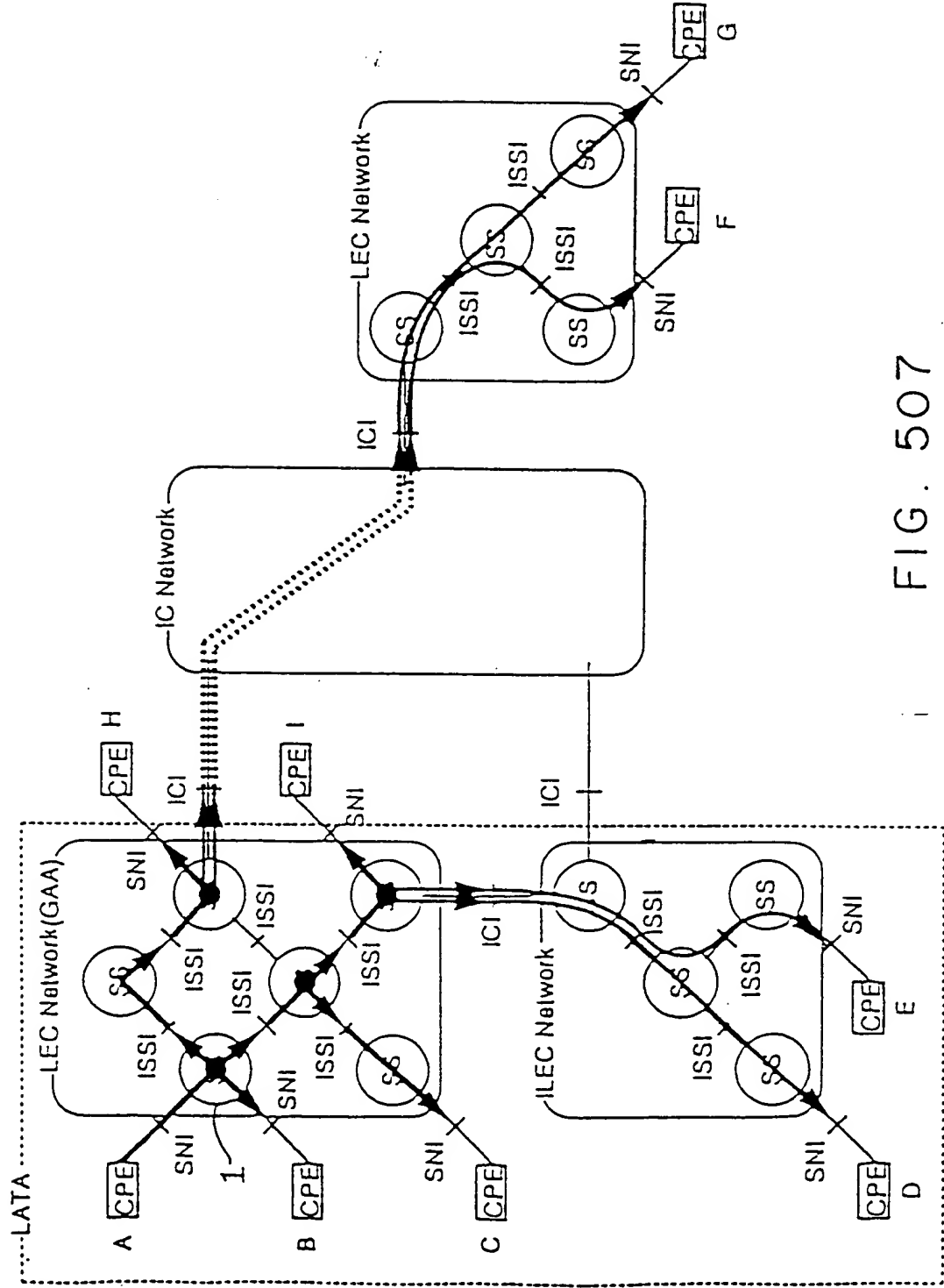


FIG. 507

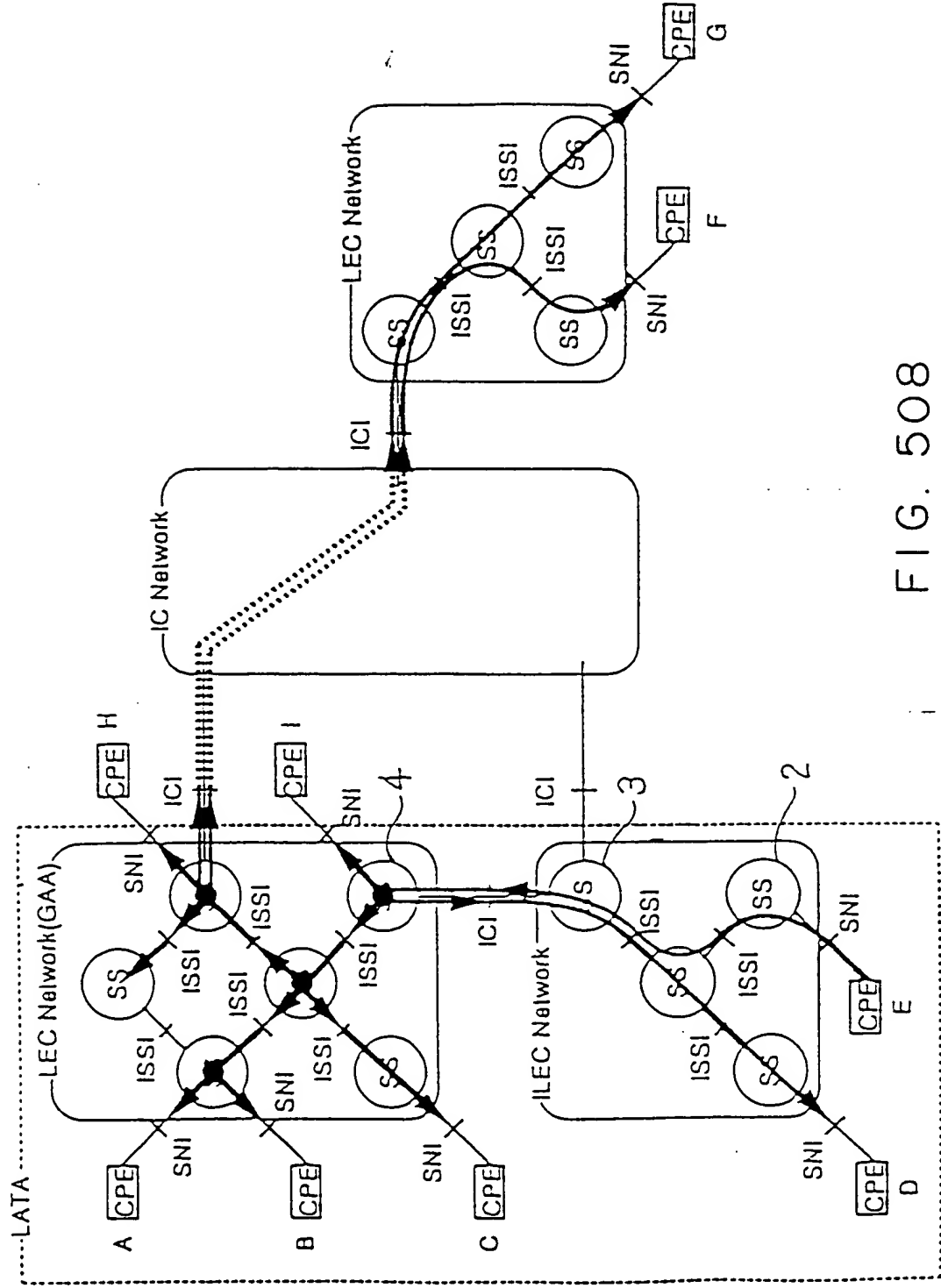
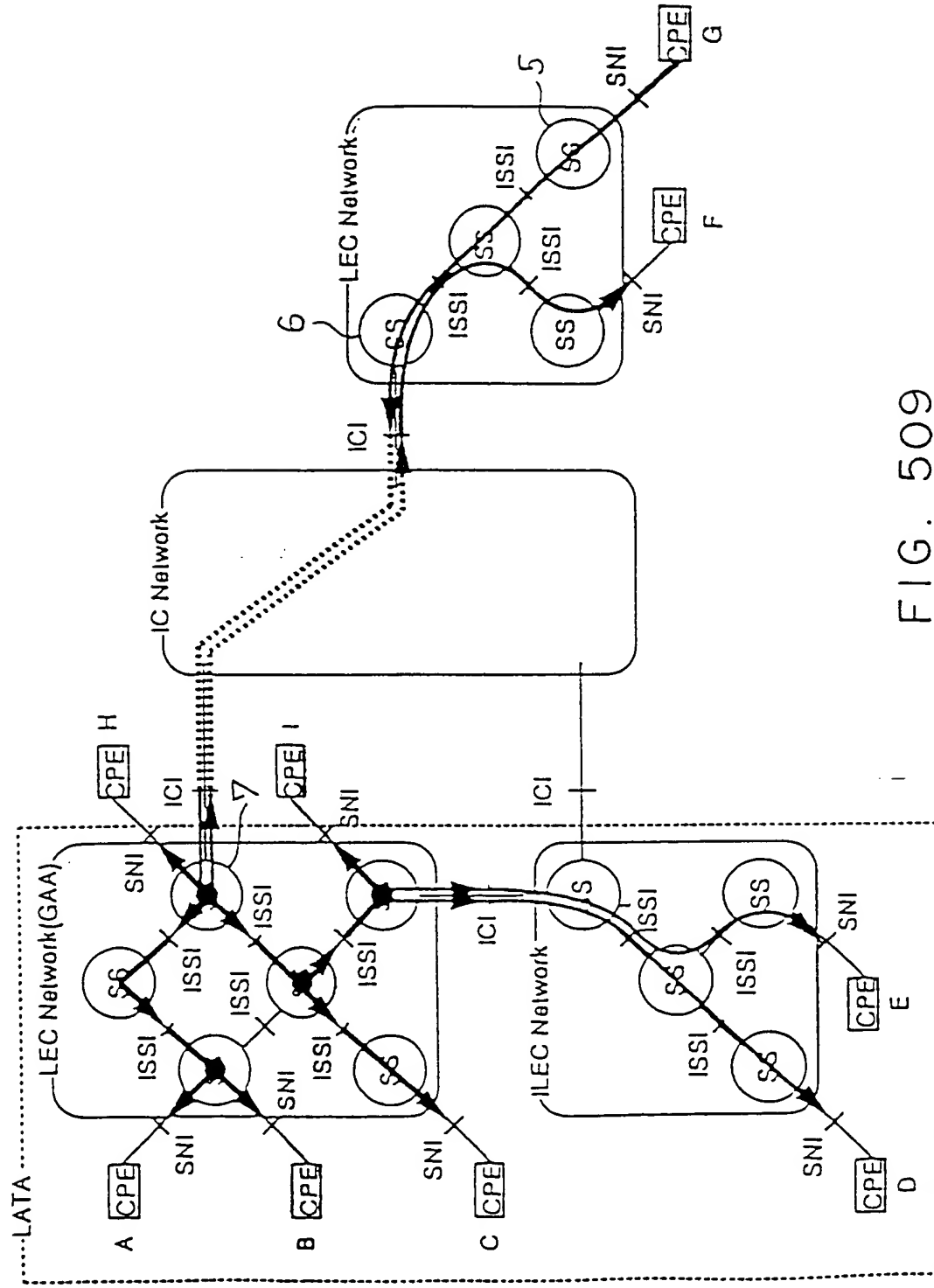


FIG. 508



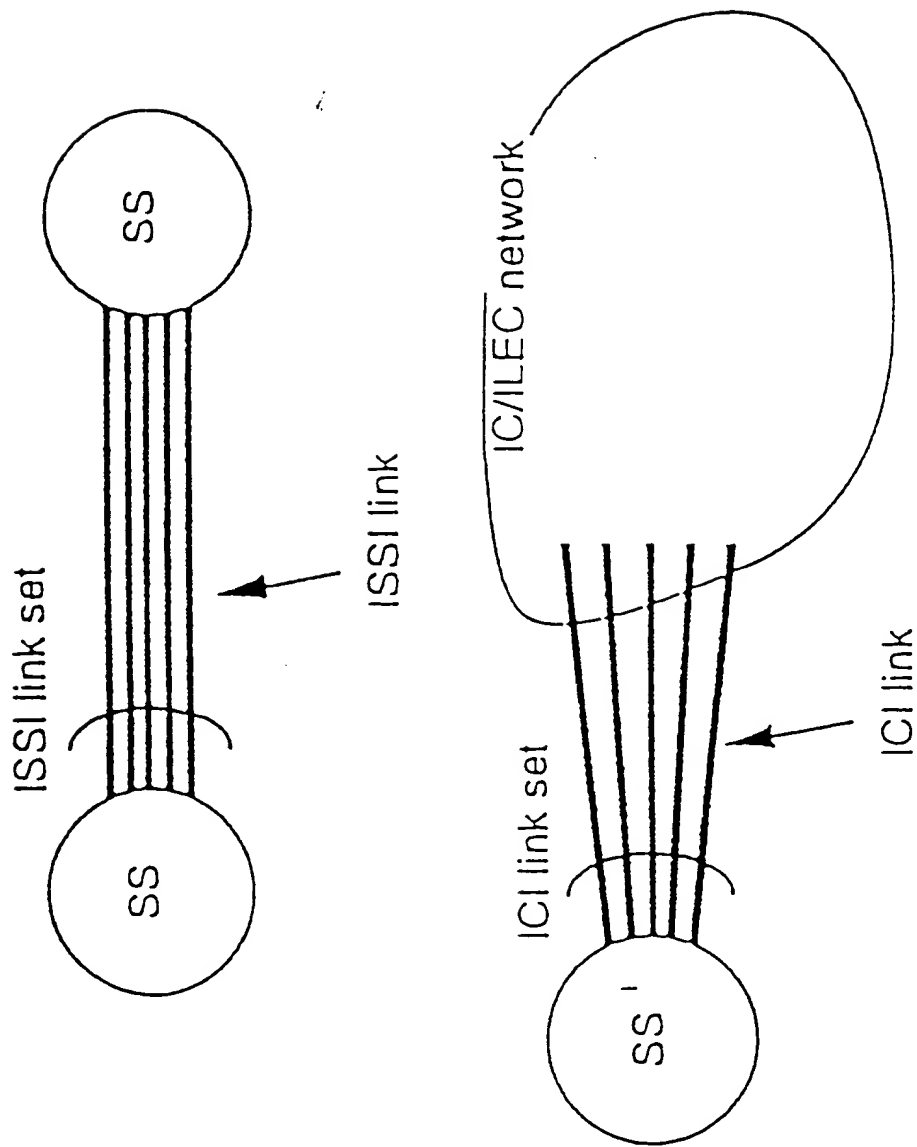


FIG. 510

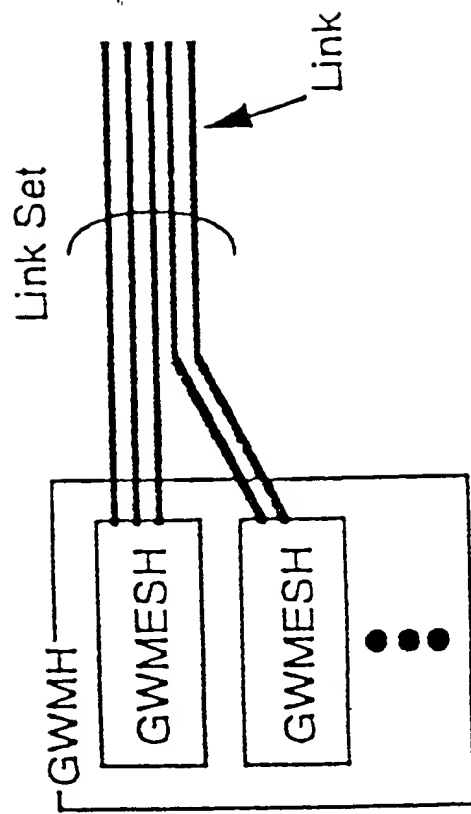


FIG. 511

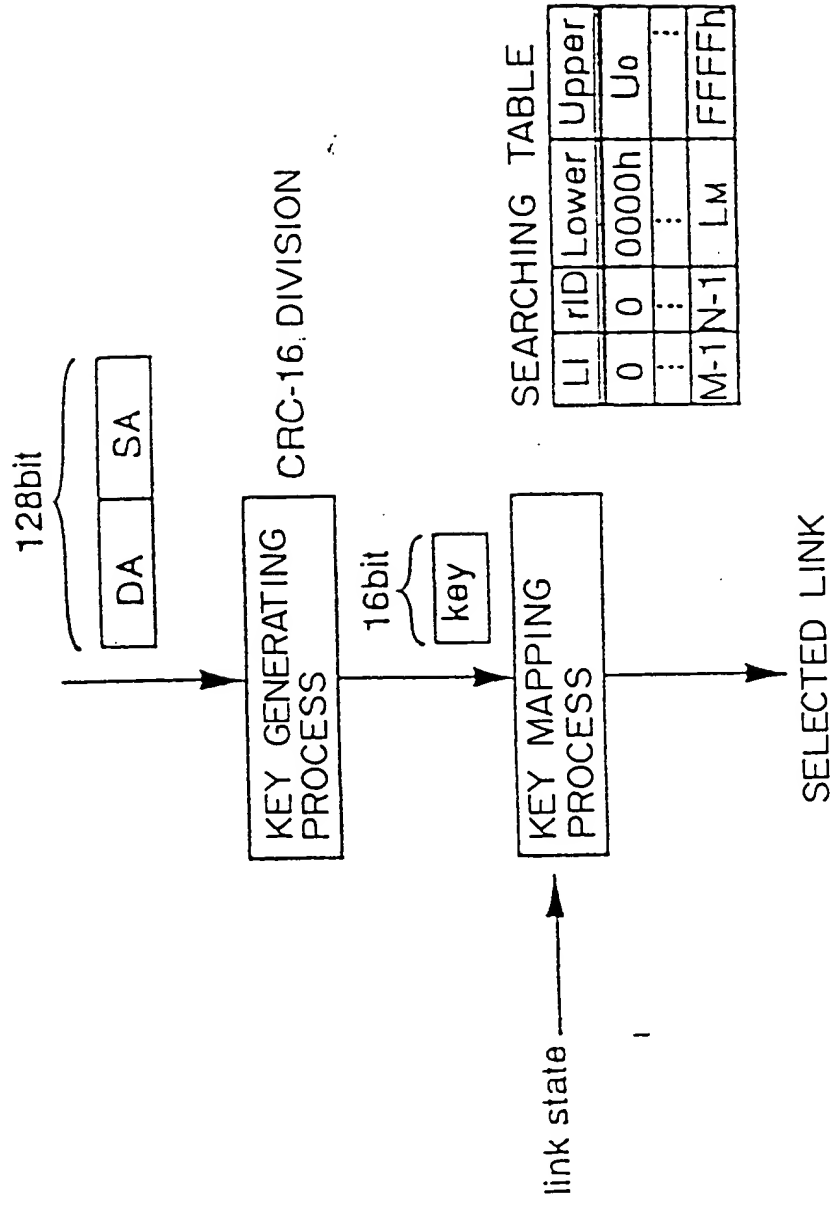


FIG. 512

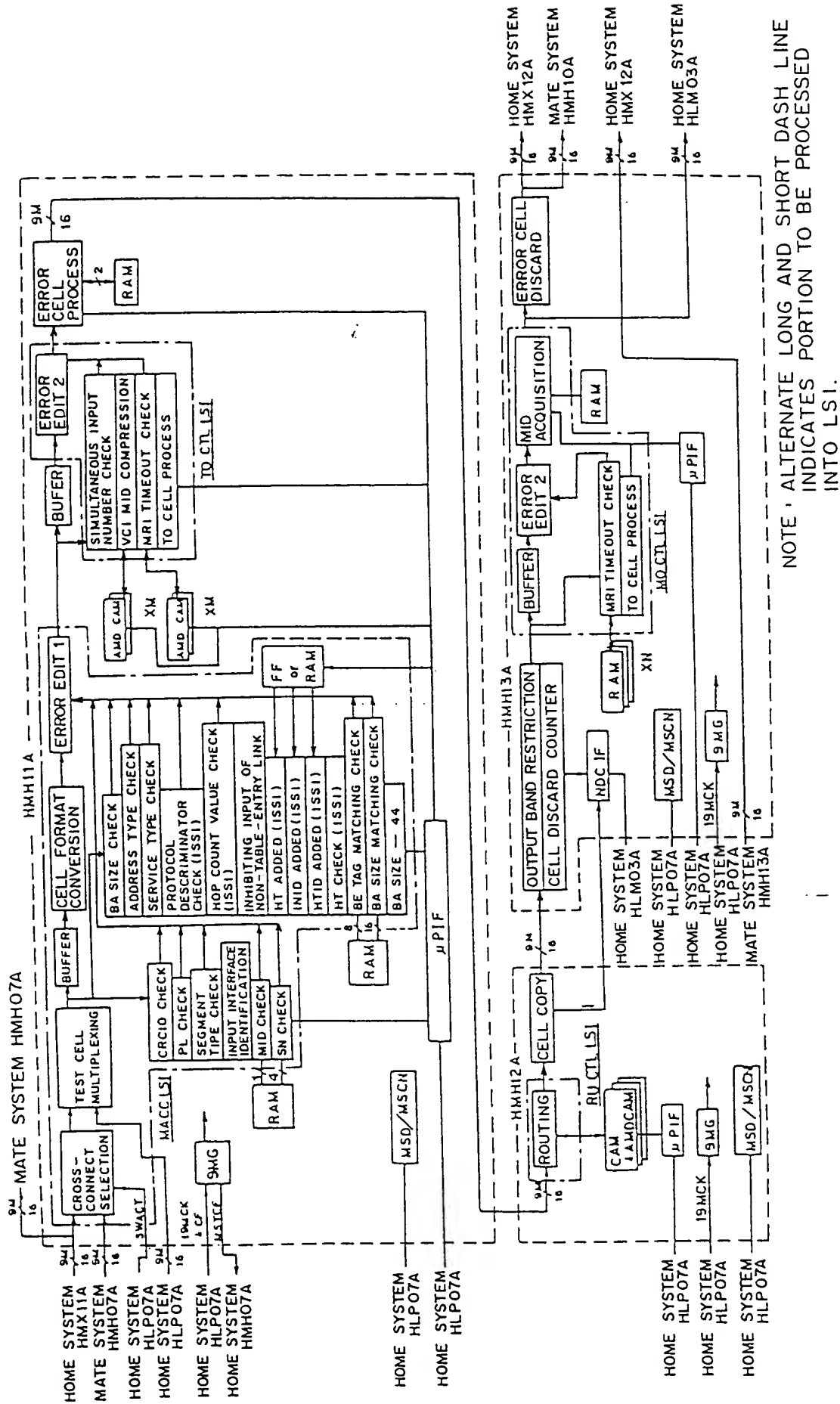


FIG. 513

ITEM	BLOCK NAME	CONTENTS
1	CROSS-CONNECT SELECTION	MOX ACT SYSTEM DATA IS SELECTED ACCORDING TO SYSTEM INFORMATION OF SWITCH. TCG CELL (TEST CELL) IS DROPPED.
2	INPUT INTERFACE IDENTIFICATION	INPUT INTERFACE IS IDENTIFIED AS ISSI OR ICI.
3	TEST CELL MULTIPLEXING	TEST CELL IS MULTIPLEXED WHEN LINE IS IN IDLE CELL STATE. TEST CELL IS TRANSMITTED DURING DIAGNOSIS.
4	CRC CHECK	CRC OPERATION IS PERFORMED ON CELL PAYLOAD AND CHECK IS MADE FOR ERROR.
5	PL CHECK	CHECK IS MADE THAT PAYLOAD LENGTH INDICATES PREDETERMINED VALUE.
6	SEGMENT TYPE CHECK	CHECK IS MADE WHETHER SEGMENT TYPE IS ROM, COM, EOM, OR SSM.
7	MIO CHECK	CHECK IS MADE THAT VCI/MIO IS NOT ACTIVE AT ROM AND VCI/MIO IS ACTIVE AT COM AND EOM.
8	SN CHECK	CHECK IS MADE THAT SN IS INITIALIZED AT ROM AND SN IS IN ORDER AT COM AND EOM.
9	BA SIZE CHECK	CHECK IS MADE THAT BASIZE INDICATES PREDETERMINED VALUE (40-9280).
10	AT CHECK	CHECK IS MADE THAT ADDRESS TYPE (IN OA AND SA FORMAT) INDICATES PREDETERMINED VALUE.
11	SERVICE TYPE CHECK	CHECK IS MADE THAT SERVICE TYPE INDICATES PREDETERMINED VALUE (NO ERROR FLAG IS SET).
12	PD CHECK	CHECK IS MADE THAT PROTOCOL DISCRIMINATOR INDICATES PREDETERMINED VALUE.
13	HOP COUNT CHECK	CHECK IS MADE THAT HOP COUNT FIELD VALUE DOES NOT INDICATE 0.
14	IT CHECK	CHECK IS MADE THAT INGRESS INTERFACE TYPE INDICATES PREDETERMINED VALUE.
15	BE TAG MATCHING CHECK	CHECK IS MADE THAT BE TAG OF L3 HEADER MATCHES BE TAG OF TAILER.
16	BA SIZE MATCHING CHECK	CHECK IS MADE THAT BE SIZE OF L3 HEADER MATCHES LENGTH OF TAILER.
17	ERROR EDIT I	ERROR CHECKED BY EACH CHECKER IS POSITIONED IN ERROR FLAG.
18	MRI TIMEOUT CHECK	MRI TIMEOUT IS DETERMINED IN IL3POU UNIT.
19	ERROR EDIT II	ERROR CHECKED BY EACH CHECKER IS POSITIONED IN ERROR FLAG.
20	TO CELL PROCESS	WHEN TIMEOUT IS REACHED IN MRI TIMEOUT CHECK, TIMEOUT CELL IS TRANSMITTED WHEN CELL IS INVALID.
21	CELL FORMAT CONVERSION	FORMAT OF ICIP/ISSIP IS CONVERTED INTO INTER-MH INTERFACE FORMAT (INCLUDING INPUT INF ICI/ISSI DISCRIMINATION INFORMATION).
22	ERROR CELL PROCESS	IF L3POU IS DETERMINED TO BE ERRONEOUS AS RESULT OF EACH CHECK, IT IS SUSPENDED.
23	ROUTING	OA AND CARRIER FIELD VALUE ARE IDENTIFIED AND MESSAGE ROUTING TABLE IS REFERRED TO IN ORDER TO SPECIFY MH (SBMH AND GMMH) CONTAINING DESTINATION SNI, ISSI, AND ICI.
24	CELL COPY	WHEN THERE ARE PLURAL DESTINATION MHS AS RESULT OF ROUTING, CELLS ARE COPIED WITH VCI ASSIGNED TO EACH MH.
25	CELL DISCARD COUNTER	CELL (L2 OR L3?) IS COUNTED IF IT IS DISCARDED BECAUSE OF INSUFFICIENT CAPACITY OF CELL COPY BUFFER.
26	OUTPUT BAND RESTRICTION	OUTPUT BAND (PEAK RATE) IS LIMITED FOR EACH OUTPUT MH.
27	CELL DISCARD	CELL IS DISCARDED WHEN OUTPUT BAND LIMIT IS EXCEEDED.
28	DISCARD COUNTER	NUMBER OF L2 AND L3 MESSAGES DISCARDED BY OUTPUT BAND LIMIT IS COUNTED.
29	MRI TIMEOUT CHECK	MRI TIMEOUT IS DETERMINED IN L3 POU UNITS.
30	ERROR EDIT	ERROR CHECKED BY MRI TIMEOUT IS POSITIONED IN ERROR FLAG.
31	TO CELL PROCESS	WHEN TIMEOUT IS REACHED IN MRI TIMEOUT CHECK, TIMEOUT CELL IS TRANSMITTED WHEN CELL IS INVALID.
32	MIO ACQUISITION	OUTPUT MIO IS ASSIGNED IN OUTPUT MH UNITS.
33	ERROR CELL DISCARD	IF CELL IS DETERMINED TO BE ERRONEOUS AS RESULT OF EACH CHECK, IT IS DISCARDED.
34	μP INTERFACE	LP COM IS INTERFACED WITH μP (SCHT).
35	MSD/MSCN INTERFACE	LP COM IS INTERFACED WITH MSD/MSCN.
36	NDC INTERFACE	LP COM IS INTERFACED WITH μP IN RELATION TO NETWORK DATA COLLECTION (NDC).

FIG. 514

	Message	Error Flag		E1 NIS	E1 RM	E2 NIT	E2 CC	E2 PL	E2 EN	E2 MC	E2 NIA	E2 SN	E2 BA	E2 DT	E2 ST	E2 PI	E2 PD	E2 HIC	E2 II	E2 EM	E2 DE	E2 LE	PVC
A	Invalid Payload CRC Code	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
B	Payload Length Error	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
C	Encapsulation Error (Segment Type = SSNI)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
D	BOM with Unexpected MID	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	COM with Unexpected MID	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	EOM with Unexpected MID	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
E	Unexpected SN Error	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
F	Invalid BAsize Field Value	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Invalid DA Type	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Invalid SA Type	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Invalid Protocol ID (ICIP) & Invalid Service Type (ISSIP)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Invalid Protocol Discriminator (ISSIP)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Hop Count = 0 (ISSIP)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	Invalid Ingress Interface Type (ISSIP)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
G	BEtag Mismatch	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M
	BAsize ≠ Length	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	M

'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG
'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK".
'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK' EF.
'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 515

	Message	Error Flag	E1 NS	E1 RM	E2 MT	E2 CC	E2 PL	E2 EN	E1 MC	E2 MA	E2 SN	E2 DA	E2 DT	E2 ST	E2 PI	E2 PD	E2 HC	E2 II	E2 EM	E2 BE	E2 LE	PVC
H	SIMULTANEOUS INPUT NUMBER CHECK 1		ON	OK															ON			M
	MRI Time Out 1		ON		ON																	M
	ROUTING		OK	OK																		
J	CELL COPY		OK	OK																		
	OUTPUT BAND LIMIT		OK	OK																		
	SIMULTANEOUS INPUT NUMBER CHECK 2		ON	OK															ON			
K	MRI Time Out 2		ON		ON																	
	MID ACQUISITION		OK	OK																		
	DISCARDING ERROR CELL		NG																			

'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG
 'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK".
 'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK'EF.
 'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 516

0000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	LID				IT		CLP	
03	1 (ST) 0		SN				MID									
04	0	0	0	0	0	0	0	0	BTag							
05	BAsize															
06	Address Type			0	0	0	1									
07	DA															
08																
09	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Address Type			0	0	0	1									
11	SA															
12																
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	Service Type						PL		Priority				CTB	HEL		
15	Protocol Version								Protocol Descriptor							
16	HE															
17																
18																
19																
20																
21																
22	(Incoming) Interface Type								Carrier							
23	Carrier								ES	HOP Count Indicator						
24	Incoming NW ID															
25	Incoming IC TFS ID															
26	Payload Length						Payload CRC									

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF: INTERFACE IDENTIFICATION (0=ISSI, 1=ICI)
 LID: INPUT LINK NUMBER (0-7)

FIG. 517

0000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	LID				PT		CLP	
03	1 (ST) 0		SN				MID									
04	0	0	0	0	0	0	0	0	BEtag							
05	DAsize															
06	Address Type			0	0	0	1									
07	DA															
08																
09	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Address Type			0	0	0	1									
11	SA															
12																
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	Protocol ID						PL		QoS				CTB	HEL		
15	Bridging															
16	HE															
17																
18																
19																
20																
21																
22	ICP Version								Carrier							
23	Carrier								ES	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	Payload Length						Payload CRC									

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
 LID:INPUT LINK NUMBER(0-7)

FIG. 518

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGU		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	LID				PT		CLP	
03	0 (ST) 1		SN				MID									
04	0	0	0	0	0	0	0	0	BEtag(SIP)							
05	BAsize(SIP)															
06	Address Type				0	0	0	1								
07	DA(SIP)															
08																
09	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Address Type				0	0	0	1								
11	SA(SIP)															
12																
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	HLPI						PL		QOS				CB	HEL		
15	Bridging															
16	HE															
17																
18																
19																
20																
21																
22	Information															
23																
24	0	0	0	0	0	0	0	0	BEtag							
25	Length															
26	Payload Length								Payload CRC							

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF:INTERFACE IDENTIFICATION(0=ISSI, 1=ICT)
 LID:INPUT LINK NUMBER(0-7)

FIG. 519


00000000000000000000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	LID			PT			CLP	
03	0 (ST) 0		SN				MID									
04	0	0	0	0	0	0	0	0	BEtag(SIP)							
05	BAsize(SIP)															
06	Address Type			0	0	0	1									
07	DA(SIP)															
08																
09	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Address Type			0	0	0	1									
11	SA(SIP)															
12																
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	HLPI						PL		QOS				CIB		HEL	
15	Bridging															
16	HE															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	Payload Length						Payload CRC									

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF:INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
 LID:INPUT LINK NUMBER(0-7)

FIG. 520

0000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0			LID			PT		CLP	
03	0 (ST) 0		SN				MID									
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
23																
24																
25																
26	Payload Length							Payload CRC								

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF: INTERFACE IDENTIFICATION(0=ISSI, 1=ICI)
 LID: INPUT LINK NUMBER (0-7)

FIG. 521

0000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	0	OAM	0	TAGA			0	0	0	TAGC			TAGB		0	0
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	LID				PT			CLP	
03	0 (ST) 1		SN				MID									
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18	0	0	0	0	0	0	0	0	BDR							
19	Length															
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	Payload Length							Payload CRC								

TCG CELL OF OAM=1 IS DISCARDED IN ICLP INPUT UNIT.
 IF: INTERFACE IDENTIFICATION(0=ISSI, I=ICI)
 LID: INPUT LINK NUMBER (0-7)

FIG. 522

00000000000000000000000000000000

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	dc															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	RVC								PT		CLP	
03	0 (ST) 0		SN			SOURCE SHELF ID			MID							
04	0	0	0	0	0	0	0	0	BEtag(SIP)							
05	BAsize(SIP)															
06	Address Type			0	0	0	1									
07	DA(SIP)															
08																
09	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
10	Address Type			0	0	0	1									
11	SA(SIP)															
12																
13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
14	HLPI						PL		QOS				CB	HEL		
15	Bridging															
16	HE															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	Payload Length								dc							

RVCI: DESTINATION MHID=SBMH (00-1Fh) AND GWMH (40-5Fh) FOR USER CELL
RVCI=FFh FOR MESH-MH TEST CELL
SOURCE SHELF ID: 0-3
IF: INTERFACE IDENTIFICATION(0=ISSI, 1=ICD)

FIG. 526

	015	014	013	012	011	010	009	008	007	006	005	004	003	002	001	000
00																
01																
02	TEST					INPUT VCI										
03					INPUT MID											
04	SEGMENT TYPE															
05																
06	DA															
07																
08																
09																
10																
11																
12																
13																
14	SERVICE TYPE															
15																
16																
17																
18																
19																
20																
21																
22																
23	CARRIER															
24																
25																
26																

EF1
 US
 CC

EF2

DATA RECOGNIZED
IN THIS BLOCK

FIG. 529

(COM)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 INT																INT	INT		
0	ST	CP	BC1	BC0		INPUT MID												T	T
1	INPUT VCI (AT MSB)			0	0	1	1	1	1	1	1	1	INPUT VCI (AT LSB)				MS		
2	PL L (MSB-LSB)			TEST	OUTPUT VCI								PT	CLP		RM	MT		
3	ST	SX			OUTPUT MID														C
4																			PL
5																			MC
6																			SX
7																			LA
8																			
9																			
10																			
11																			
12																			
13																			
14																			
15																			
16																			
17																			
18																			
19																			
20																			BO
21																			
22																			
23																			
24																			EX
25																			
26	PL L				PT														L

FIG. 536

(BOM)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ST	RF1	RF2															
0	ST		CP	BC1	BC2	INPUT MID												T	X															
1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	MS															
2	0	0	1	1	TEST	OUTPUT VCI							PT	CLP	RM	MT																		
3	ST		SH			OUTPUT MID													C															
4	0	0	0	0	0	0	0	0	0	RZ											PL													
5	RAC																			MA														
6	DA																			SH														
7																				BA														
8																				DT														
9																				ST														
10	SA																			PI														
11																				IS														
12																																		
13																				PO														
14	Service Type																			EC														
15																				A														
16																																		
17																																		
18																																		
19																																		
20																				ME														
21																				EM														
22																				RE														
23	Carrier																			EN														
24																																		
25																																		
26																			PL Len				IP											T

FIG. 539

669260-022260

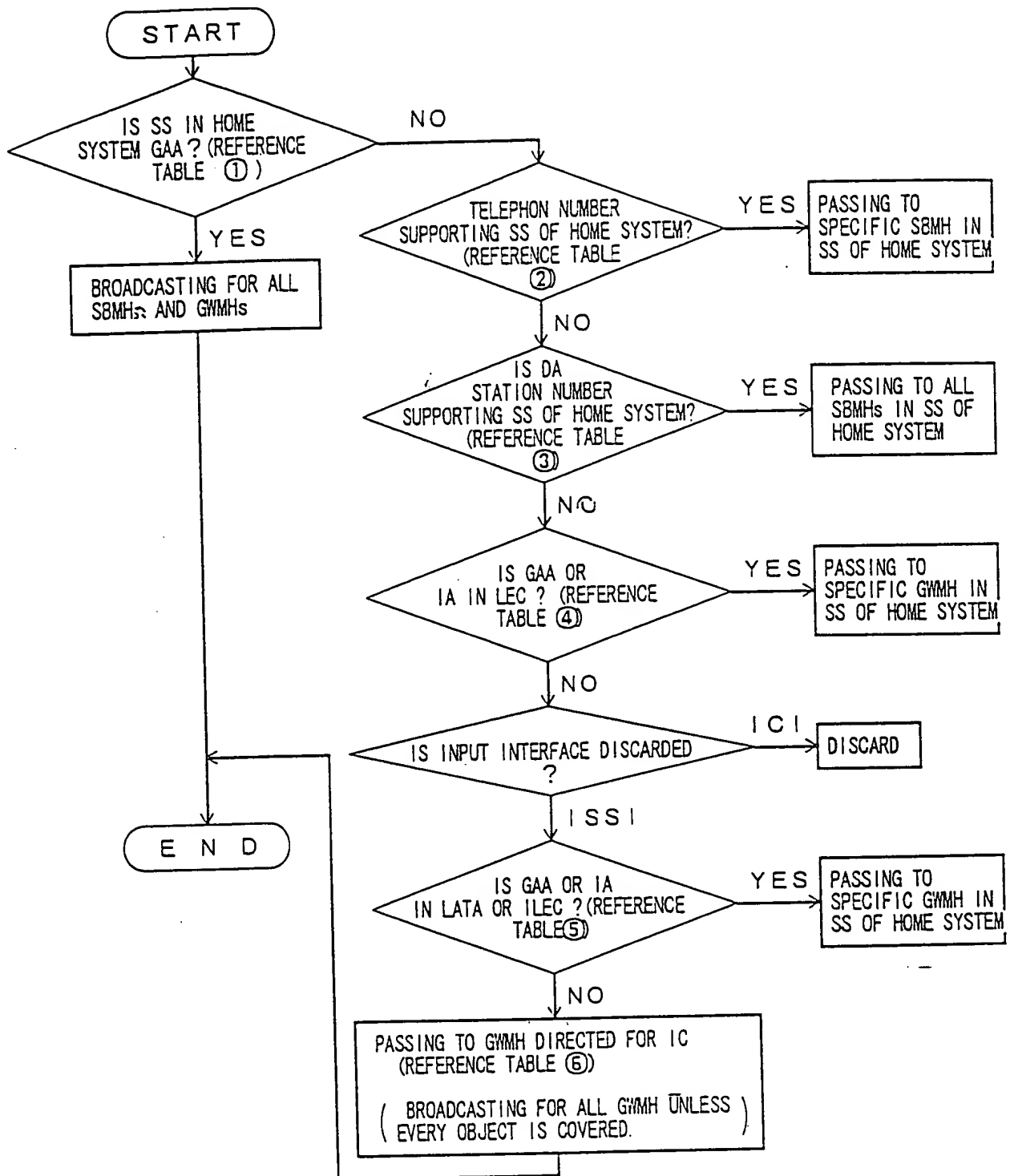


FIG. 544

- ① DETERMINING WHETHER OR NOT SS IN HOME SYSTEM IS GAA ACCORDING TO GAA LIST.

	GAA LIST (64 bit)
1024 (M)

- ② DETERMINING WHETHER OR NOT THERE IS SBMH FOR SUPPORTING SNI OF HOME SYSTEM ACCORDING TO DA (TELEPHONE NUMBER).

	DA (64 bit)	SBMH No (5 bit)
2048 (M)

- ③ DETERMINING WHETHER OR NOT STATION NUMBER REFERS TO SS IN HOME SYSTEM ACCORDING TO STATION NUMBER OF DA.

	STATION NUMBER (32 bit)
64 (M)

- ④ AT GA : DETERMINING WHETHER OR NOT THERE IS SS IN LEC OF HOME SYSTEM FOR SUPPORTING GAA ACCORDING TO (STATION NUMBER) OF DA.

	GAA STATION NUMBER IN LEC (32 bit)	GMMH No (5 bit)
1024 (M)

- AT IA : DETERMINING WHETHER OR NOT THERE IS SS IN LEC OF HOME SYSTEM FOR SUPPORTING IA ACCORDING TO (STATION NUMBER) OF DA.

	IA STATION NUMBER IN LEC (32 bit)	GMMH No (5 bit)
1024 (M)

- ⑤ AT GA : DETERMINING WHETHER OR NOT THERE IS SS IN LATA FOR SUPPORTING GAA ACCORDING TO (STATION NUMBER) OF DA.

	ILEC GAA STATION NUMBER (32 bit)	GMMH No (5 bit)
1024 (M)

- AT IA : DETERMINING WHETHER OR NOT THERE IS SS IN LATA FOR SUPPORTING IA ACCORDING TO (STATION NUMBER) OF DA.

	ILEC IA STATION NUMBER (32 bit)	GMMH No (5 bit)
1024 (M)

- ⑥ DETERMINING GMMH No. FOR SUPPORTING ICI TO IC ACCORDING TO SMDS CIC.

	SMDS CIC (16 bit)	GMMH No (5 bit)
256 (M)

TOTAL STATION NUMBER
OF TABLES ③-⑤ IS
512.

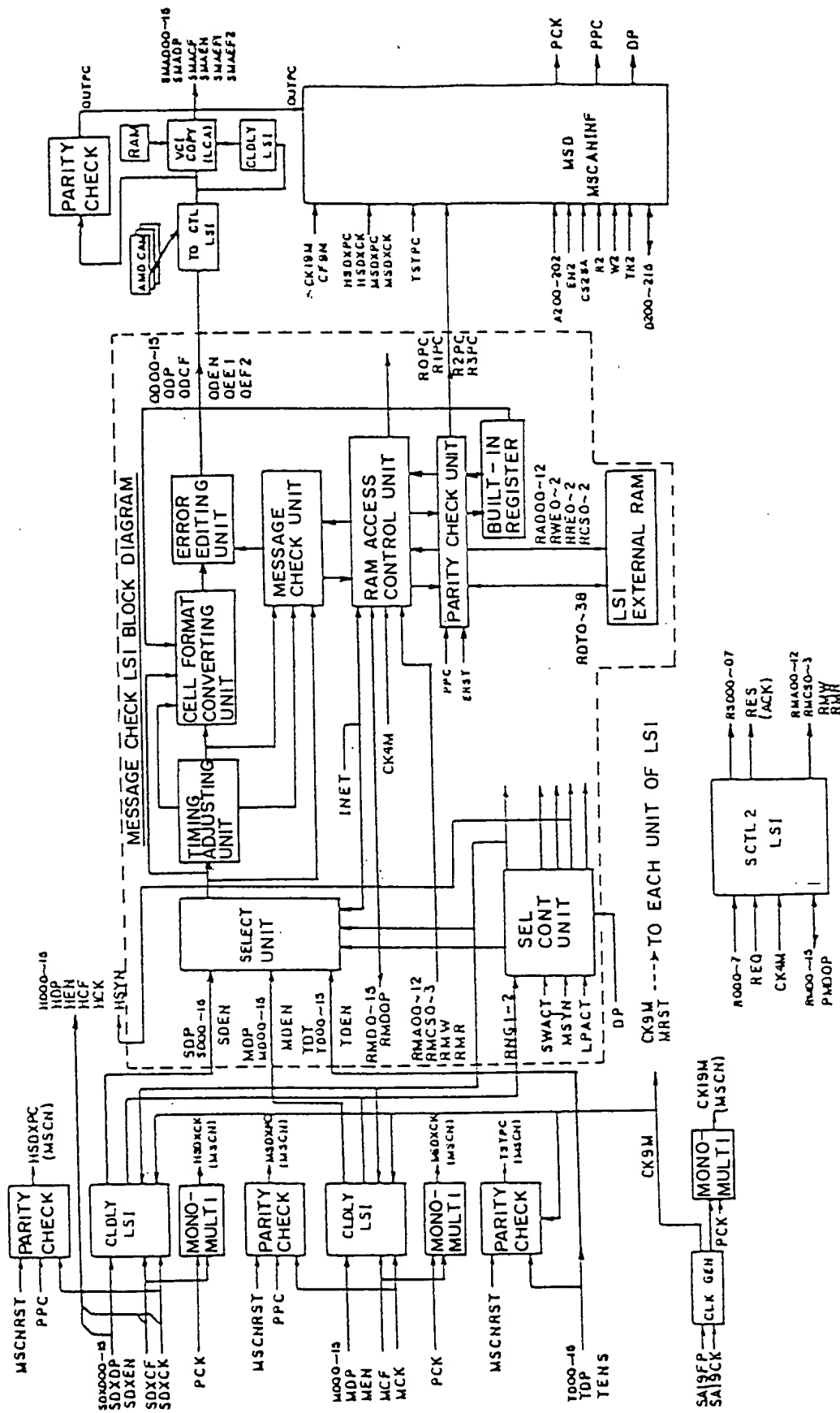


FIG. 546

NAME	POLARITY	LEVEL	POSITION	EXPLANATION OF FUNCTION	REMARKS
SDXD00~15	P	TTL	BWB	HIGHWAY DATA OF SDMX → ICLP. MSB FOR SDXD15, AND LSB FOR SDXD00	
SDXDP	P	TTL	BWB	ODD PARITY FOR SDXDxx AND SDXEN	
SDXEN	N	TTL	BWB	ENABLE OF SDMX → ICLP	
SDXCF	N	TTL	BWB	CELL FRAME OF SDMX → ICLP	
SDXCK	CLK	TTL	BWB	9MHZ CLK IN PARALLEL TO HIGHWAY DATA OF SDMX → ICLP	
MD00~15	P	TTL	FCN	HIGHWAY DATA OF MATE ICLP. MSB FOR MD15, AND LSB FOR MD00	
MDP	P	TTL	FCN	ODD PARITY FOR MDxx AND MEN	
MEN	N	TTL	FCN	ENABLE OF MATE ICLP	
MCF	N	TTL	FCN	CELL FRAME OF MATE ICLP	
MCK	CLK	TTL	FCN	9MHZ CLK IN PARALLEL TO HIGHWAY DATA OF MATE ICLP	
TD00~15	P	TTL	BWB	TEST DATA OF HLP07 → ICLP. MSB FOR TD15, AND LSB FOR TD00	
TDP	P	TTL	BWB	ODD PARITY FOR TDxx AND TENS	
TENS	N	TTL	BWB	TEST CELL ENABLE	
TS00	N	TTL	BWB	ICLP CELL FRAME	
TS01	N	TTL	BWB	TEST CELL SEND OK/NG	
SMAD00~15	P	TTL	BWB	HIGHWAY DATA OF HMH11A → HMH09A. MSB FOR SMAD15, AND LSB FOR SMAD00	
SMADP	P	TTL	BWB	ODD PARITY FOR SMADxx AND SMAEN	
SMAEN	N	TTL	BWB	ENABLE OF HMH11A → HMH09A	
SMACF	N	TTL	BWB	CELL FRAME OF HMH11A → HMH09A	
SMAEF1	N	TTL	BWB	ERROR FLAG OF HMH11A → HMH09A (PROTECTION AGAINST STACK FOR 0, 26WORD) NG:L, GOOD:H	
SMAEF2	N	TTL	BWB	ERROR FLAG OF HMH11A → HMH09A (PROTECTION AGAINST STACK FOR 0, 26WORD) NG:L, GOOD:H	
SWACTA	—	TTL	BWB	INDICATES ACTIVE SW UNIT (HOME SW ACT(L)/MATE SW ACT(H))	
LPACTA	—	TTL	BWB	INDICATES ACTIVE LP UNIT (HOME LP ACT(L)/MATE LP ACT(H))	
MSTCF	N	TTL	BWB	SYNCHRONIZATION FRAME PULSE FROM ICLP TO OGLP	
SA19CK	CLK	TTL	BWB	HLP02A → ALL LP UNITS 19MHz CLK	
SA19FP	N	TTL	BWB	HLP02A → ALL LP UNITS 19MHz FRAME PULSE	
ROD00 ~07	P	TTL	BWB	HLP07A → ALL LP UNIT 8BIT COMMAND BUS. MSB FOR ROD07, AND LSB FOR ROD00	
REQ	N	TTL	BWB	HLP07A → ALL LP UNITS REQUEST ENABLE	
CK4M	CLK	TTL	BWB	HLP07A → ALL LP UNITS 4MHz CLK	
RSDD00~07	P	TTL	BWB	HLP07A → ALL LP UNIT 8BIT COMMAND BUS. MSB FOR RSD07, AND LSB FOR RSD00	
RES	N	TTL	BWB	HLP07A → ALL LP UNITS RESPONSE ENABLE	

FIG. 547

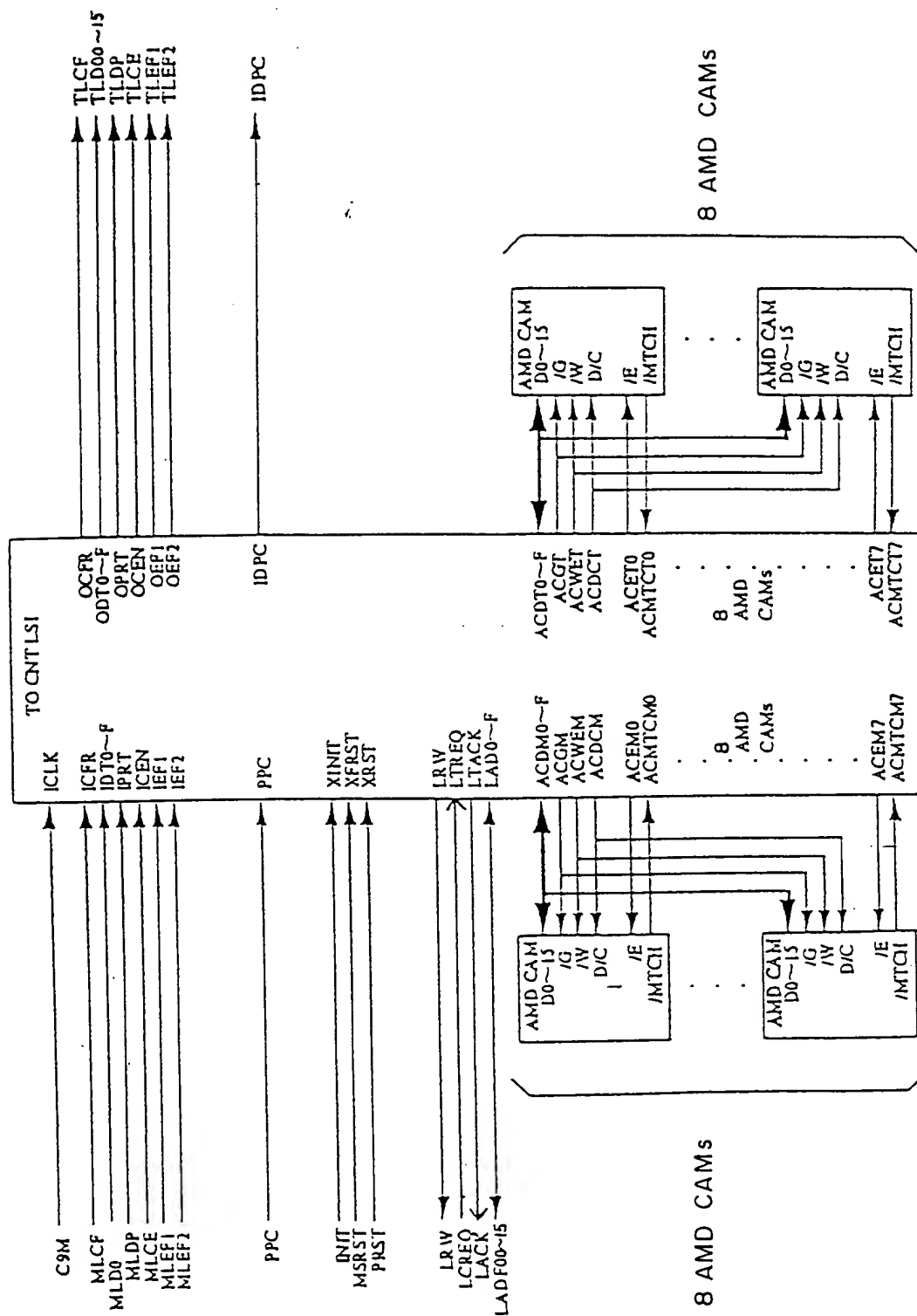


FIG. 548

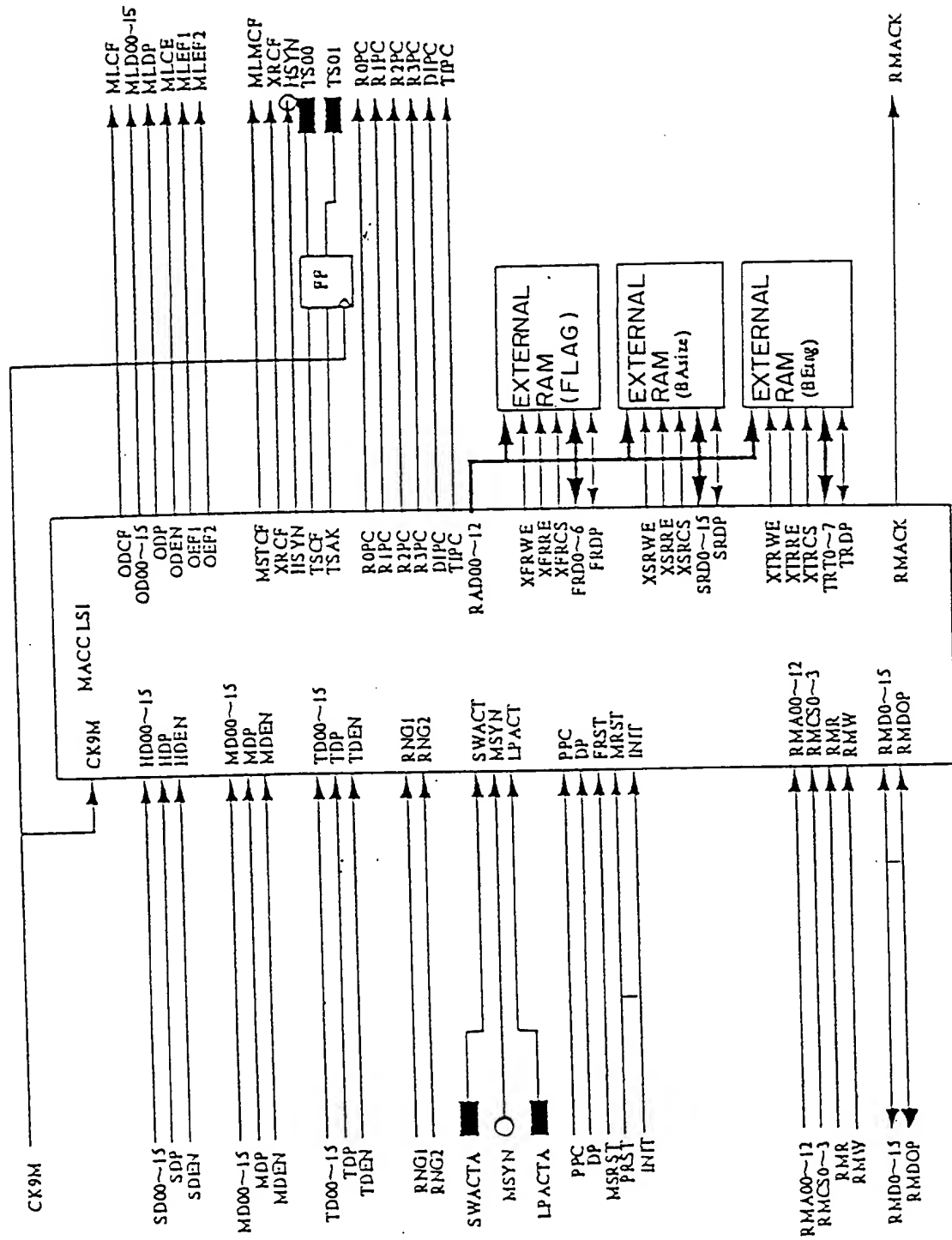


FIG. 549

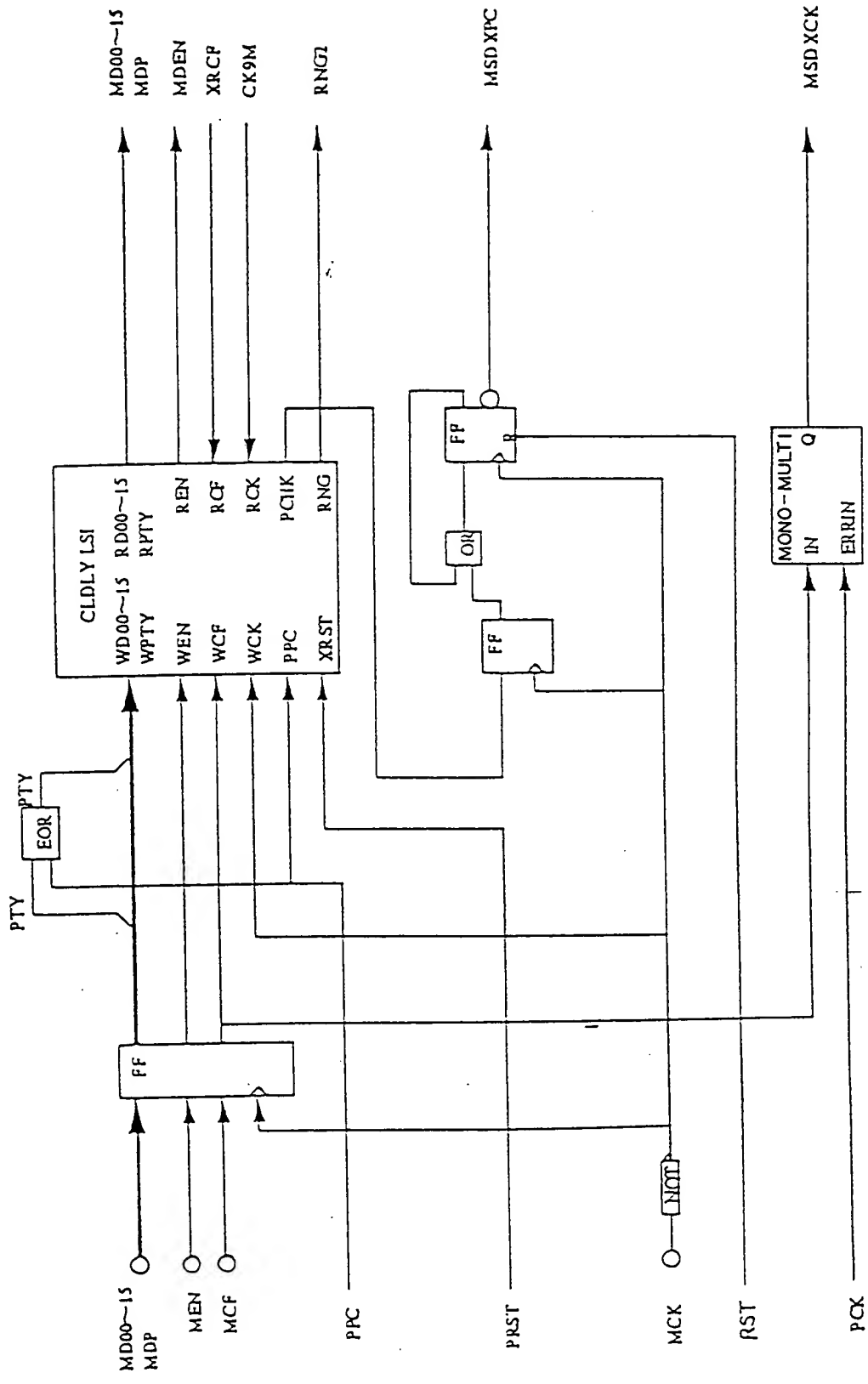


FIG. 550

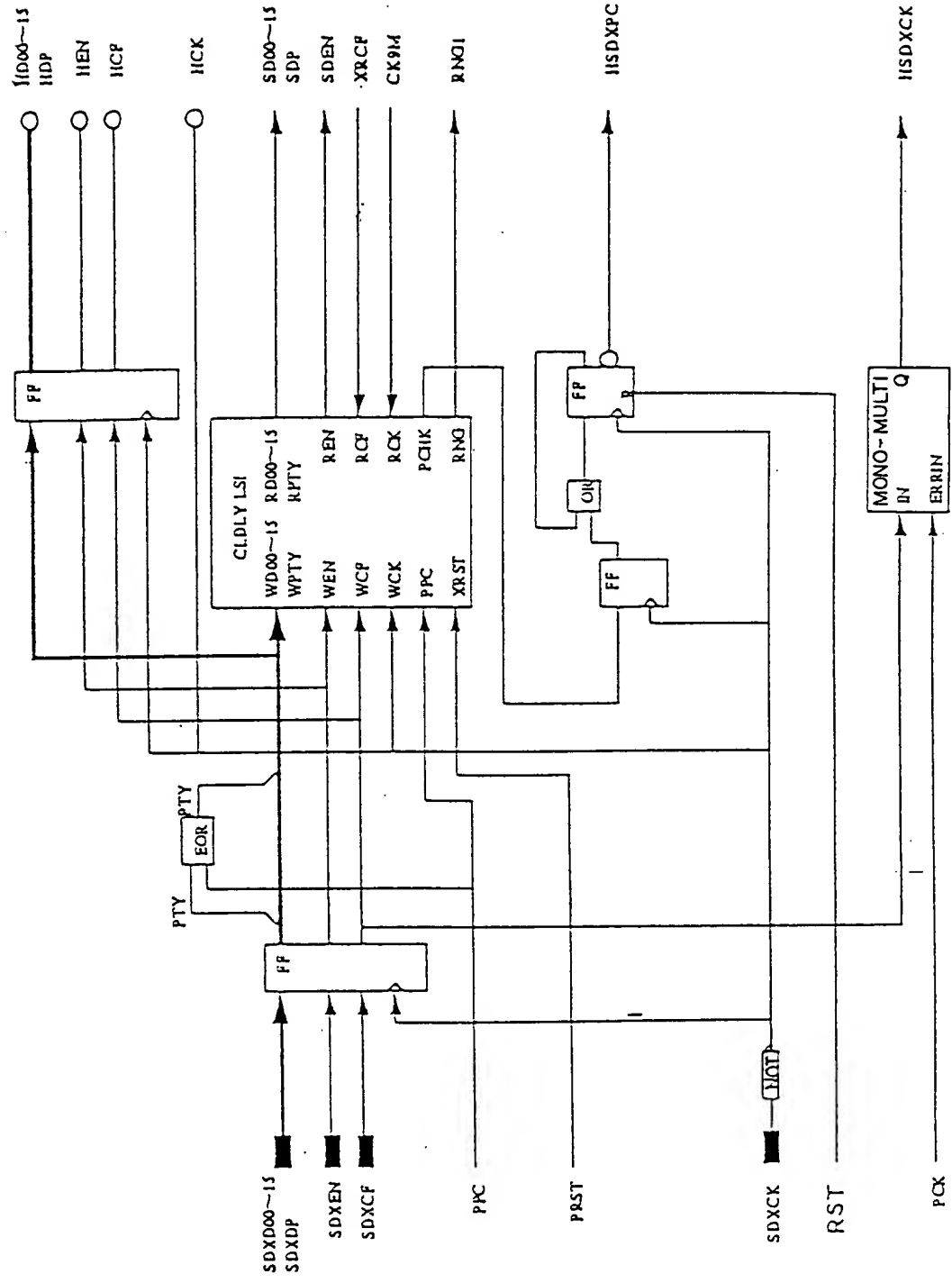


FIG. 551

FIG. 552

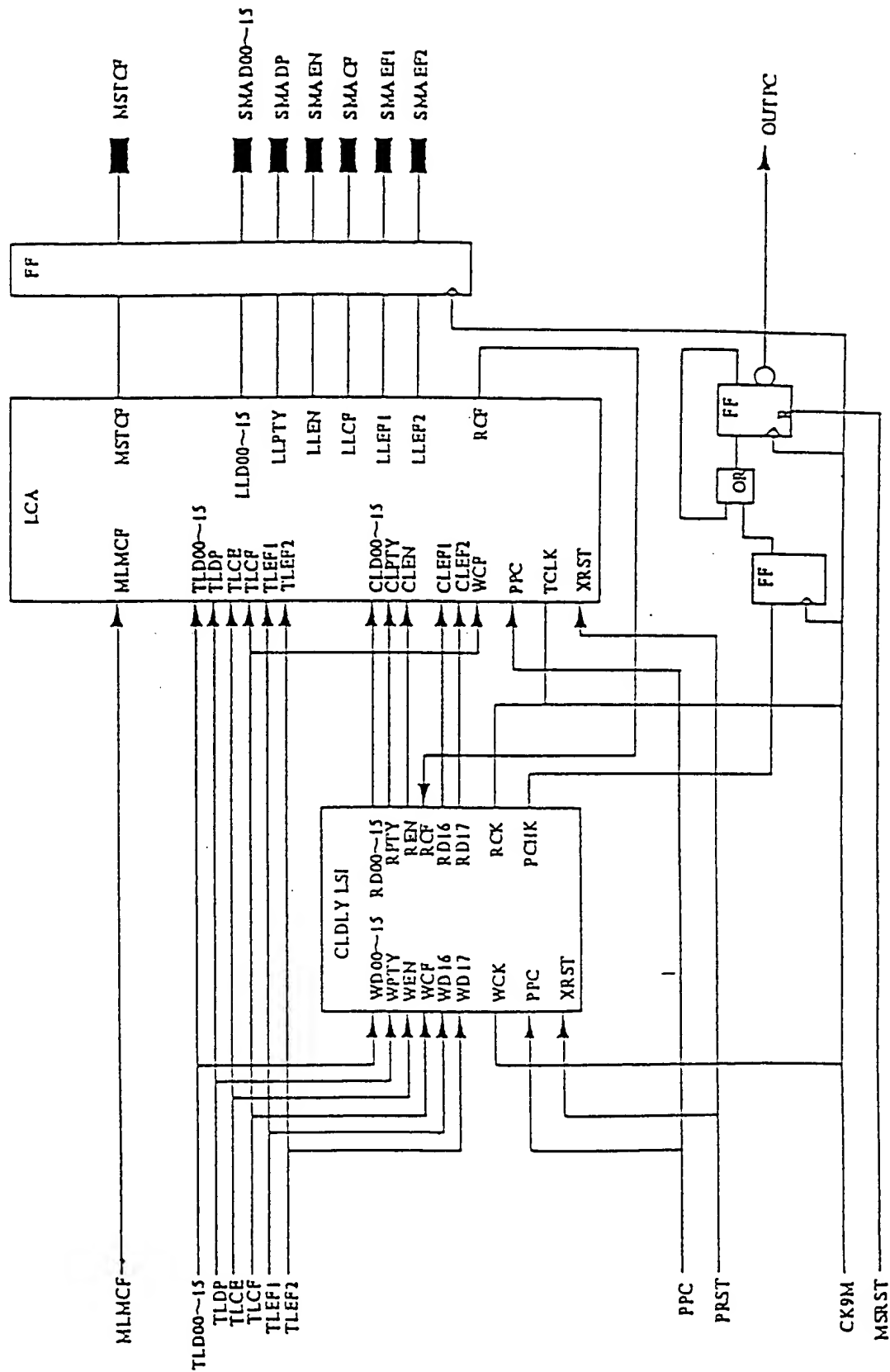
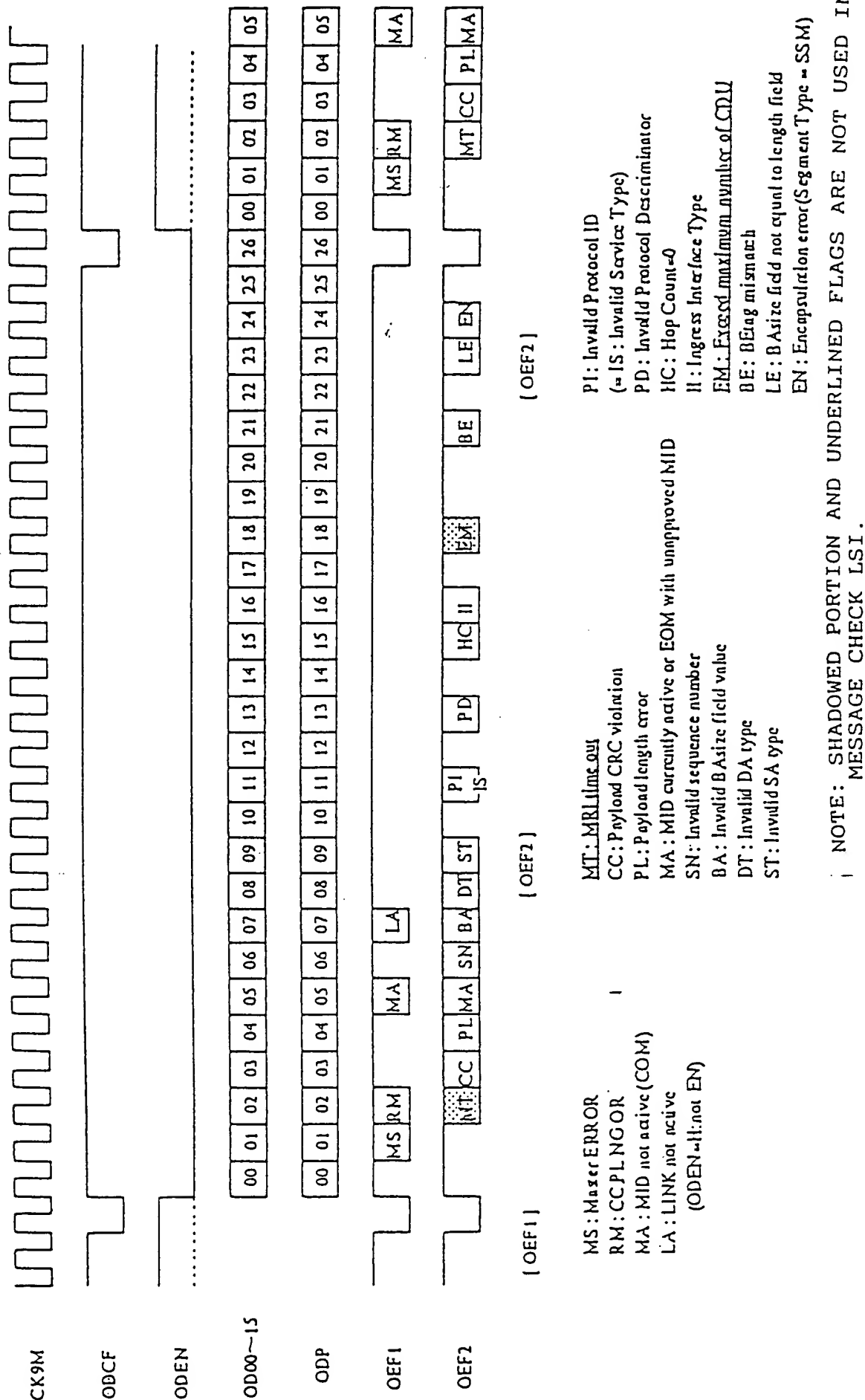


FIG. 553



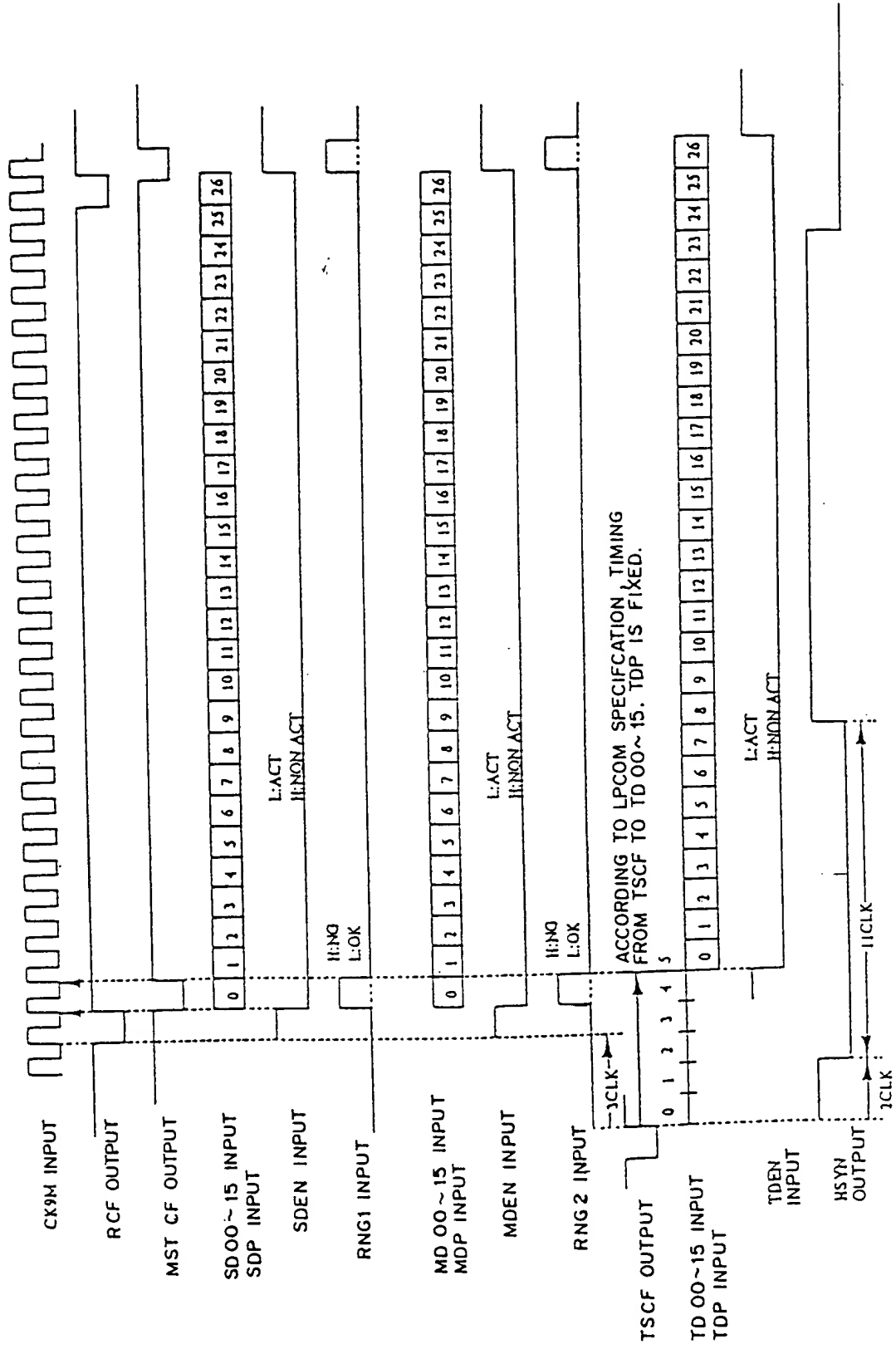


FIG. 555

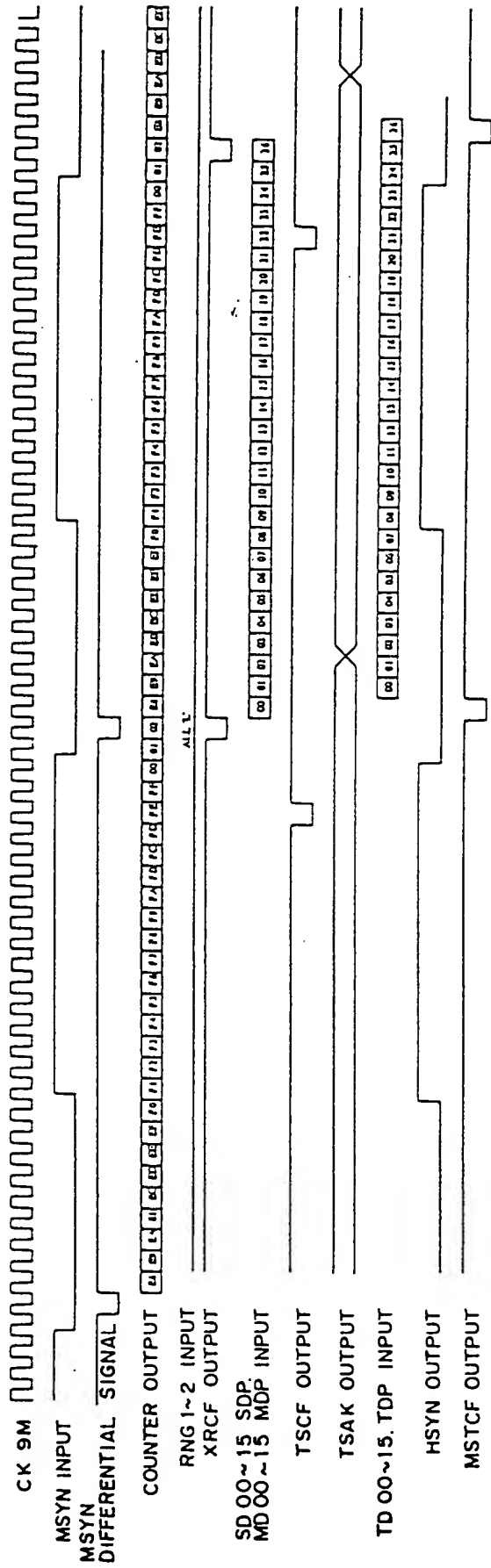


FIG. 556

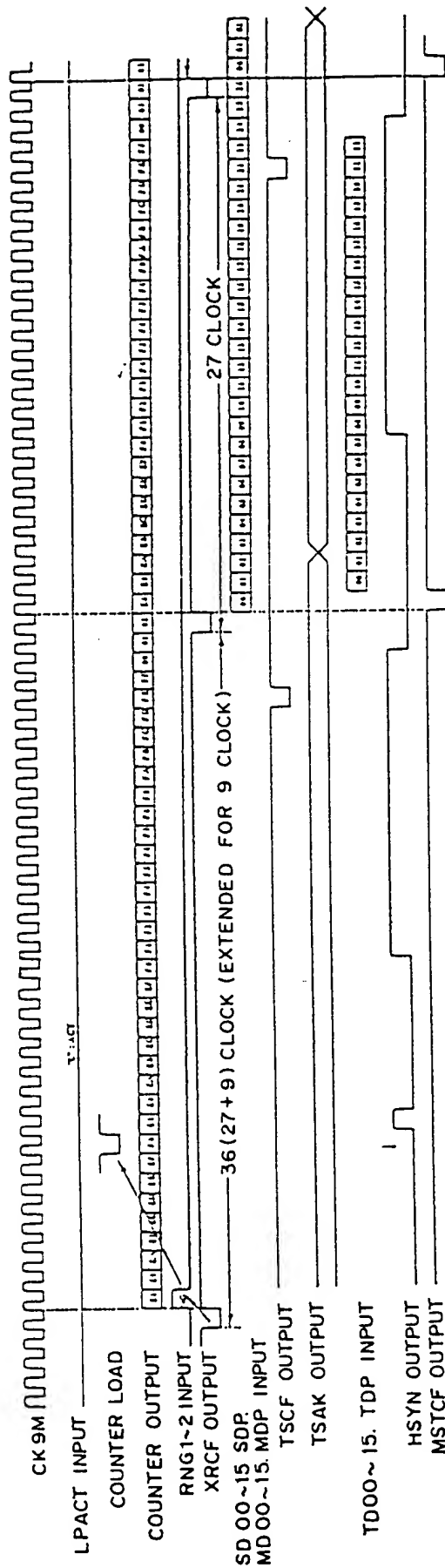
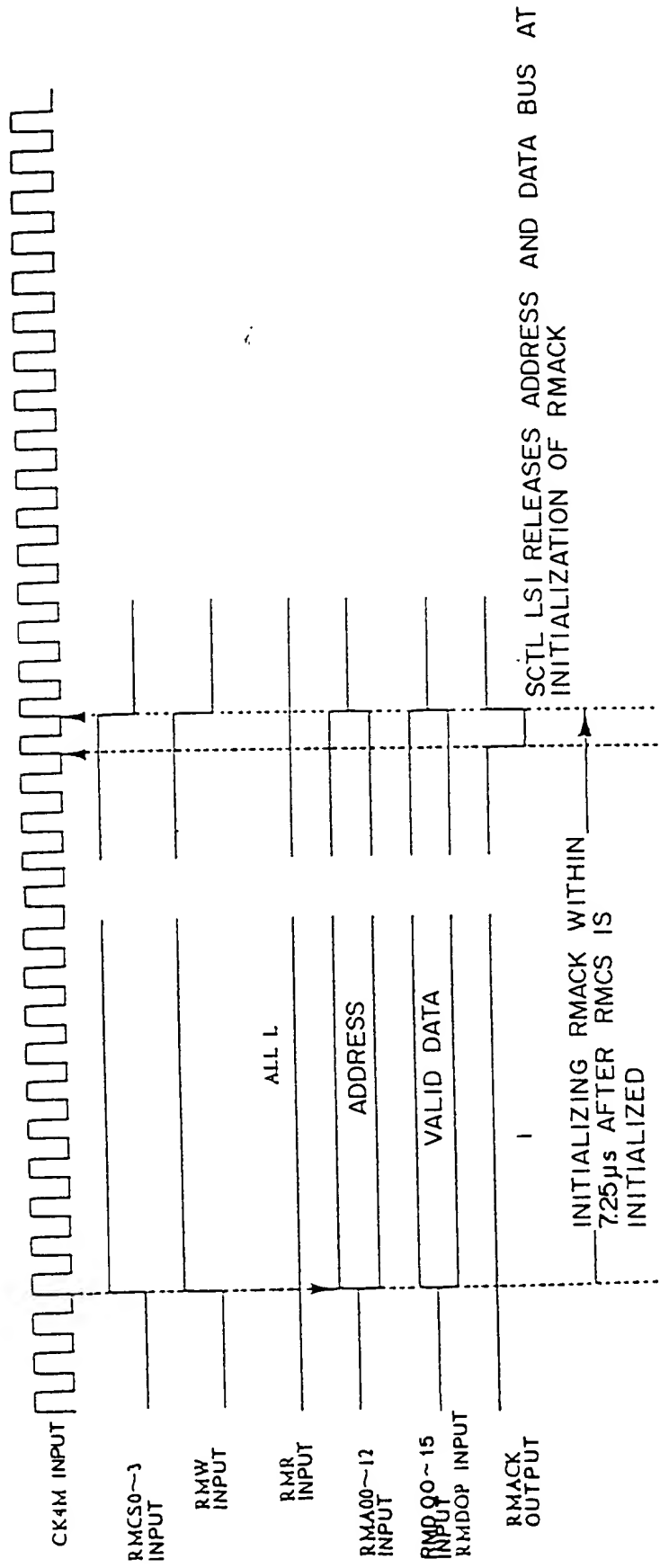


FIG. 557



KEEP SUFFICIENT MARGIN FOR STORING SCTL DATA
(STORING TIMING CAN BE OPTIONALLY SET).

FIG. 558

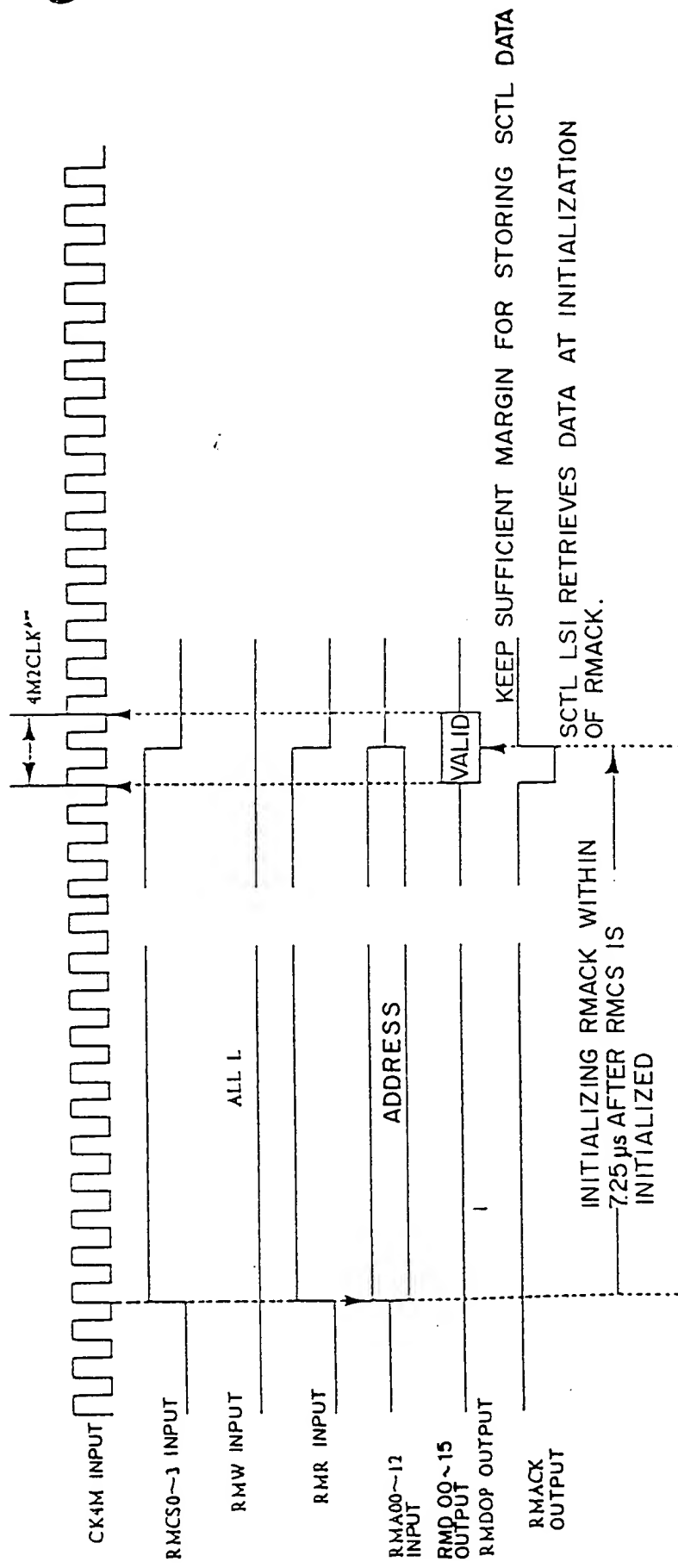


FIG. 559

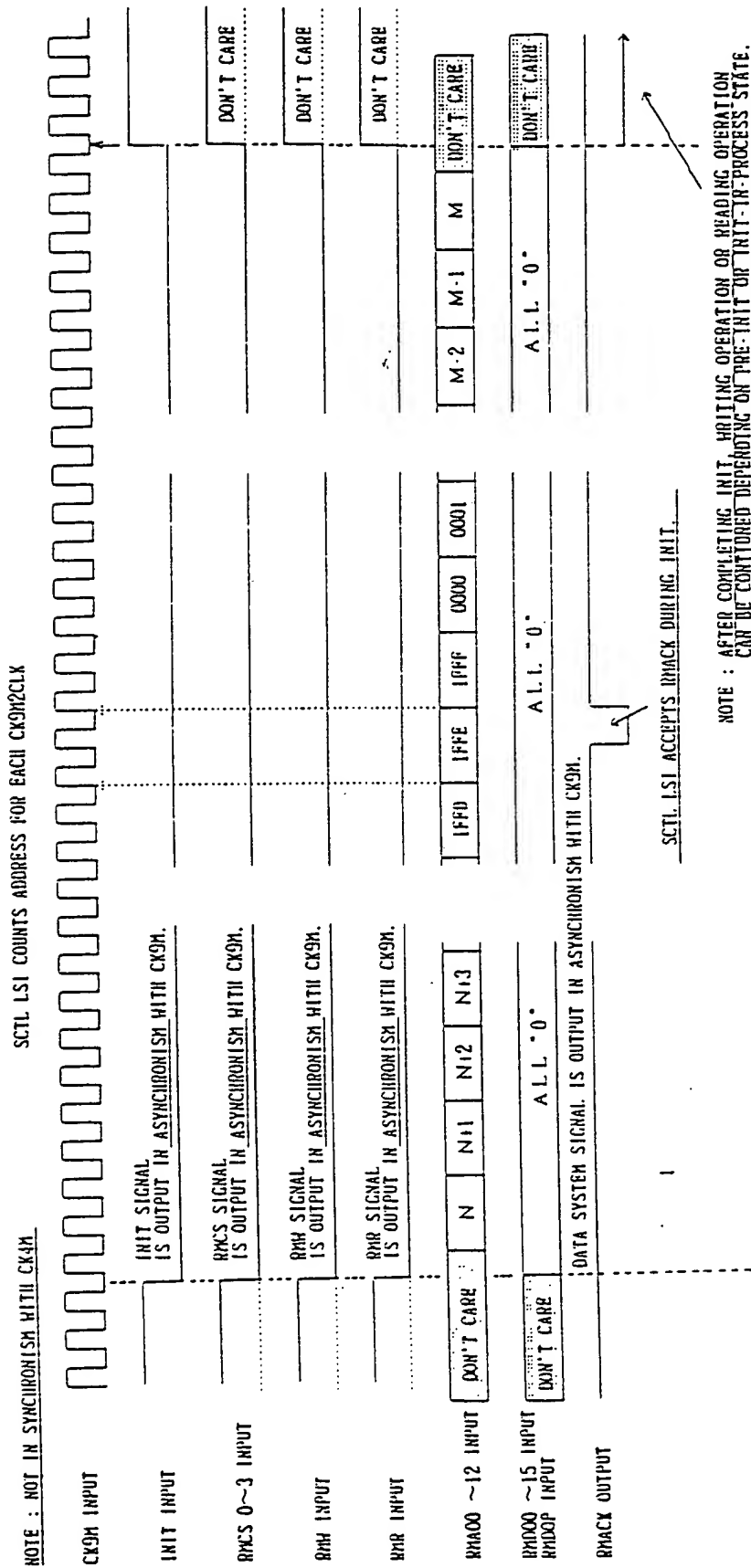


FIG. 560

[illegible]

- ★ Parity checker
- ☆ Parity generator
- ◇ DETECTING DISCO
- OTHER ALARMS

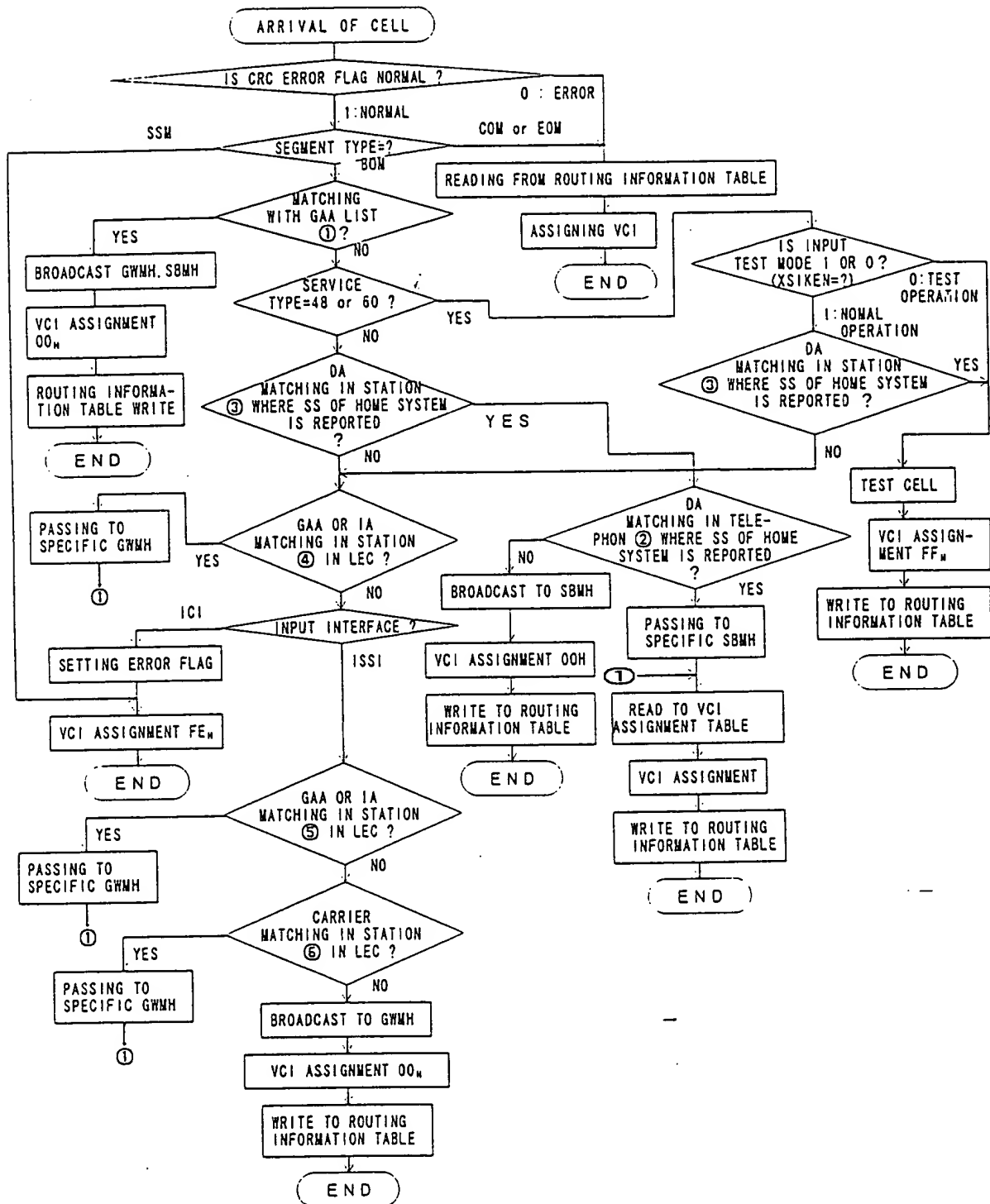
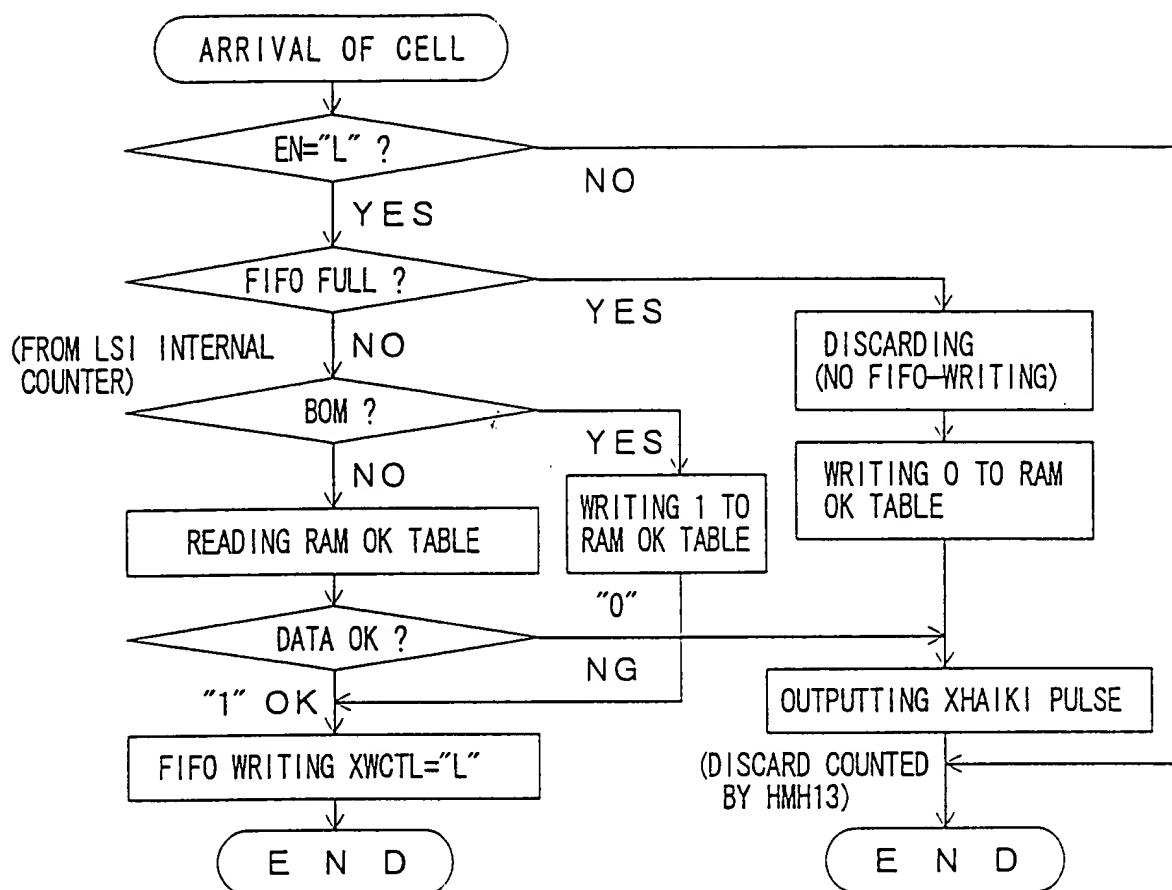


FIG. 562

(1) FLOWCHART OF FIFO WRITING UNIT (REALIZED BY RU CTL LSI)



(1) FLOWCHART OF FIFO READ CLOCK GENERATING UNIT (REALIZED BY BROX/CAST LCA)

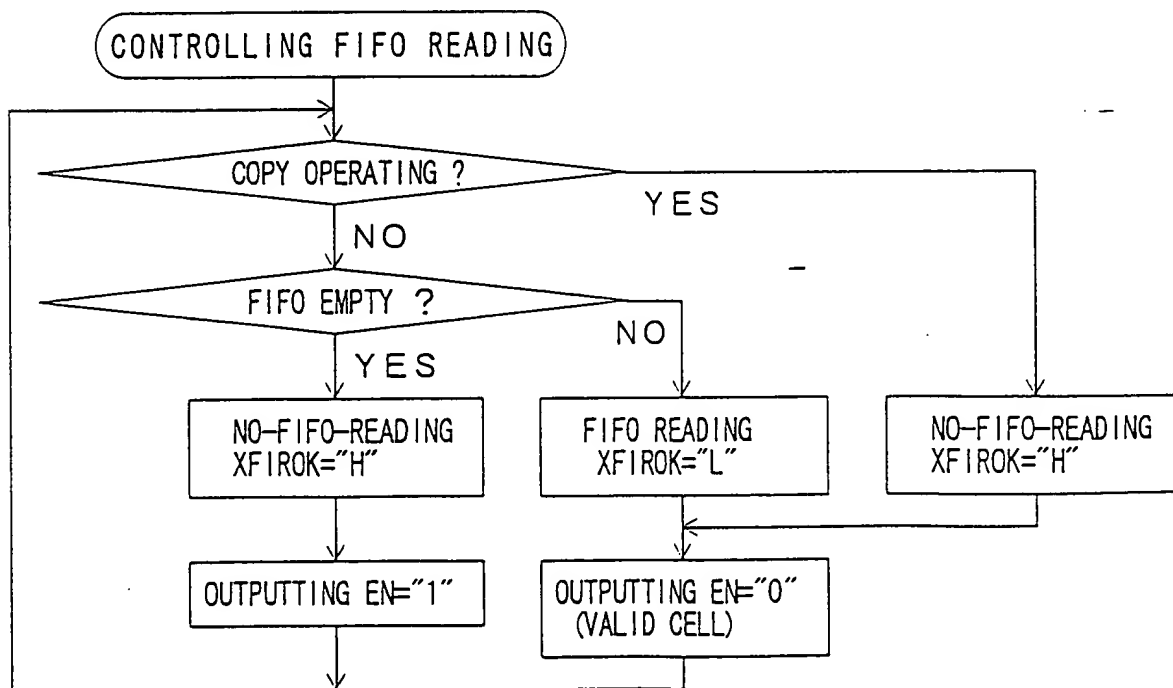


FIG. 563

(3) FLOWCHART OF COPY CONTROL UNIT (REALIZED BY BROADCAST LCA)

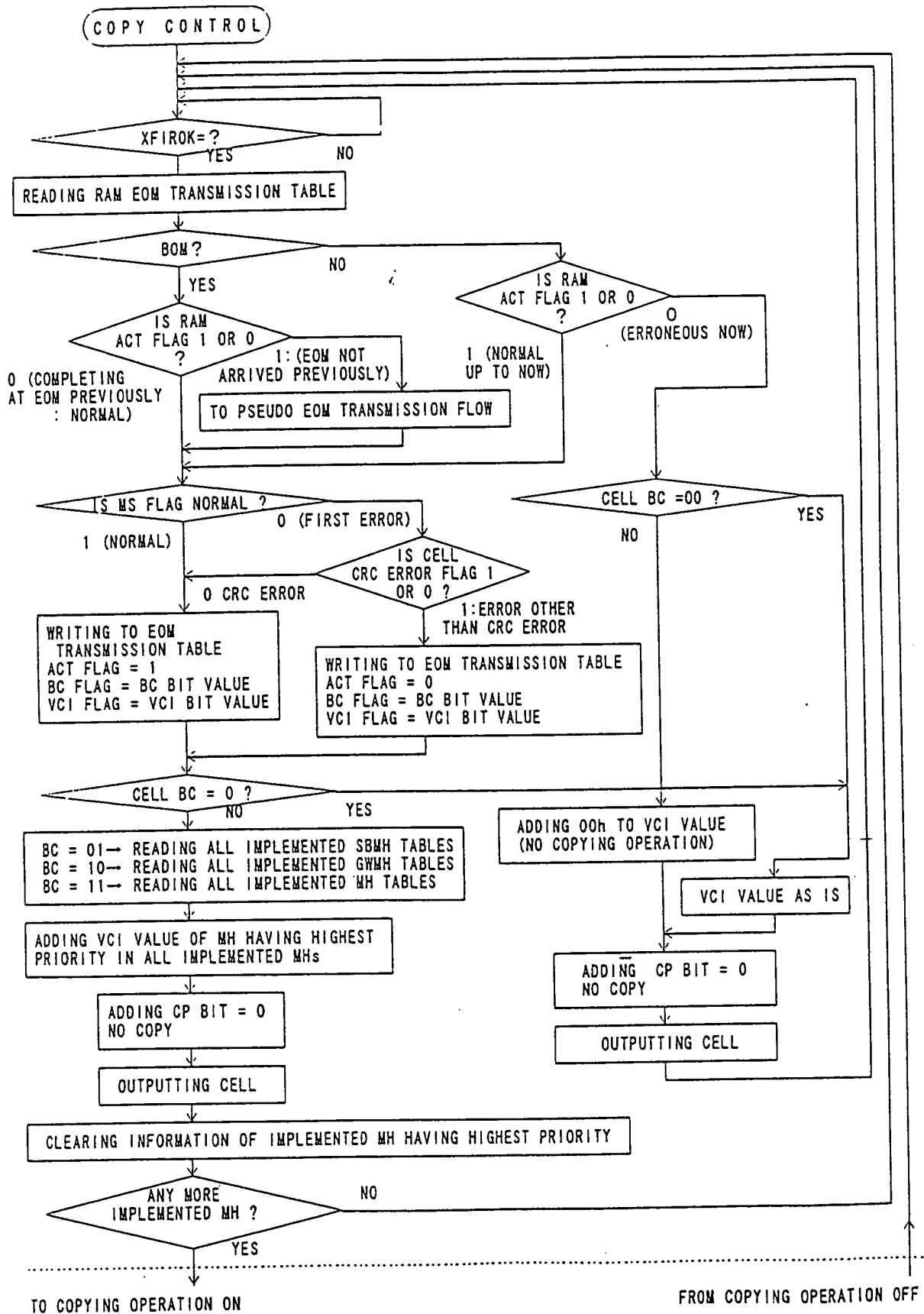


FIG. 564

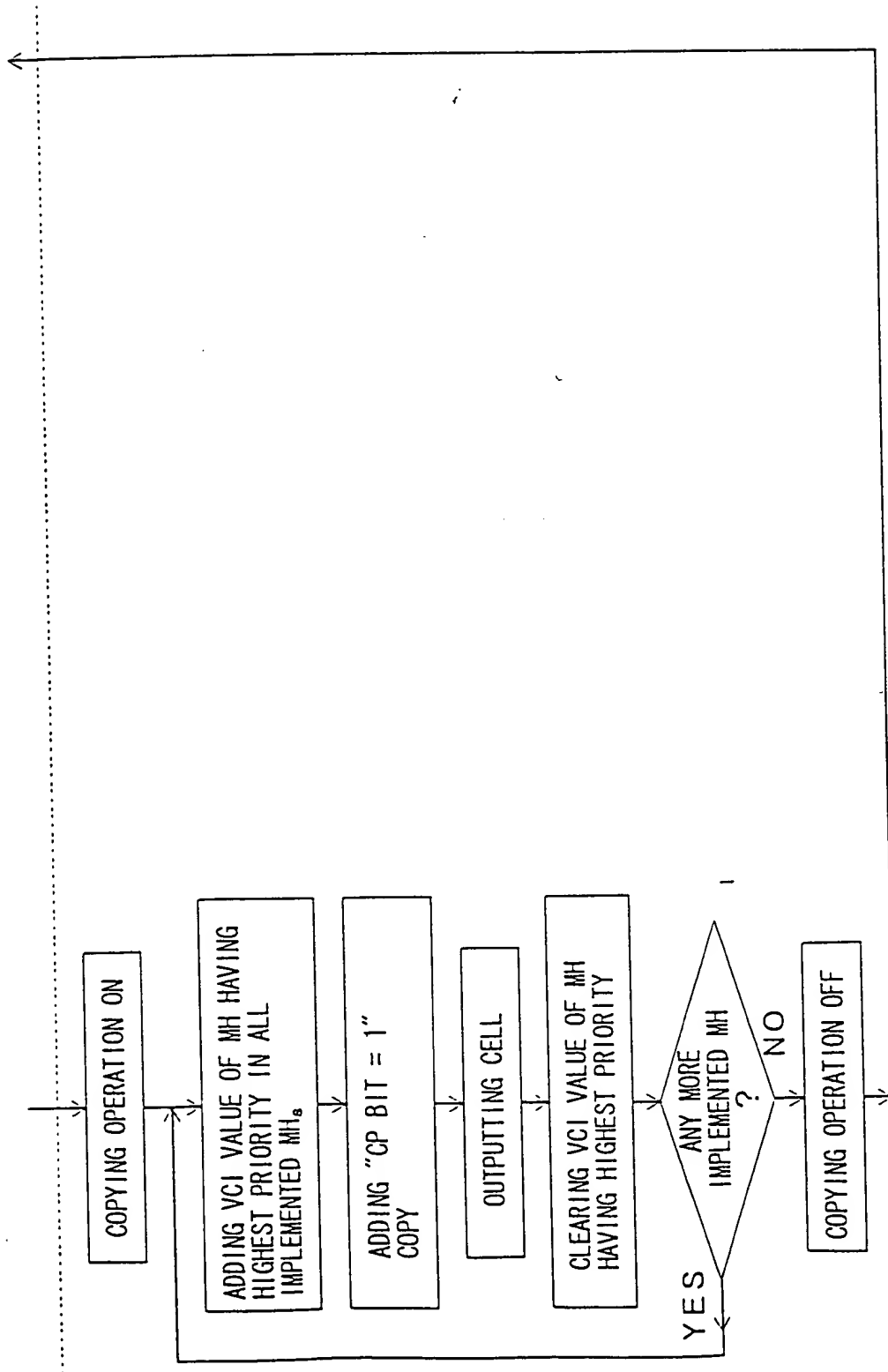
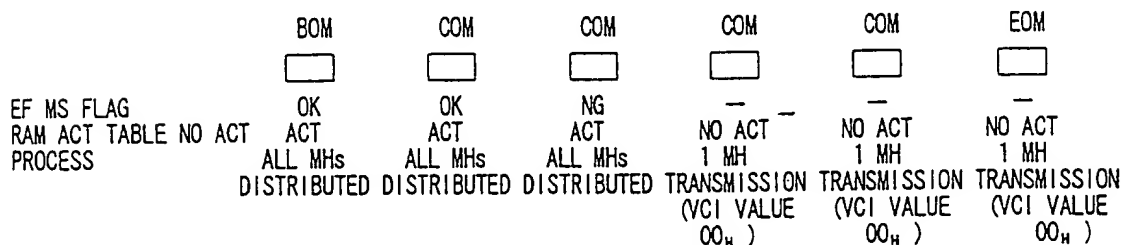
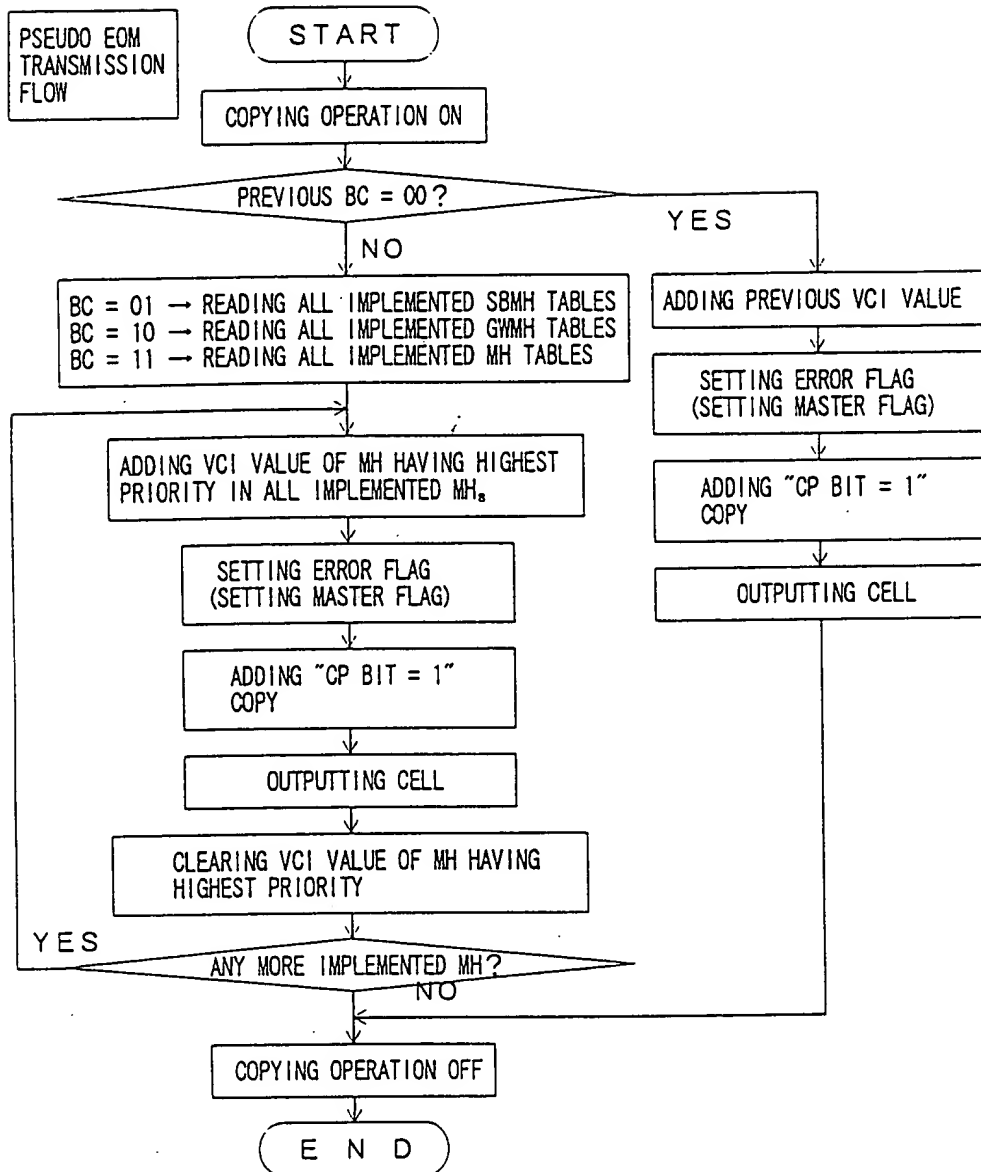


FIG. 565



- (4) FIFO MONITOR UNIT OPERATION CONDITION (REALIZED BY RU CTL LSI)
- COUNTING UP WITH FIFO WRITE
 - COUNTING DOWN WITH FIFO READ
 - FIFO FULL OUTPUT WITH COUNT VALUE 511
 - FIFO EMPTY OUTPUT WITH COUNT VALUE 0

FIG. 566

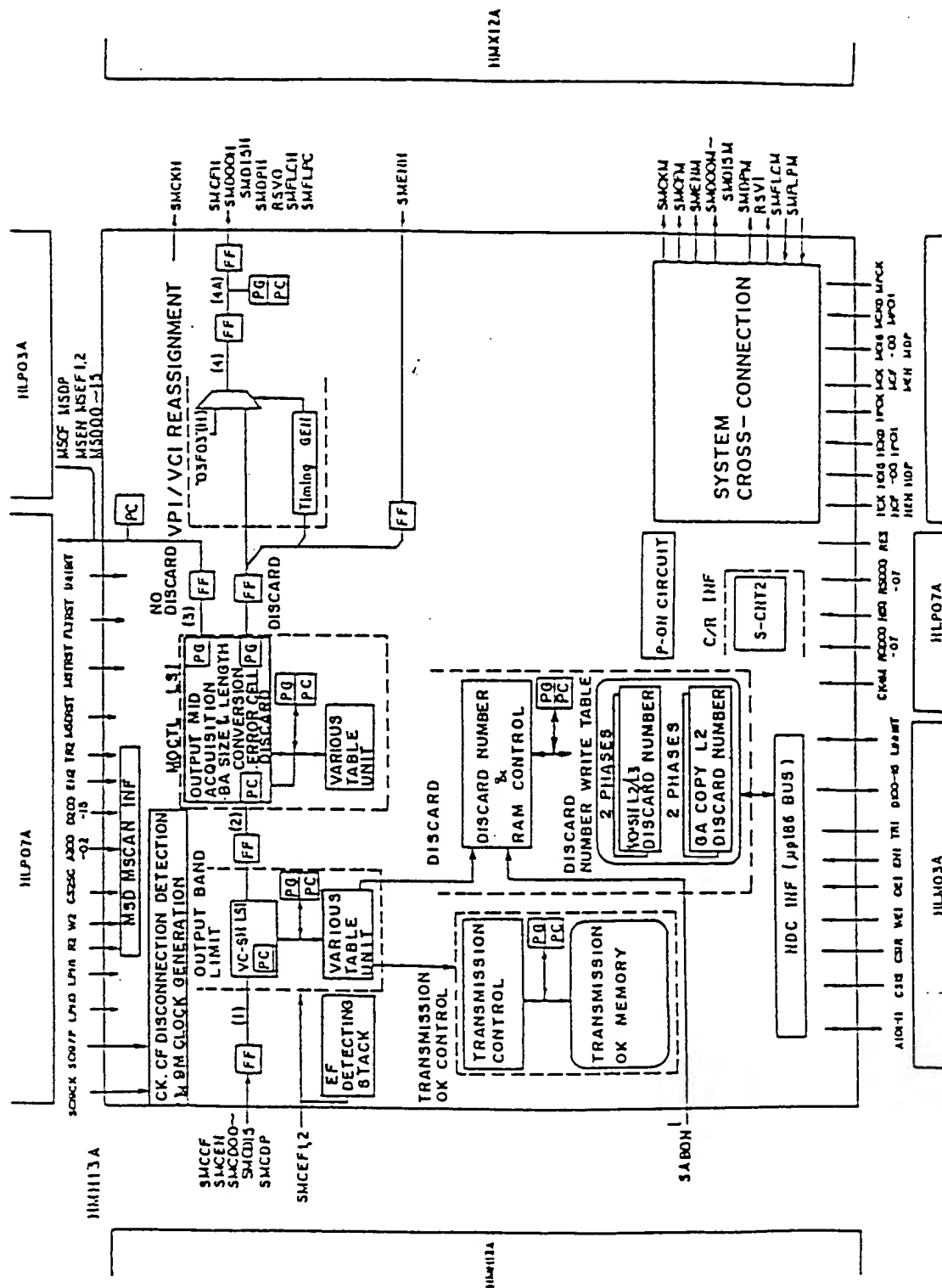
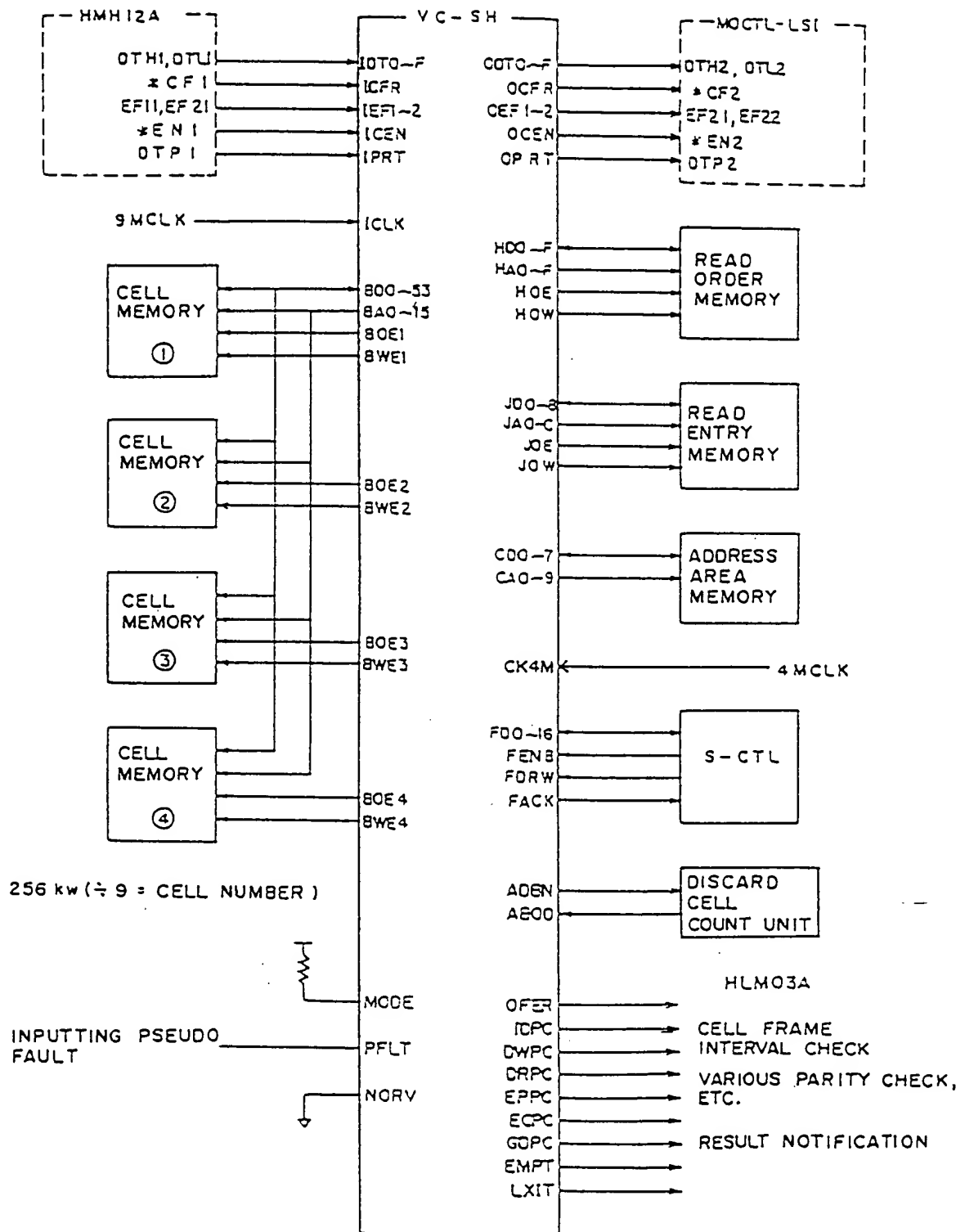


FIG. 567

00000-00000



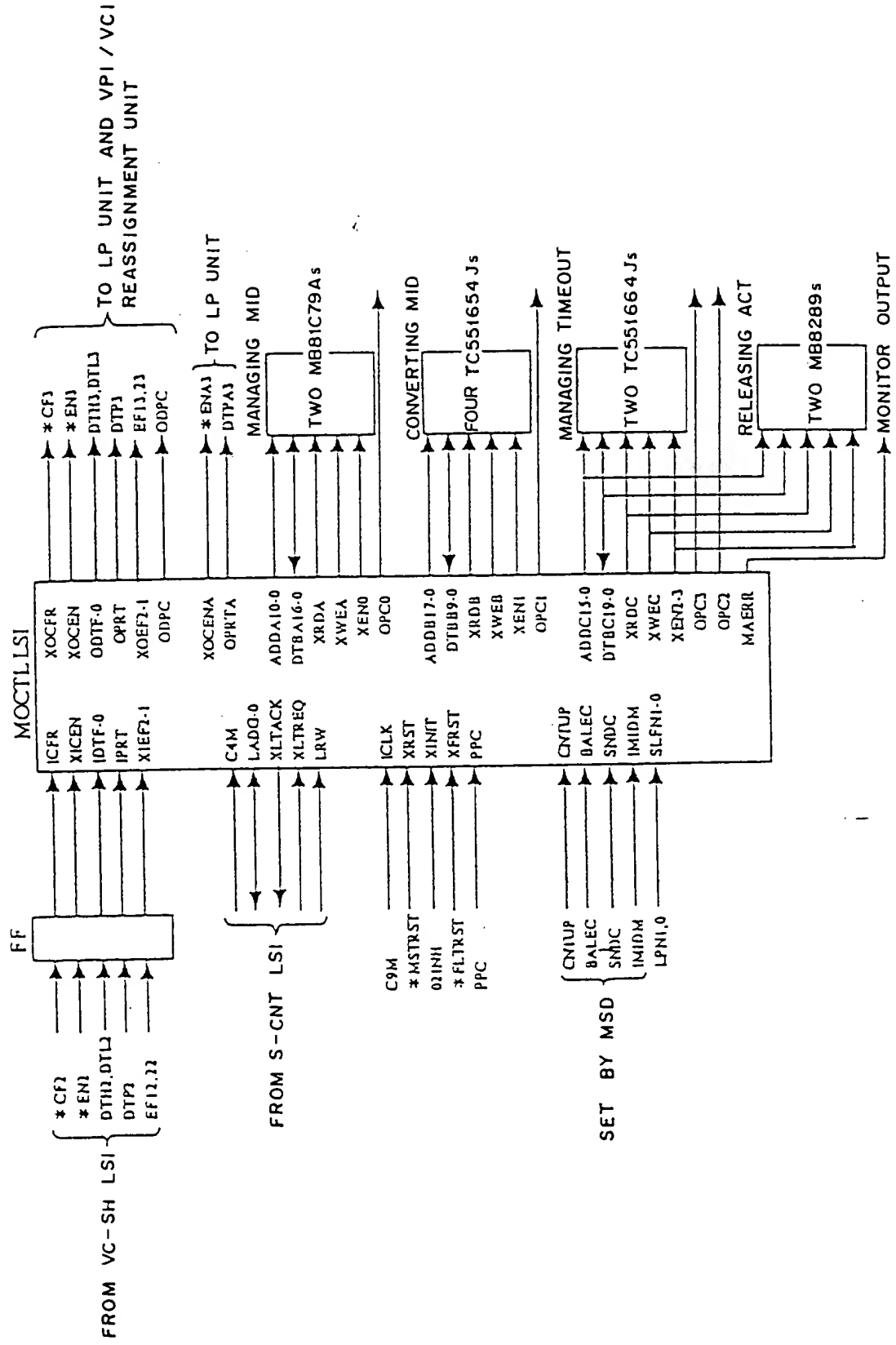


FIG. 569

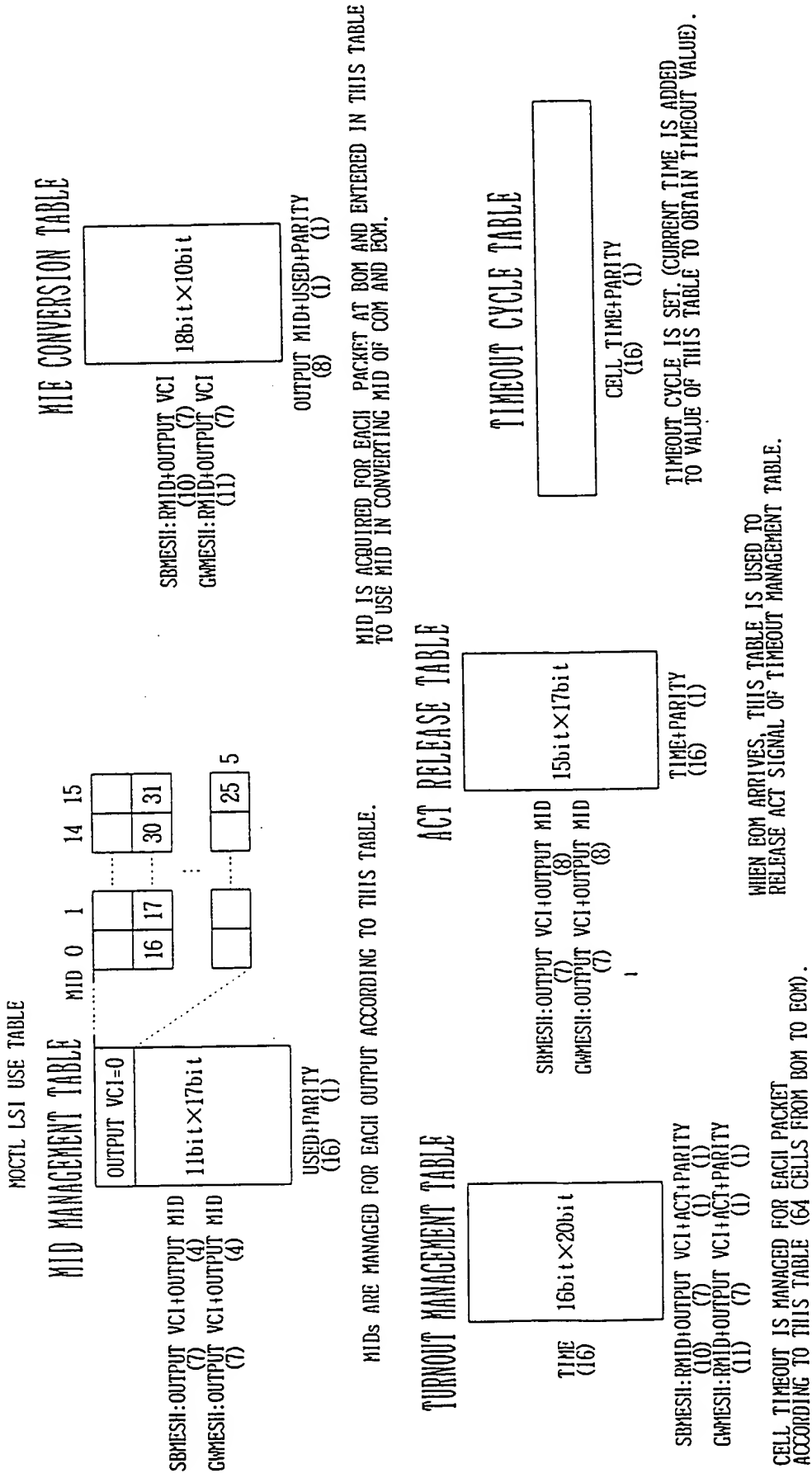


FIG. 570

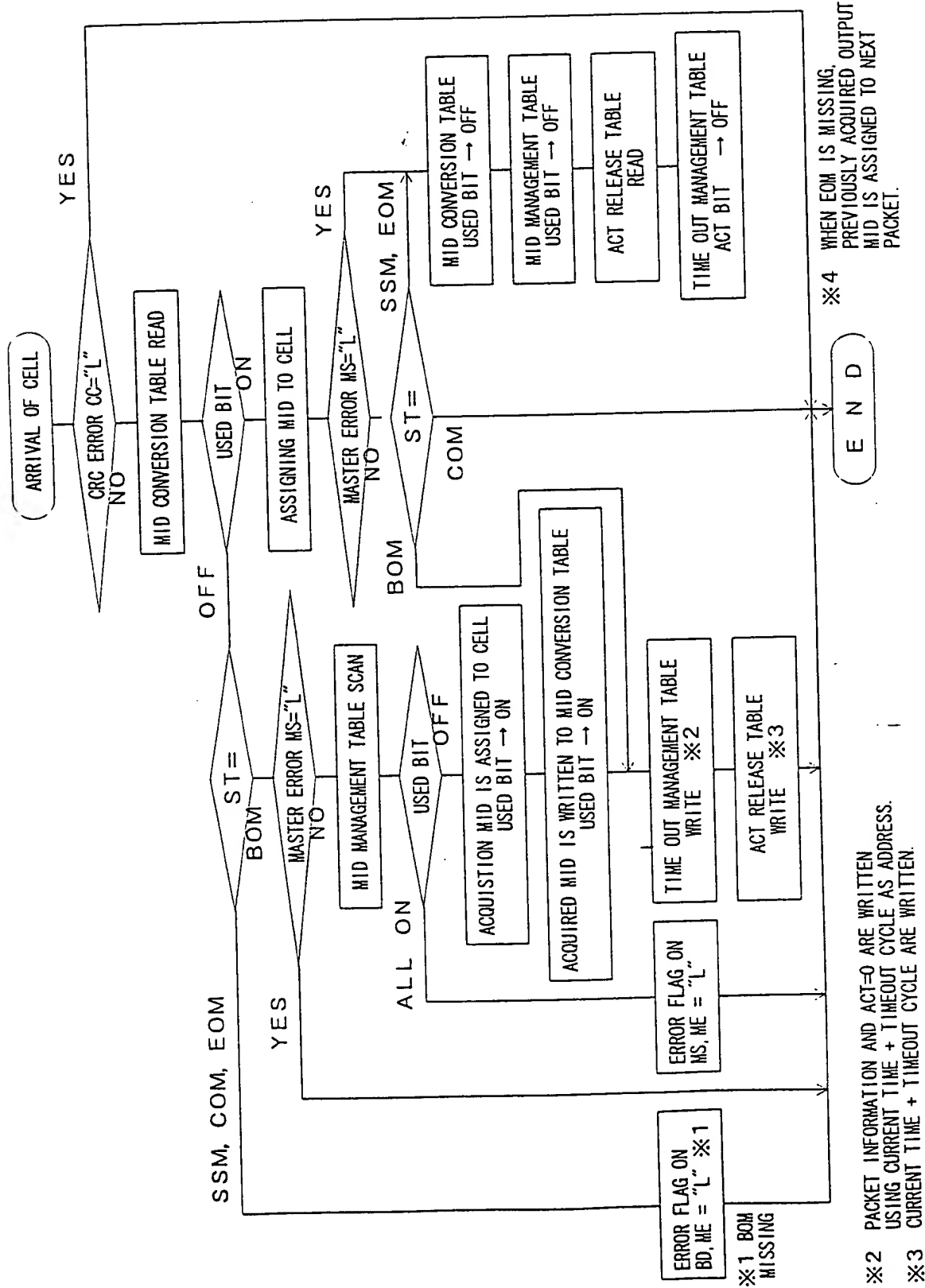
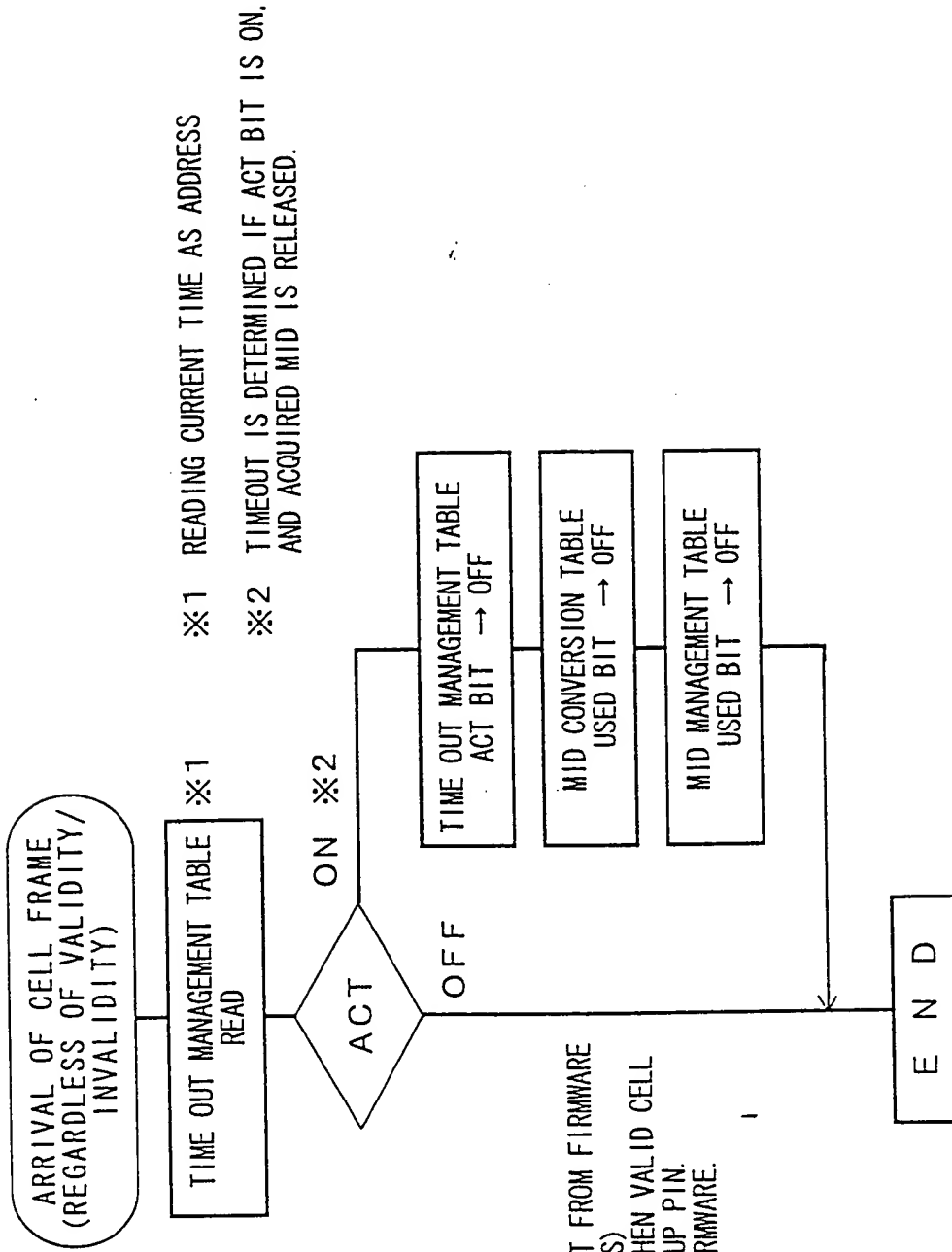


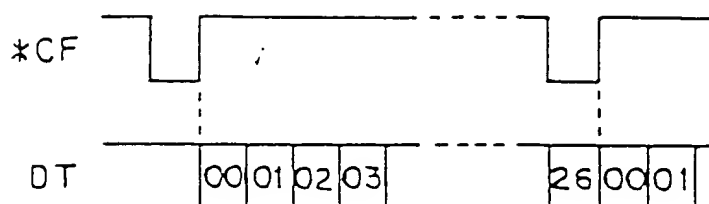
FIG. 571



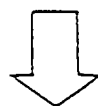
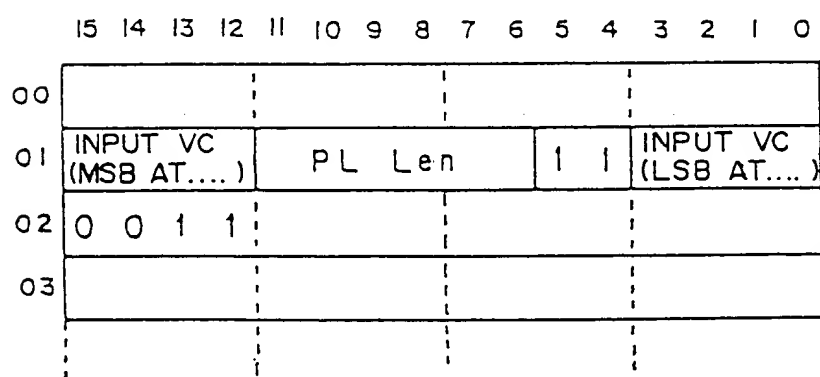
- TIMEOUT CYCLE TABLE IS SET FROM FIRMWARE
- AT INITIALIZATION (16 BITS)
- CLOCK CAN BE COUNTED UP WHEN VALID CELL
- IS ENTERED BY SETTING CNTUP PIN.
- CLOCK CAN BE READ FROM FIRMWARE.

FIG. 572

VPI / VCI REASSIGNMENT



HMH12A → HMH13A INPUT CELL FORMAT



HMH13A OUTPUT CELL FORMAT

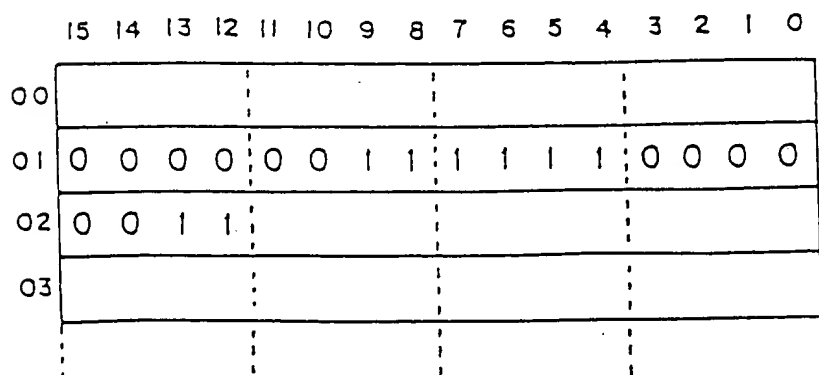


FIG. 573

669360-272200

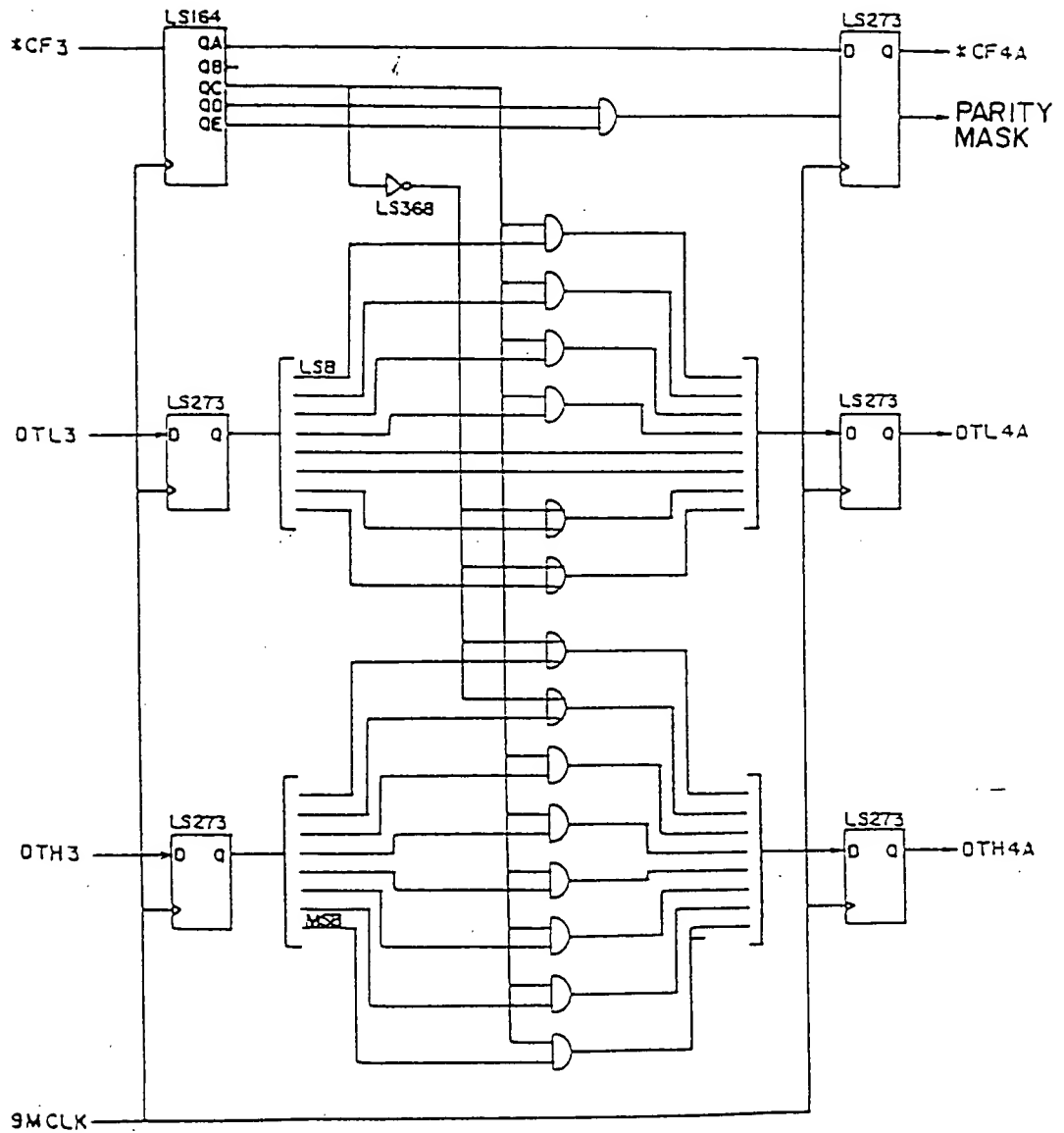


FIG. 574

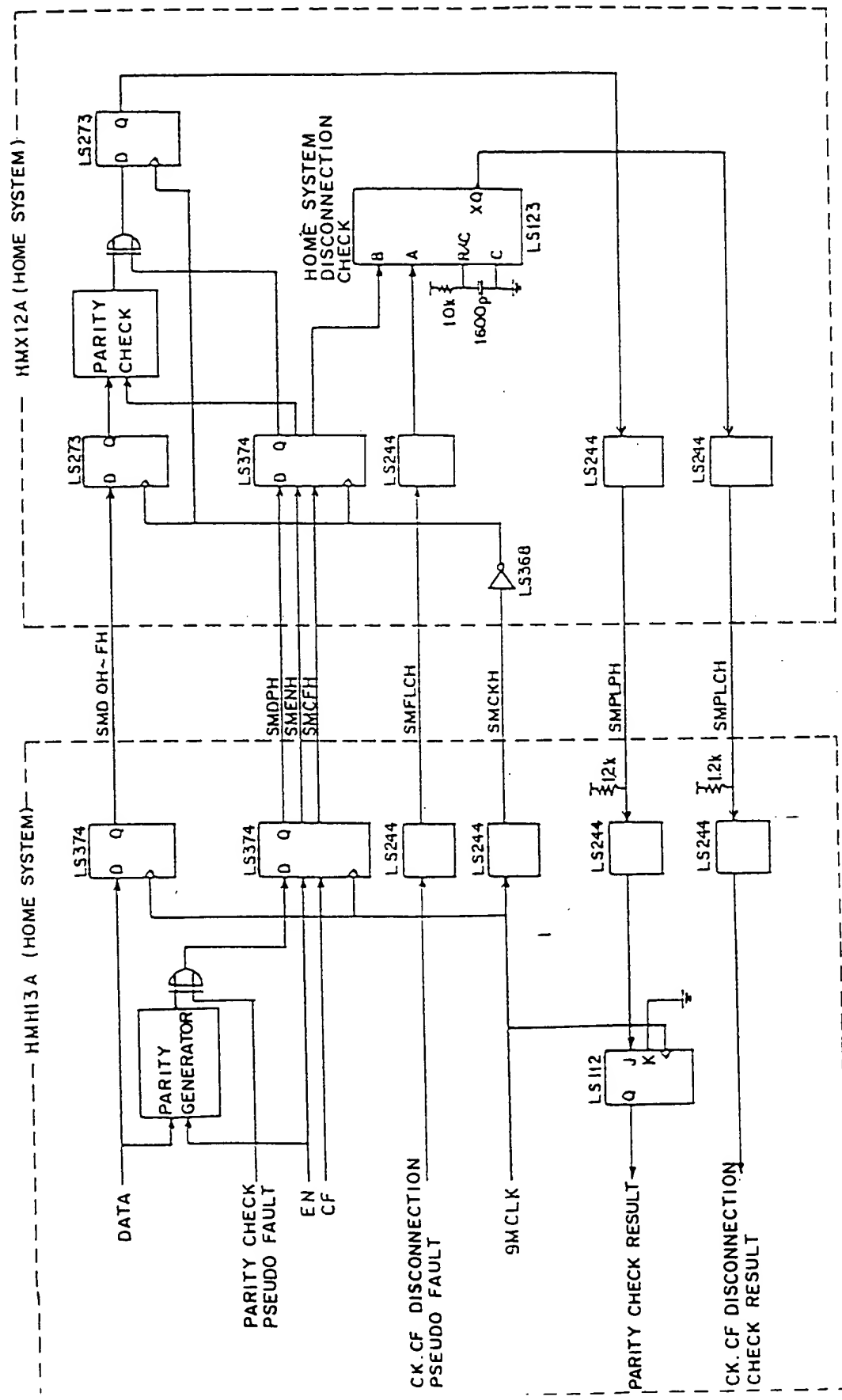
[illegible]

FIG. 575

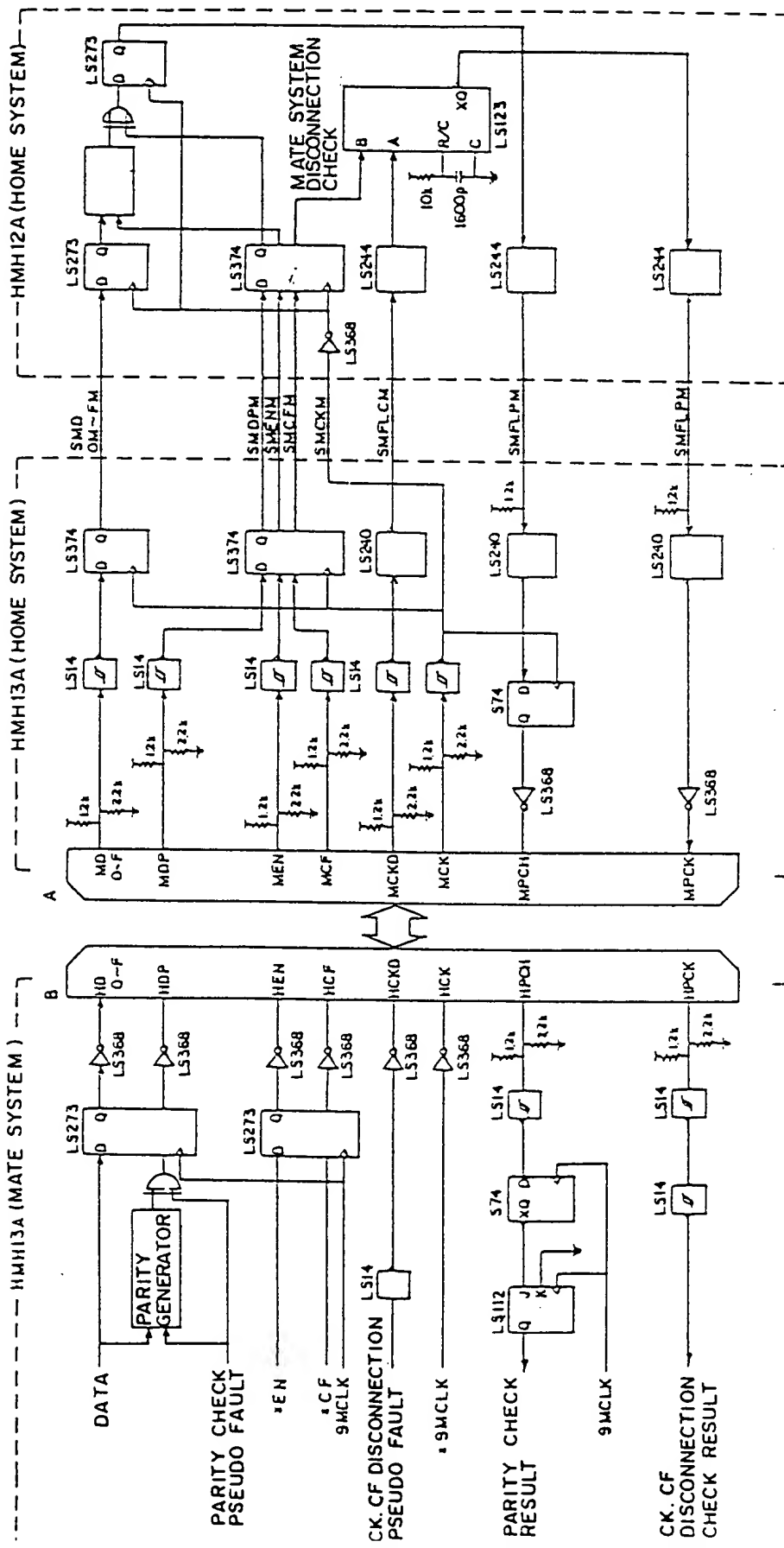


FIG. 576

669220-2

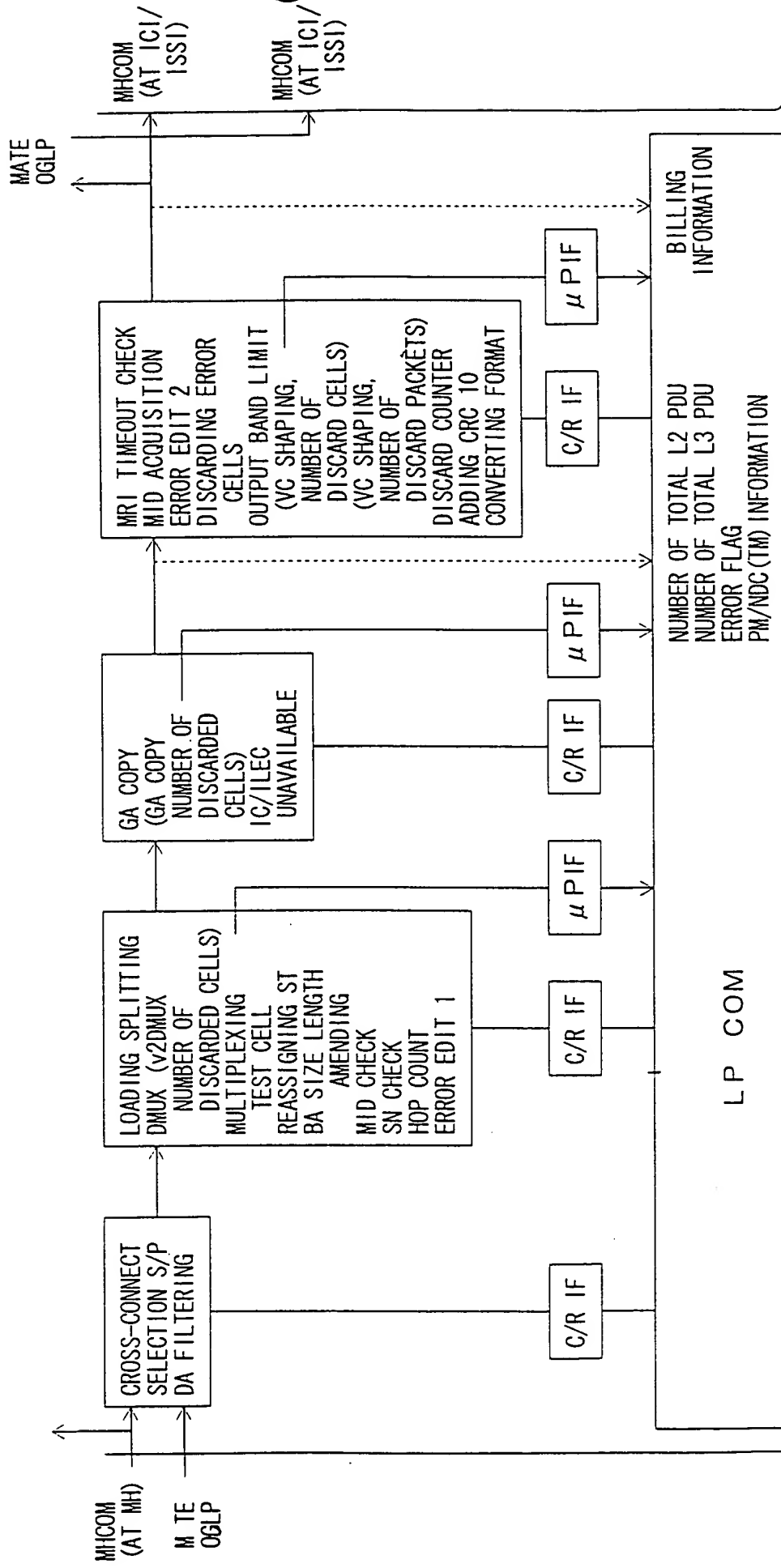


FIG. 577

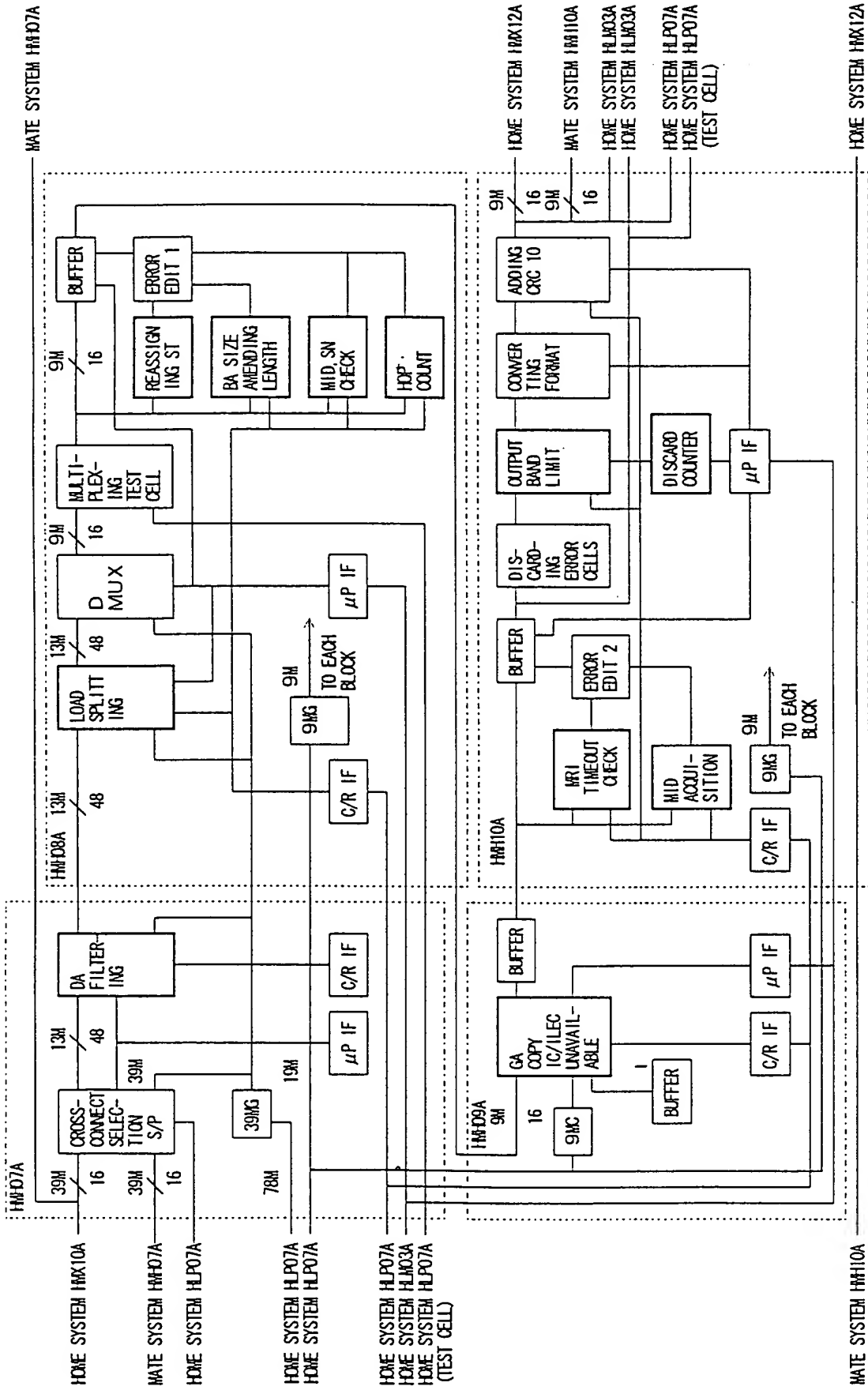


FIG. 578

The diagram illustrates the architecture of the H-1000 computer system, organized into three main functional areas, each interfaced with a HOME SYSTEM HMX10A.

- Top Section (HOME SYSTEM HMX10A):** This section includes a CELL DLY block connected to a 9M bus. It features a V2D MUX (16 lines) and a L DSP (48 lines) connected to a 13M bus. A RAM block is also present. The output of the L DSP is connected to a μP IF block.
- Middle Section (HOME SYSTEM HMX10A):** This section contains a DA CTL (x5) block connected to a 39M bus. It also includes a C/R IF block and a μP IF block. The output of the DA CTL is connected to a μP IF block.
- Bottom Section (HOME SYSTEM HMX10A):** This section includes a V ID MUX (16 lines) connected to a 39M bus. It also features a C/R IF block and a μP IF block. The output of the V ID MUX is connected to a μP IF block.

The diagram shows the interconnections between these blocks and the external systems (HOME SYSTEM HMX10A, HOME SYSTEM HMX10A, HOME SYSTEM HMX10A) via various buses and interfaces.

F1G. 579

	Message	Error Flag	E1 MS	E2 MT	E1 MC	E2 MA	E2 SN	E2 LC	E2 GA	E2 EM	PVC
A	BOM with Unexpected MID		ON			ON					
	COM with Unexpected MID		ON		ON						
	EOM with Unexpected MID		ON			ON					
B	Unexpected SN Error		ON		OK	OK	ON				
C	ILEC/IC Unavailable		ON					ON			
D	CARRIER SELECTION		OK								
E	RMID ACQUISITION		OK								
F	MRI Time Out			ON							
G	GA COPY		ON		OK	OK	ON				
H	LIMIT OF SIMULTANEOUS TRANSMISSION NUMBER		ON		OK	OK				ON	

'ON': EF INDICATING "ON" WHEN CHECK RESULT OUTPUTS NG
 'OK': CHECK IS MADE ONLY WHEN OK-MARKED EF INDICATES "OK."
 'NO MARK': CHECK IS MADE REGARDLESS OF OK OR NG OF 'NO MARK' EF
 'M': NO CHECK IS MADE FOR INTER-MESH PVC TEST CELL.

FIG. 581

HMH07 INPUT CELL (FROM SB)
INTER-MH BOM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	0																																	
01	0		0		0		0		0		0		1		1		1		1		1		1		0		0		0		0			
02	0		0		1		1		INPUT VCI (SOURCE MH ID)														PT				CLP							
03	1		0		SN										INPUT MID																			
04	0		0		0		0		0		0		0		0		SIP PBEtag																	
05	SIP BAsize																																	
06	ISSIP DA																																	
07																																		
08																																		
09																																		
10	SA																																	
11																																		
12																																		
13																																		
14	High Layer Protocol										Pad I				QOS						CI		HE Len											
15	Bridging																																	
16	Header Extension (SIP)																																	
17																																		
18																																		
19																																		
20																																		
21																																		
22	Ingress Interface Type														ES		DC																	
23	Carrier																																	
24	Incoming Network ID																																	
25	Incoming ICI Transmission Path Set																																	
26	PL Len														CRC																			

FIG. 582

SIP SSM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	0																
01	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT		CLP		
03	0	1	SN						INPUT MID								
04	0	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize																
06	SIP DA																
07																	
08																	
09																	
10	SA																
11																	
12																	
13																	
14	High Layer Protocol						Pad l		QOS				CI		HE Len		
15	Bridging																
16	Header Extension																
17																	
18																	
19																	
20																	
21																	
22	Information																
23																	
24	0	0	0	0	0	0	0	0	0	SIP BEtag							
25	SIP Length																
26	PL Len.								CRC								

FIG. 585

HMM07 INPUT CELL (FROM GW)
 INTER-MH BOM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00		0														
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)							PT		CLP		
03	1	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	0	ISSIP Btag						
05	SIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type															
15																
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	Hop Count Ind						
23	Carrier															
24	Incoming Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.						If	(CRC)								

VALID ONLY WHEN INPUT INTERFACE TO SS OF
 HOME SYSTEM IS ISSI AND IF BIT INDICATES 0

FIG. 588

INTER-MH SSM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00		0															
01	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT		CLP		
03	1	1	SN				INPUT MID										
04	Unknown																
05																	
06																	
07																	
08																	
09																	
10																	
11																	
12																	
13																	
14																	
15																	
16																	
17																	
18																	
19																	
20																	
21																	
22																	
23																	
24																	
25																	
26	PL Len.										CRC						

FIG. 589

SIP BOM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	0															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT		CLP	
03	0	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol						Pad l		QOS				CI		HE Len	
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						If		(CRC)							

FIG. 590

0000000000000000

SIP SSM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	0																	
01	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	
02	0	0	1	1	INPUT VCI (SOURCE MH ID)								PT		CLP			
03	0	1	SN					INPUT MID										
04	0	0	0	0	0	0	0	0	SIP BEtag									
05	SIP BAsize																	
06	SIP DA																	
07																		
08																		
09																		
10	SA																	
11																		
12																		
13																		
14	High Layer Protocol						Pad 1		QOS				CI		HE Len			
15	Bridging																	
16	Header Extension																	
17																		
18																		
19																		
20																		
21																		
22	Information																	
23																		
24	0	0	0	0	0	0	0	0	0	BEtag							-	
25	SIP Length																	
26	PL Len.						If		(CRC)									

FIG. 591

HMH08 INPUT CELL (FROM GW)
INTER-MH BOM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	ST	DM	DC	MCHPO				MADRO								
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)						PT		CLP			
03	1	0	SN				INPUT MID									
04	0	0	0	0	0	0	0	0	ISSIP Btag							
05	SIP BAsize															
06	ISSIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	Service type															
15																
16	Header Extension															
17																
18																
19																
20																
21																
22	Ingress Interface Type								ES	Hop Count Ind						
23	Carrier															
24	Incominng Network ID															
25	Incoming ICI Transmission Path Set															
26	PL Len.						If	(CRC)								

VALID ONLY WHEN INPUT INTERFACE TO SS OF
HOME SYSTEM IS ISSI AND IF BIT INDICATES 0

FIG. 594

66920 66200

INTER-MH SSM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	ST	DM	DC	MCHPO	MADRO											
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	INPUT VCI (SOURCE MH ID)							PT		CLP		
03	1	1	SN		INPUT MID											
04	Unknown															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
23																
24																
25																
26	PL Len.				CRC											

FIG. 595

60930-672200

INTER MII SSM CELL

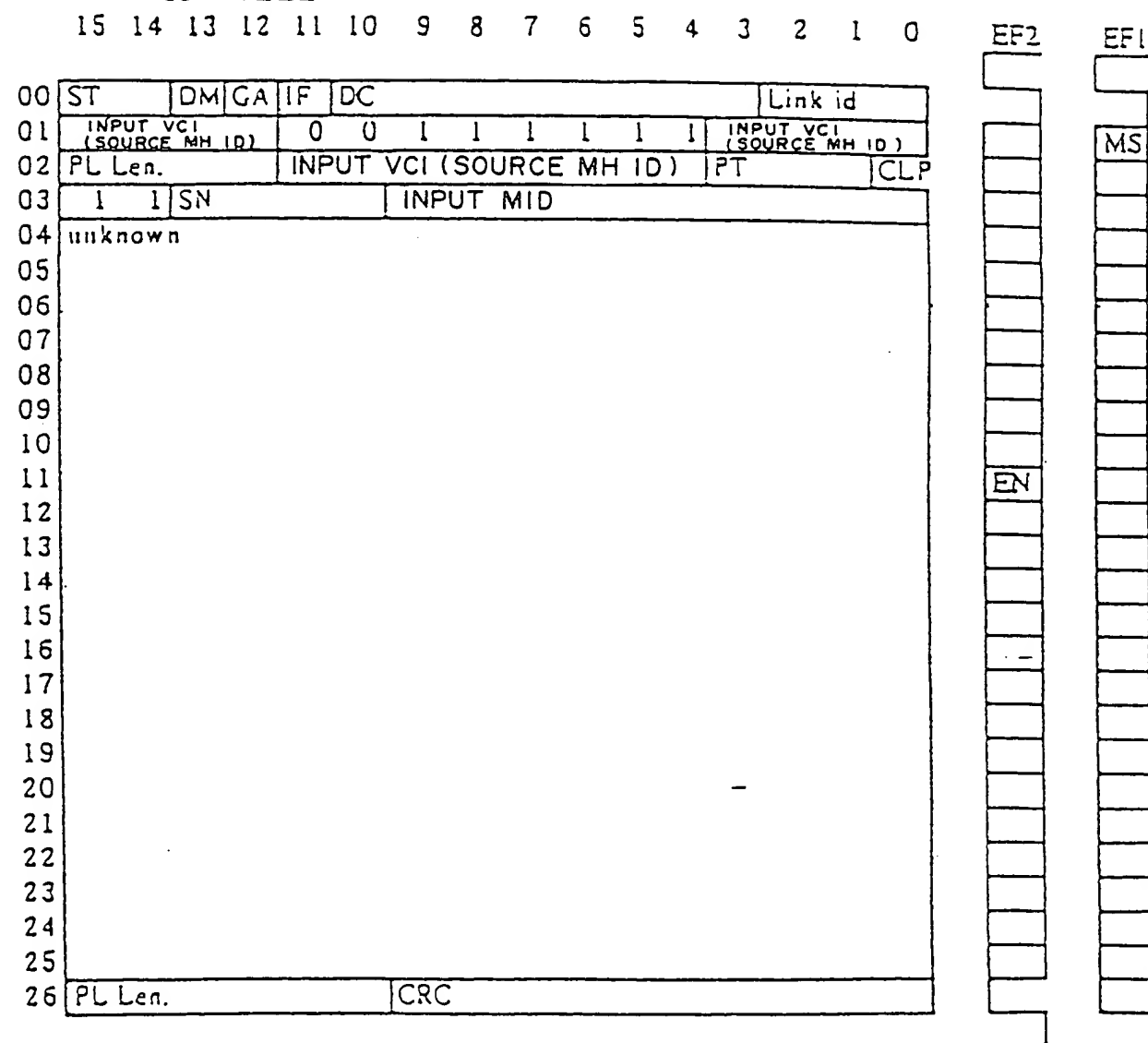


FIG. 601

0000000000000000

SIP SSM CELL

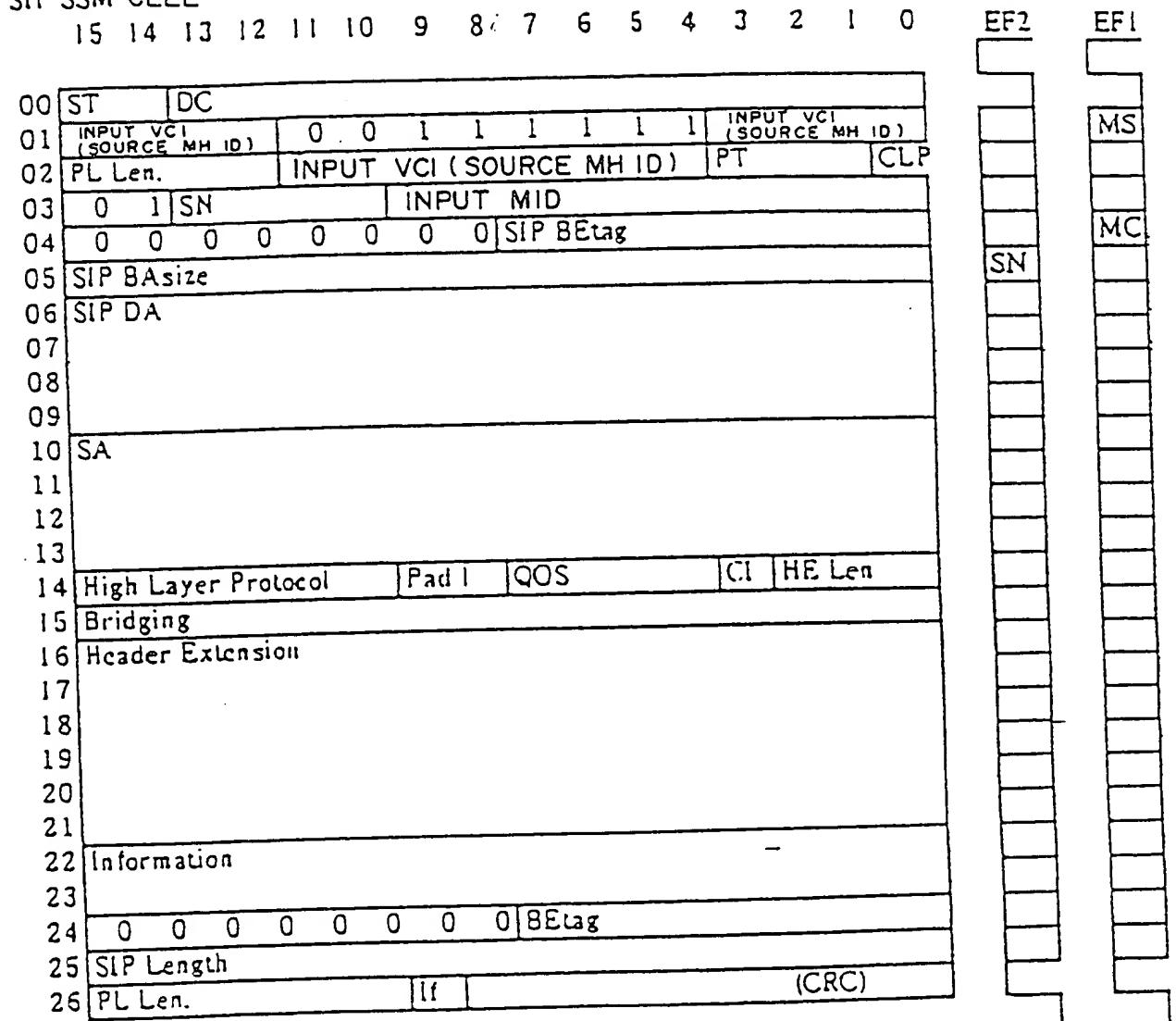


FIG. 603

[illegible]

00	ST	DC																	
01	INPUT VCI (SOURCE MH ID)		0	0	1	1	1	1	1	1	1	INPUT VCI (SOURCE MH ID)							
02	PL Len.		INPUT VCI (SOURCE MH ID)								PT				CLP				
03	0	1	SN				INPUT MID												
04	Information																		
05																			
06																			
07																			
08																			
09																			
10																			
11																			
12																			
13																			
14																			
15																			
16																			
17																			
	Reserved										SEtag								
	Length(SIP)																		
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
26	PL Len.										1	(CRC)							

[illegible]

•

0092724-03600

SIP BOM CELL

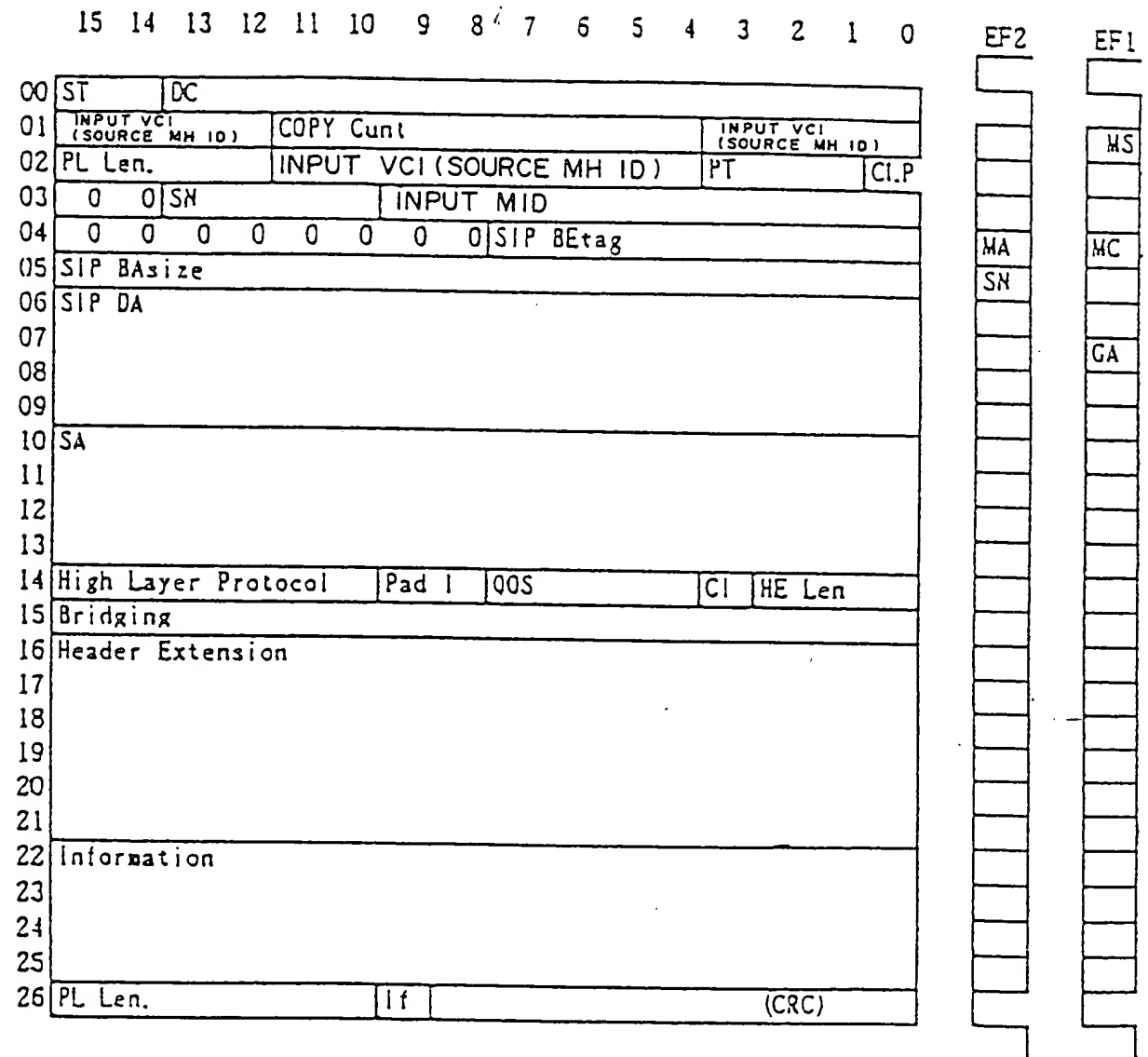


FIG. 608

66920-012200

SIP SSM CELL

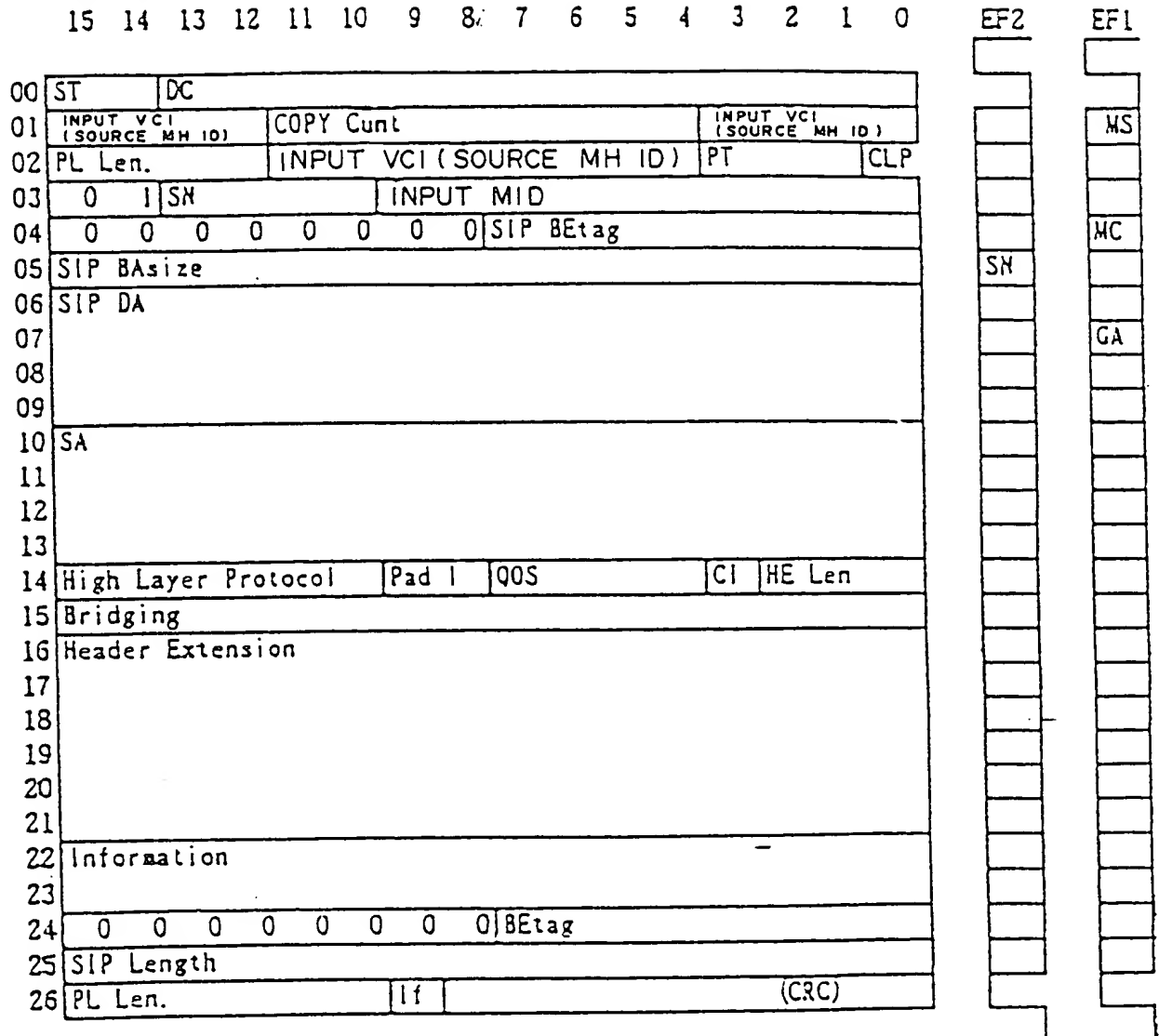


FIG. 609

[illegible]

00	ST	DC		
01	INPUT VCI (SOURCE MH ID)	COPY Cunt	INPUT VCI (SOURCE MH ID)	
02	PL Len.	INPUT VCI (SOURCE MH ID)	PT	CLP
03	0 0 SN	INPUT MID		
04	Information			
05				
06				
07				
08				
09				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				
26	PL Len.	If	(CRC)	

[illegible][illegible]
$$\begin{array}{l} 2N \\ 2N+1 \\ 2N+2 \end{array}$$

FIG. 610

00	ST	DC																		
01	INPUT VCI (SOURCE MH ID)				COPY Cunt								INPUT VCI (SOURCE MH ID)							
02	PL Len.				INPUT VCI(SOURCE MH ID)								PT				CLP			
03	0		1		SN				INPUT MID											
04	Information																			
05																				
06																				
07																				
08																				
09																				
10																				
11																				
12																				
13																				
14																				
15																				
16																				
17																				
	Reserved										BETag									
	Length (SIP)																			
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
26	PL Len.				If				(CRC)											

[illegible][illegible]

FIG. 611

DATA INTERFACE BETWEEN OGLP AND LPCOM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	ST	DM	GA	IF	DC	Link id					Link id				
01	INPUT VCI (SOURCE MH ID)		COPY Count			INPUT VCI (SOURCE MH ID)									
02	PL Len.				Link id			PT		CLP					
03	SST	SN	OUTPUT MID												
04	0	0	0	0	0	0	0	0	0	ISSIP Btag					
05	ISSIP Bsize														
06	ISSIP DA														
07															
08															
09															
10	SA														
11															
12															
13															
14	Service type														
15															
16	Header Extension														
17															
18															
19															
20															
21															
22	Ingress Interface Type					ES		Hop Count Ind*							
23	Carrier														
24	Incoming Network ID														
25	Incoming ICI Transmission Path Set														
26	PL Len.					If		I		(CRC)					

·VALID ONLY WHEN INPUT INTERFACE TO SS OF HOME SYSTEM IS ISSI AND IF BIT IS 0.

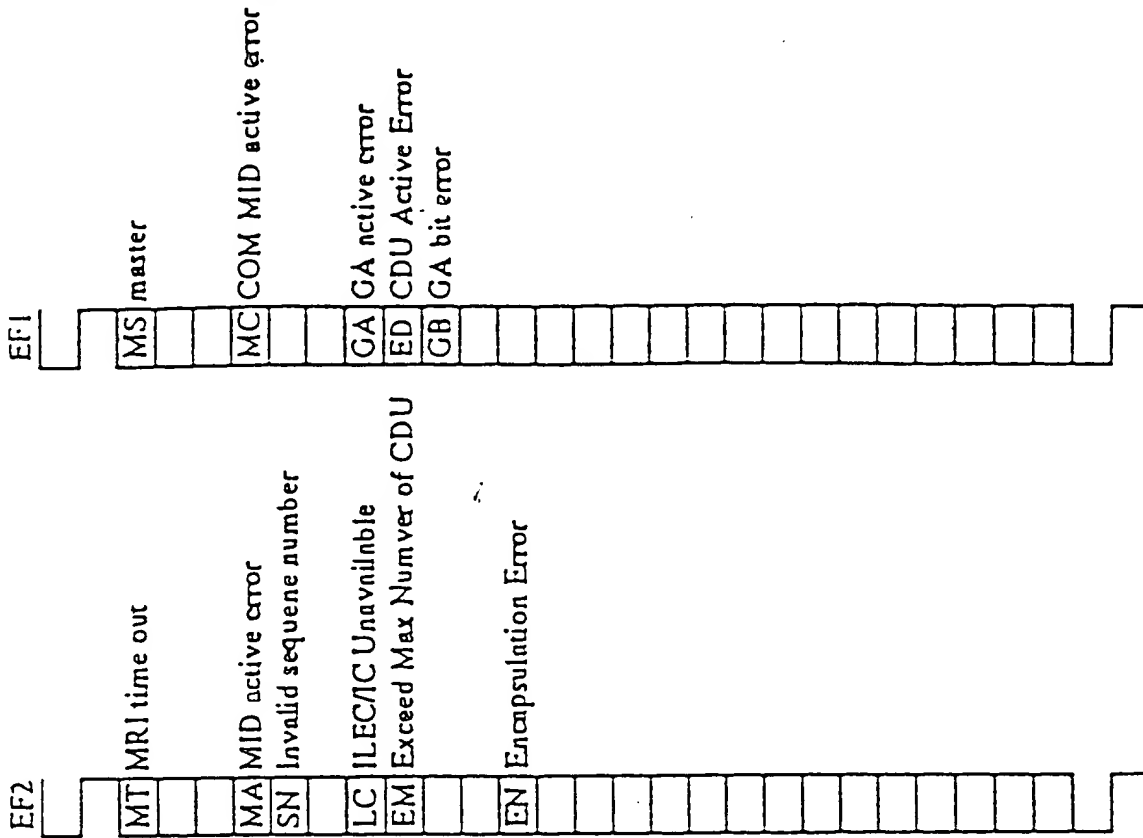


FIG. 612

009320-242200

SIP BOM CELL

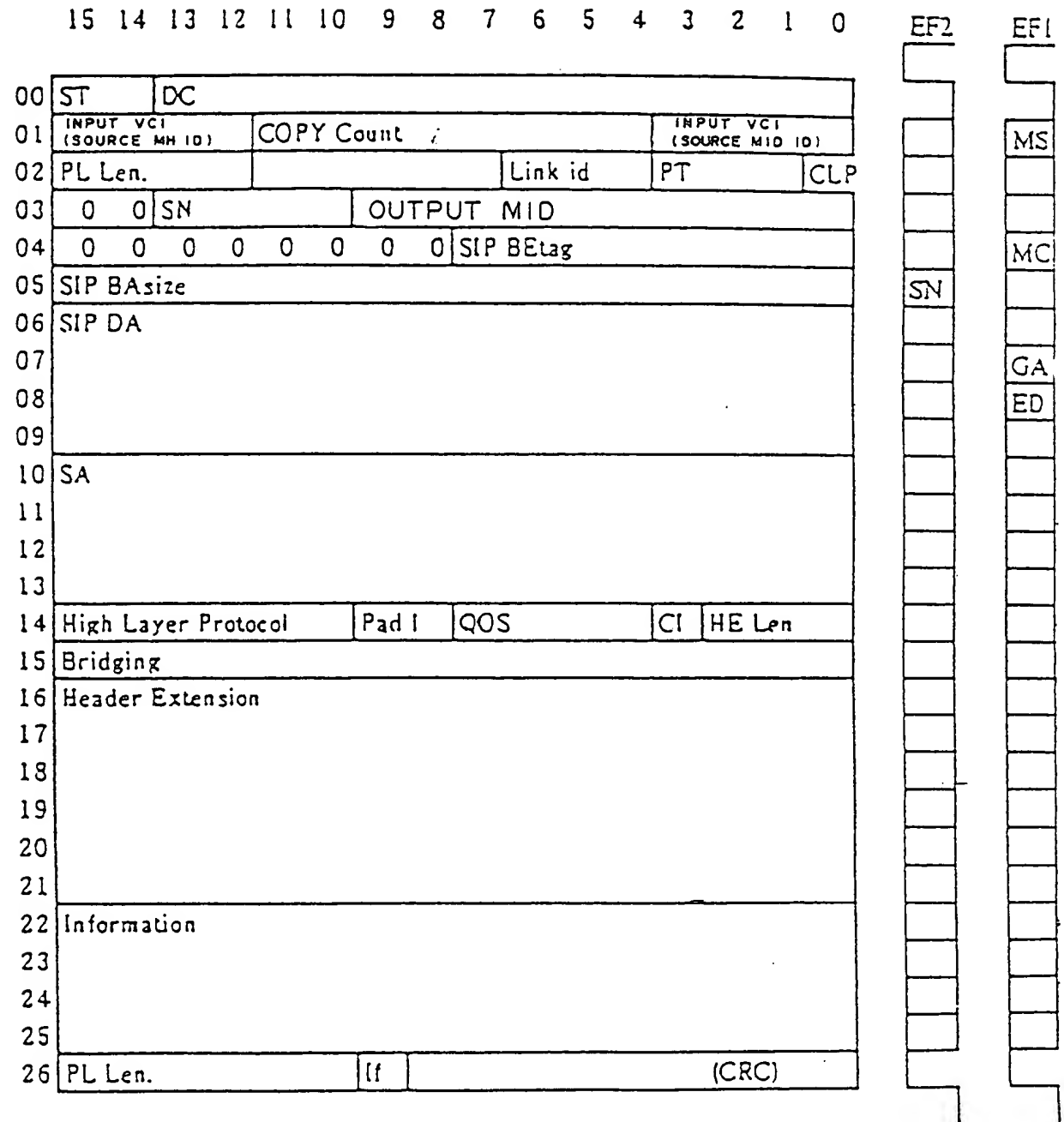


FIG. 615

0000000000000000

SIP SSM CELL

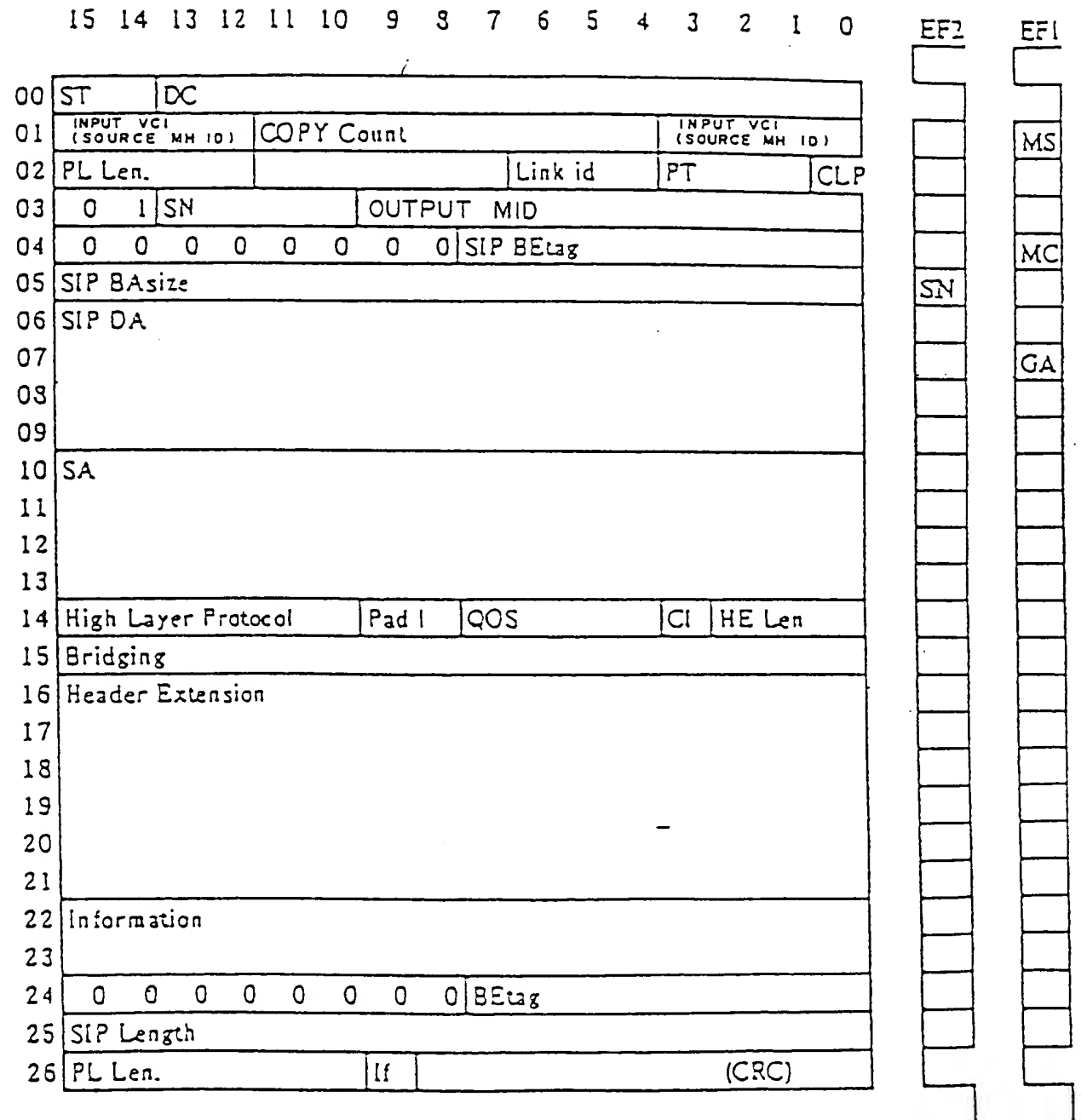


FIG. 616

SIP SSM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	DC																
01	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	0	Link ID			PT		CLP		
03	0	1	SN				0	0	0	MID							
04	0	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize																
06	SIP DA																
07																	
08																	
09																	
10	SA																
11																	
12																	
13																	
14	High Layer Protocol					Pad 1			QOS				CI	HE Len			
15	Bridging																
16	Header Extension																
17																	
18																	
19																	
20																	
21																	
22	Information																
23																	
24	0	0	0	0	0	0	0	0	0	SIP BEtag							
25	SIP Length																
26	PL Len.							CRC									

FIG. 621

SIP COM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	1	0	Link ID		PT		CLP		
03	0	0	SN				0	0	0	MID						
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
23																
24																
25																
26	PL Len.							CRC								

FIG. 622

00000000000000000000000000000000

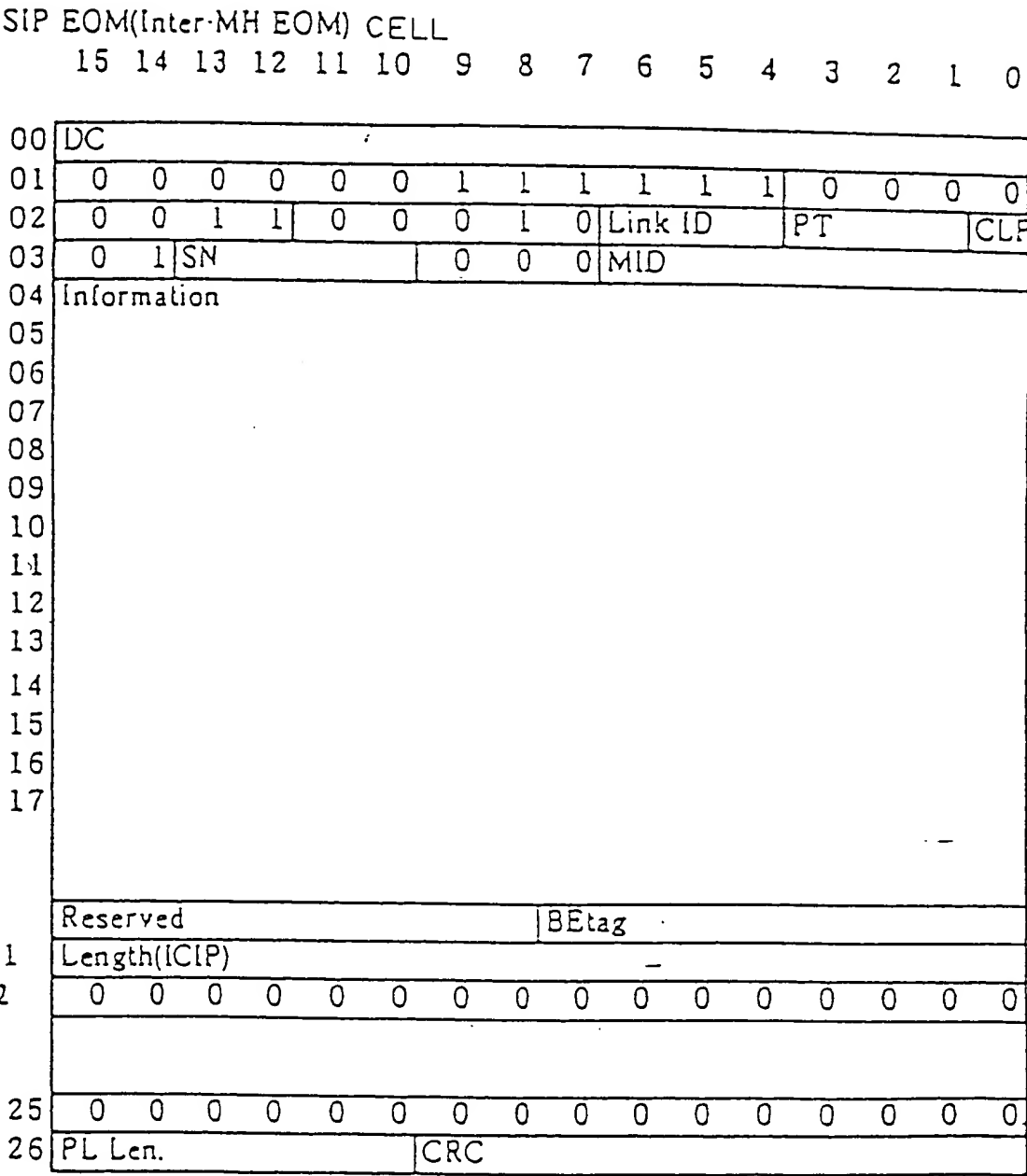


FIG. 623

6636072250

SIP BOM CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID		PT		CLP		
03	0	0	SN				0	0	0	MID						
04	0	0	0	0	0	0	0	0	SIP BEtag							
05	SIP BAsize															
06	SIP DA															
07																
08																
09																
10	SA															
11																
12																
13																
14	High Layer Protocol				Pad 1		QOS				CI	HE Len				
15	Bridging															
16	Header Extension															
17																
18																
19																
20																
21																
22	Information															
23																
24																
25																
26	PL Len.						CRC									

FIG. 625

669360 612260

SIP COM CELL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	DC															
01	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID	PT			CLP		
03	0	0	SN				0	0	0	MID						
04	Information															
05																
06																
07																
08																
09																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
23																
24																
25																
26	PL Len.						CRC									

FIG. 627

SIP EOM(Inter-MH EOM) CELL

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

00	DC																
01	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
02	0	0	1	1	0	0	0	0	0	Link ID		PT		CLP			
03	0	1	SN				0		0	0	MID						
04	Information																
05																	
06																	
07																	
08																	
09																	
10																	
11																	
12																	
13																	
14																	
15																	
16																	
17																	
2N	Reserved									BEtag							
2N+1	Length(ISSIP)																
2N+2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	PL Len.							CRC									

FIG. 628

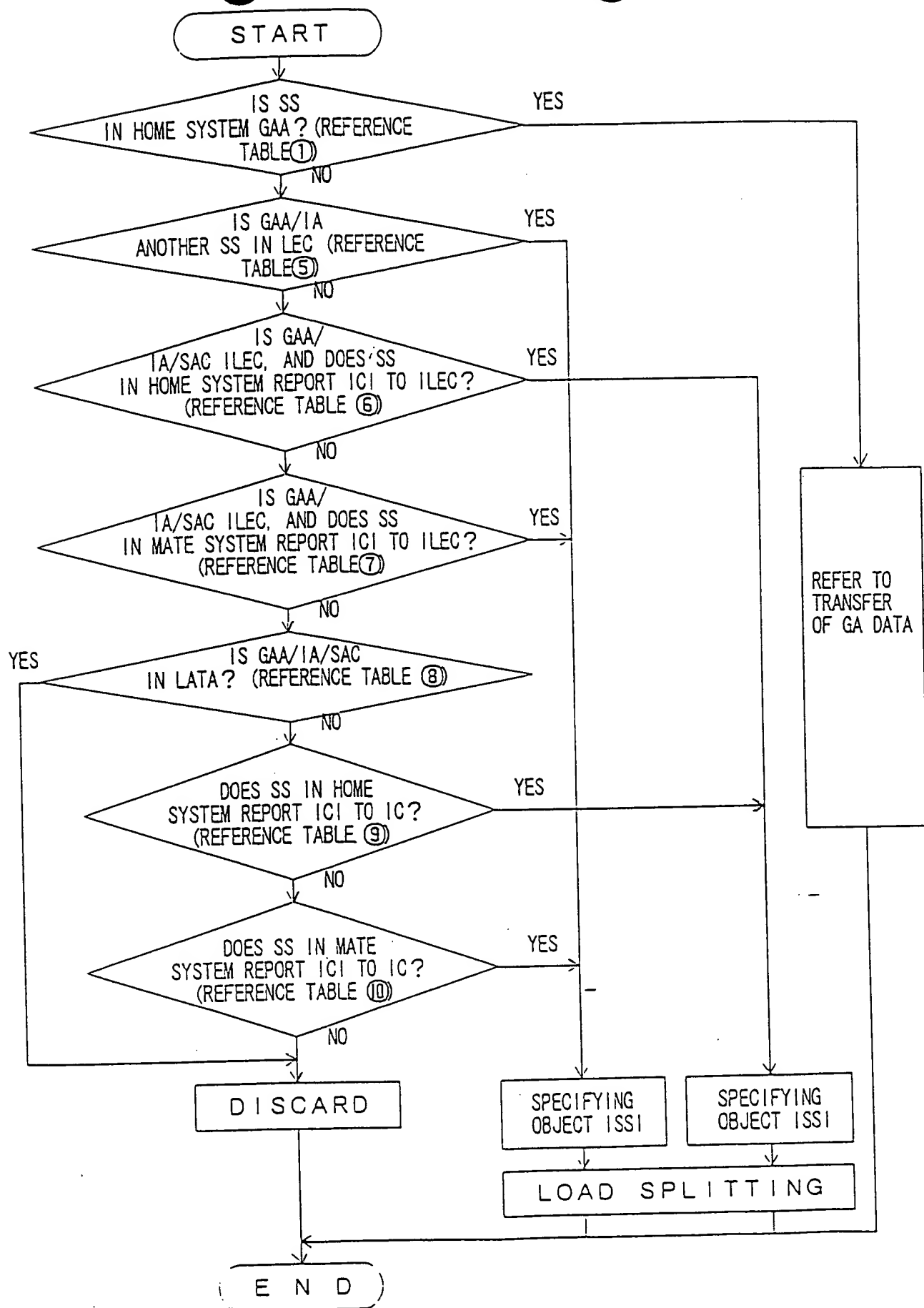


FIG. 629

- ① DETERMINING WHETHER OR NOT SS IN HOME SYSTEM "GAA" ACCORDING TO GAA LIST.

	GAA (64 bit)	GA ID (10 bit)
1024 (W)

- ② COPYING WHILE ASSIGNING GA-SUPPORTED IA, ISSI/ICI No., GA MEMBER ID, AND FLAG FOR OUTSIDE OF LATA.

	GA ID (10bit)	IA (64 bit)	ISSI/ICI No. (3 bit)	GA MEMBER ID (6 bit)	OUTSIDE LATA (1 bit)
1024 (W)

- ③ ASSIGNING CARRIER BY REFERRING TO TABLE BELOW WHEN OUTSIDE-OF-LATA FLAG IS SET AFTER VOPYING GA.

	SMDS CIC(16 bit)	ISSI/ICI No. (3bit)
256 (W)

- ④ DETERMINING WHETHER OR NOT SPECIFIED LINK IS SUPPORTED BY MESH OF HOME SYSTEM ACCORDING TO TABLE BELOW.

	ISSI/ICI No. (3 bit)	GA MEMBER ID (6 bit)	LINK (3 bit)
256 (W)

FIG. 631

- ⑤ IT IS DETERMINED ACCORDING TO THE GAA/IA STATION NUMBER IN THE LEC WHETHER OR NOT GAA/IA IS ANOTHER SS IN THE LEC.

INSIDE LEC GAA STATION NUMBER (32bit)	ISSI No. (3bit)
.....
INSIDE LEC IA STATION NUMBER (32bit)	ISSI No. (3bit)
.....

- ⑥ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LEC WHETHER OR NOT GAA/IA/SAC REFERS TO THE ILEC AND THE ICI TO THE ILEC IS SUPPORTED BY THE SS IN THE HOME SYSTEM.

INSIDE ILEC GAA STATION NUMBER (32bit)	ICI No. (3bit)
.....
INSIDE ILEC IA STATION NUMBER (32bit)	ICI No. (3bit)
.....
INSIDE ILEC SAC STATION NUMBER (32bit)	ICI No. (3bit)
.....

TOTAL STATION
NUMBER
OF TABLES
⑤-⑧ IS 512

- ⑦ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LEC WHETHER OR NOT GAA/IA/SAC REFERS TO THE ILEC AND THE ICI TO THE ILEC IS SUPPORTED BY THE SS IN THE MATE SYSTEM.

INSIDE ILEC GAA STATION NUMBER (32bit)	ISSI No. (3bit)
.....
INSIDE ILEC IA STATION NUMBER (32bit)	ISSI No. (3bit)
.....
INSIDE ILEC SAC STATION NUMBER (32bit)	ISSI No. (3bit)
.....

- ⑧ IT IS DETERMINED ACCORDING TO THE GAA/IA/SAC STATION NUMBER IN THE LATA WHETHER OR NOT STATION NUMBER OF LATA IS REFERRED TO.

INSIDE LATA GAA STATION NUMBER (32bit)
.....
INSIDE LATA IA STATION NUMBER (32bit)
.....
INSIDE LATA SAG STATION NUMBER (32bit)
.....

FIG. 632

⑨ IT IS DETERMINED WHETHER OR NOT ICI FROM SMDS CIC TO IC
IS SUPPORTED BY SS OF HOME SYSTEM.

SMDS CIC (16BIT)	ICI No. (3 BIT)
.....

⑩ IT IS DETERMINED WHETHER OR NOT ICI FROM SMDS CIC TO IC
IS SUPPORTED BY SS OF MATE SYSTEM.

SMDS CIC (16BIT)	ISSI No. (3 BIT)
.....



A TOTAL OF 256 CARRIERS ARE
SPECIFIED FOR ⑫ AND ⑬

FIG. 633

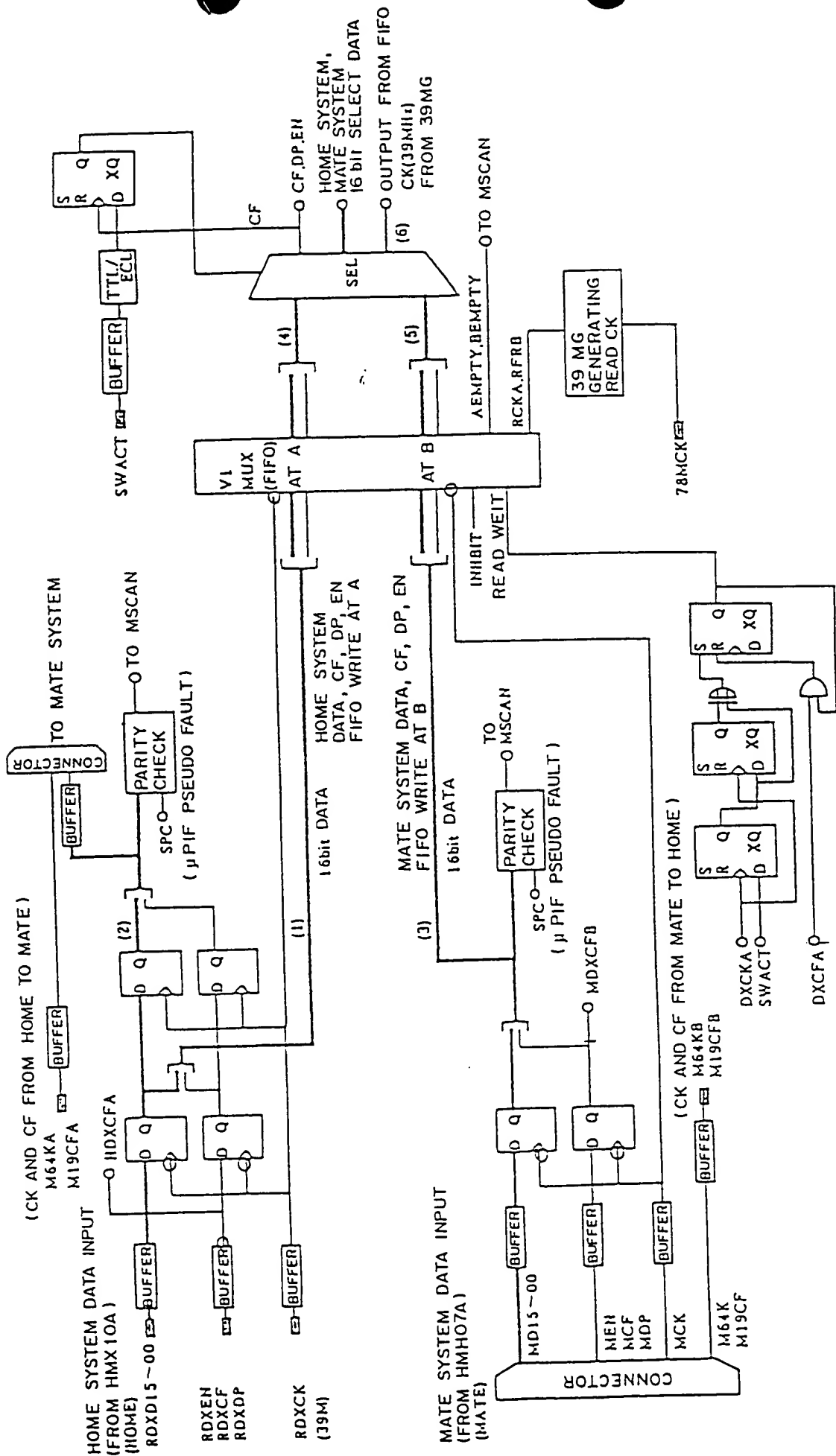


FIG. 634

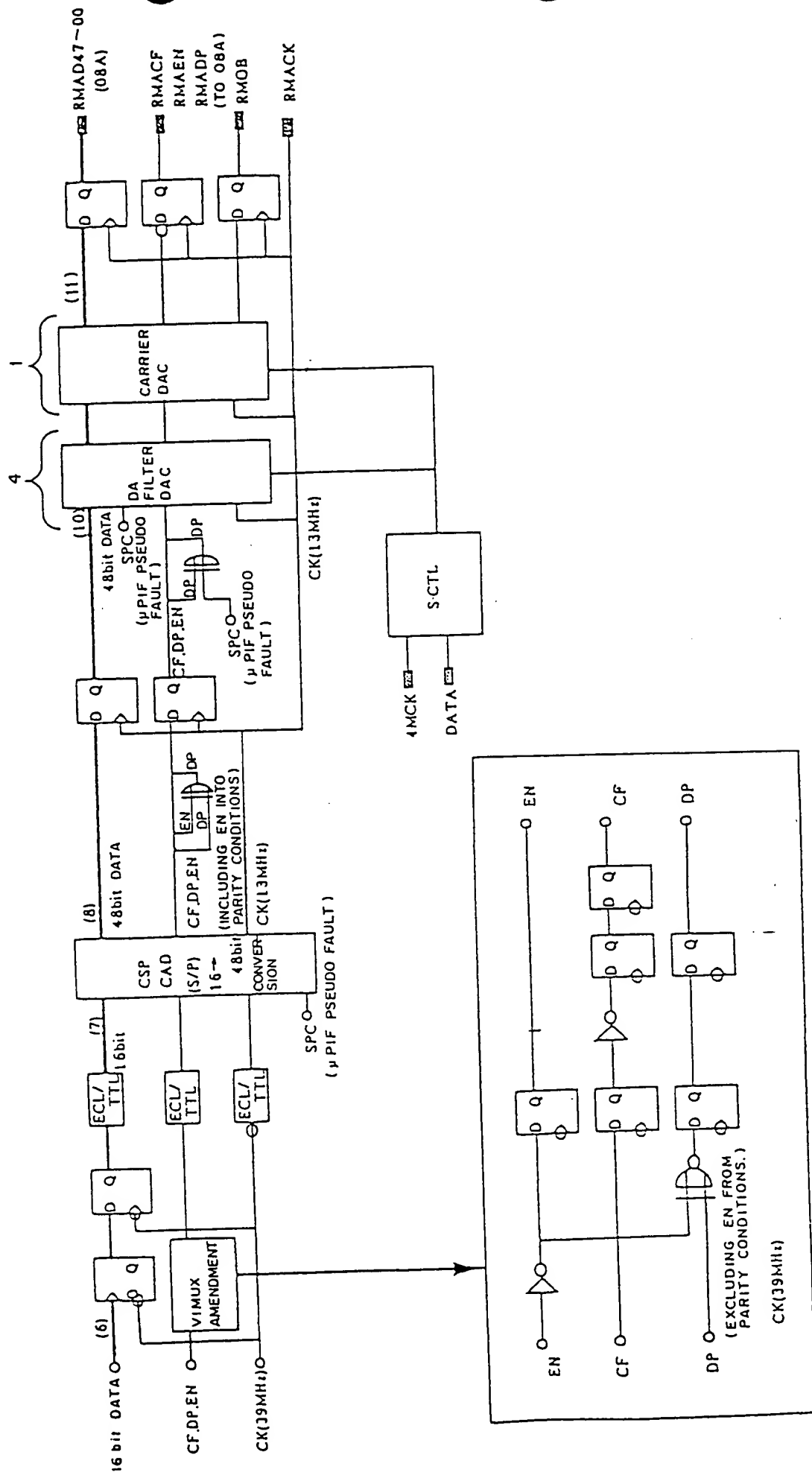
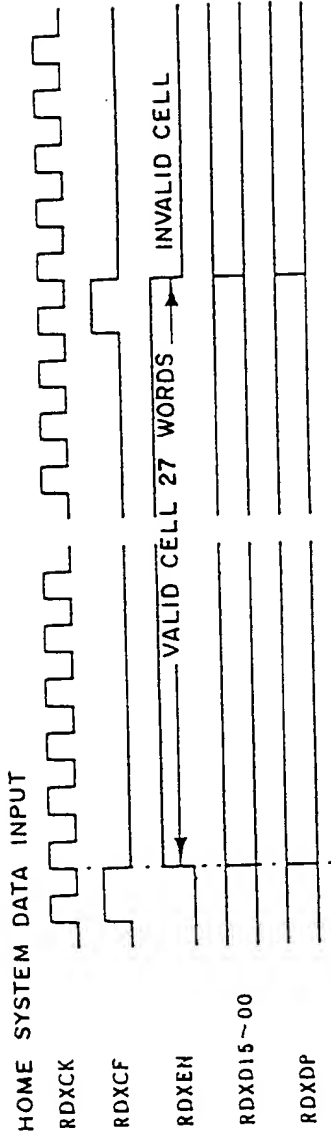
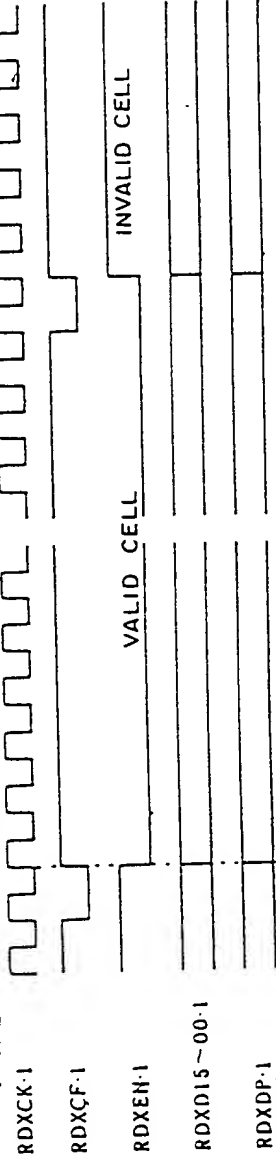


FIG. 635



(1) HOME SYSTEM DATA (CF, EN, AND DP ARE INVERTED IN THE INPUT BUFFER) IS PROCESSED BY INVERTING THE RDXCK AND FETCHED TO THE VIMUX (FIFO) USING THE CK.

X THE VIMUX FETCHES DATA AT THE FALL OF CK.



(2) (1) DATA IS PROCESSED BY THE RDXCK, PARITY-CHECKED, AND PASSED TO A MATE SYSTEM

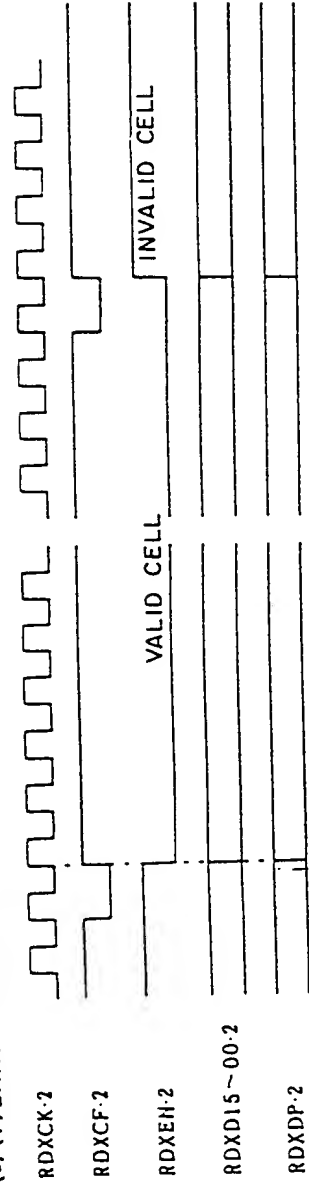


FIG. 636

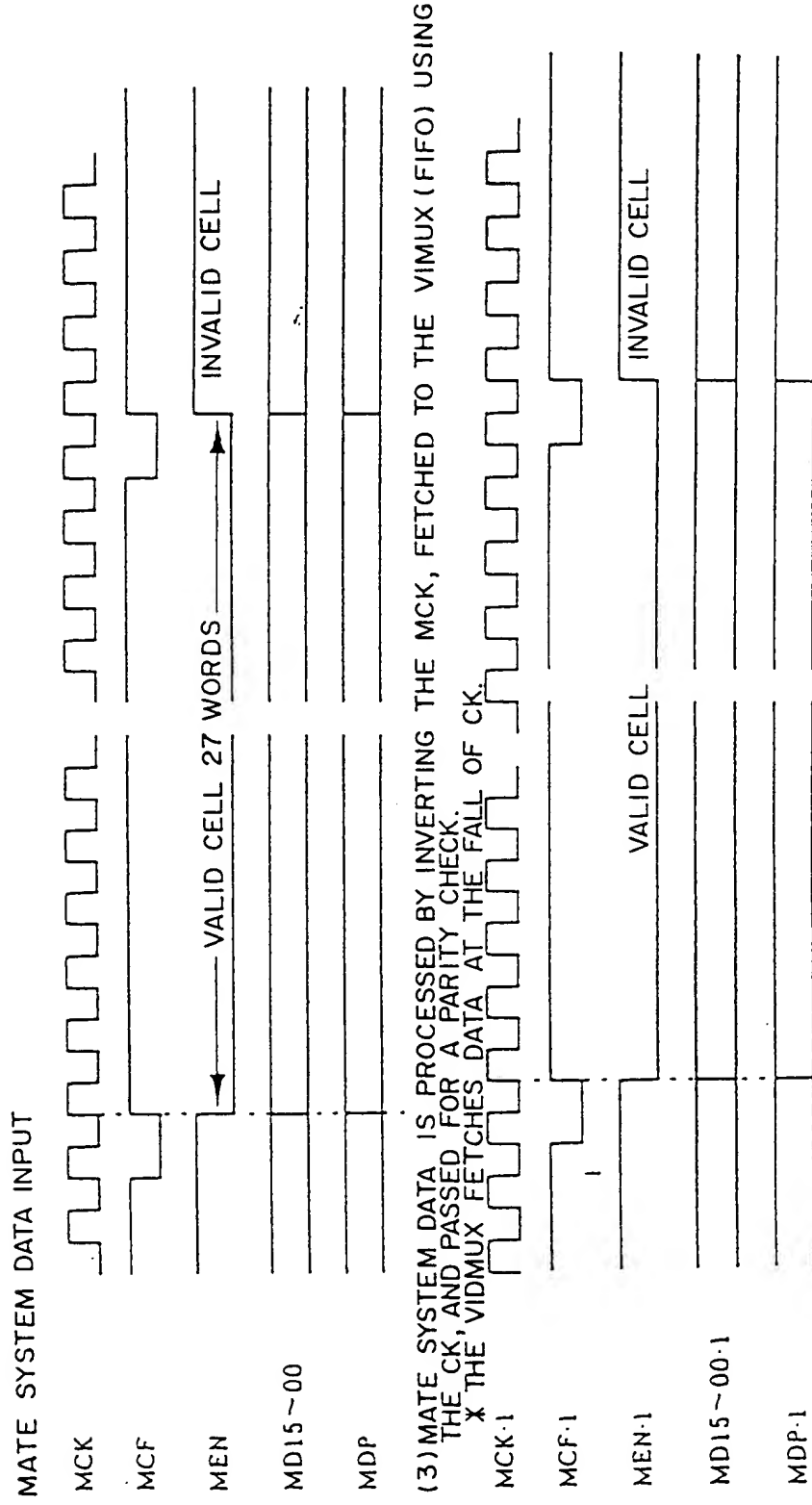
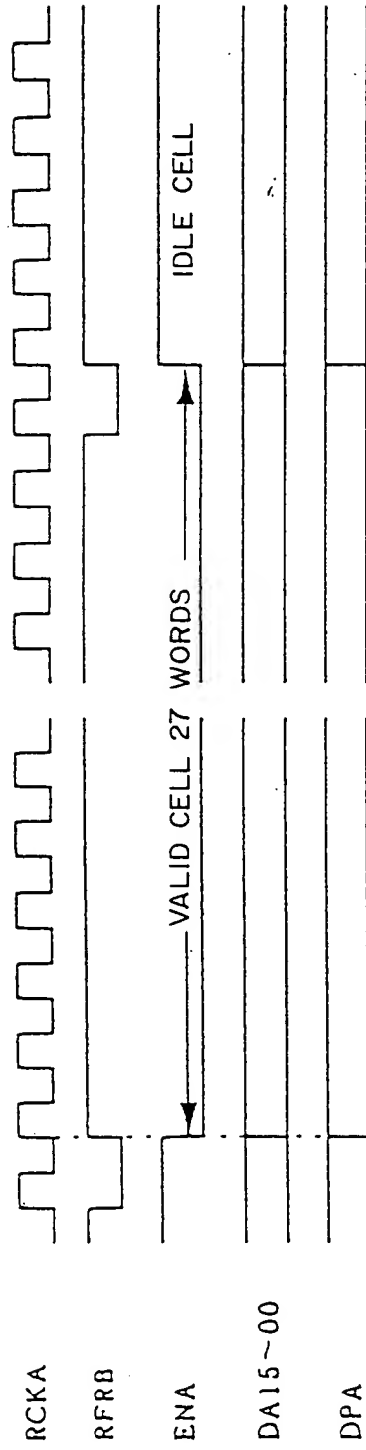


FIG. 637

(4) HOME SYSTEM DATA FIFO (VIMUX) READ AT A



(5) MATE SYSTEM DATA FIFO (VIMUX) READ AT B

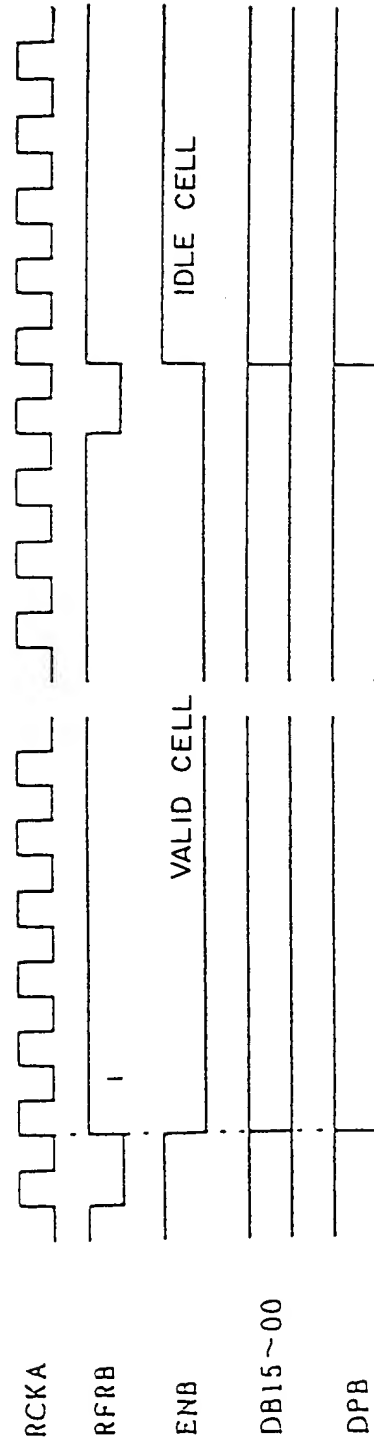
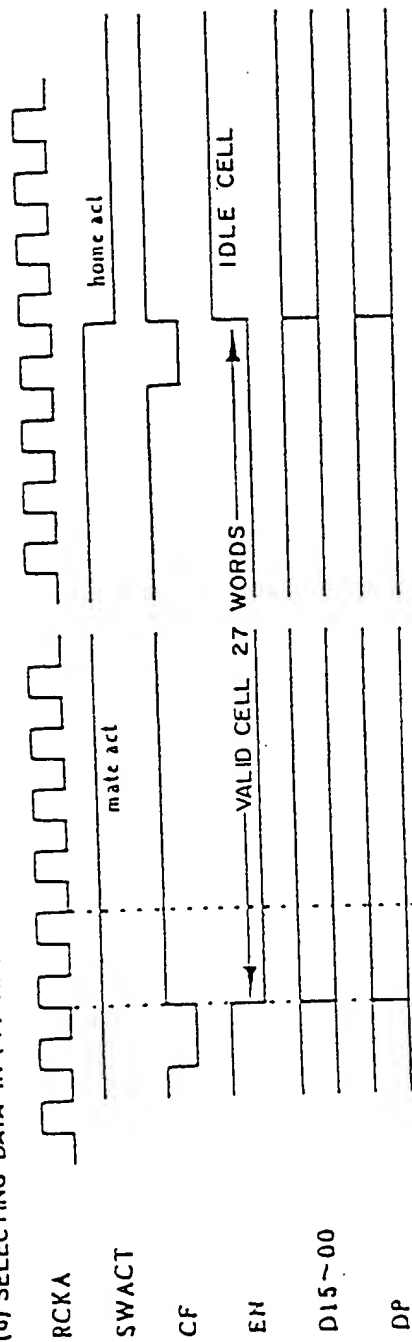
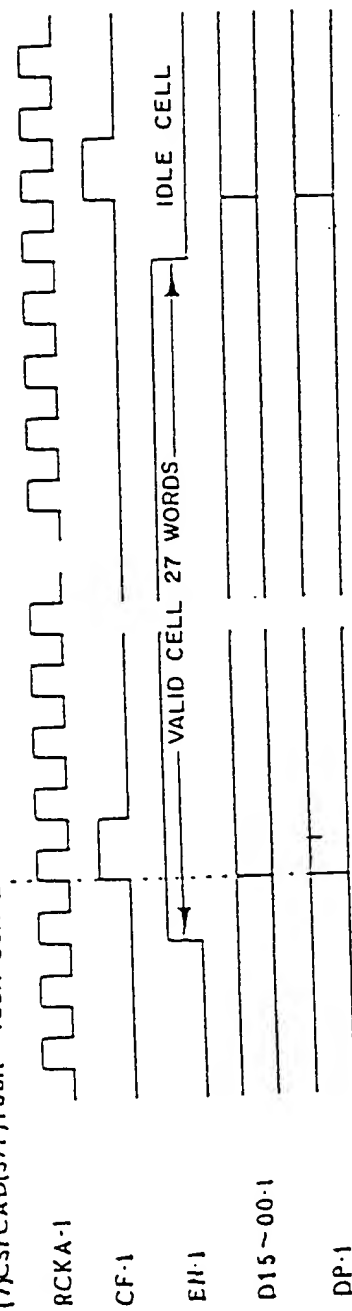


FIG. 638

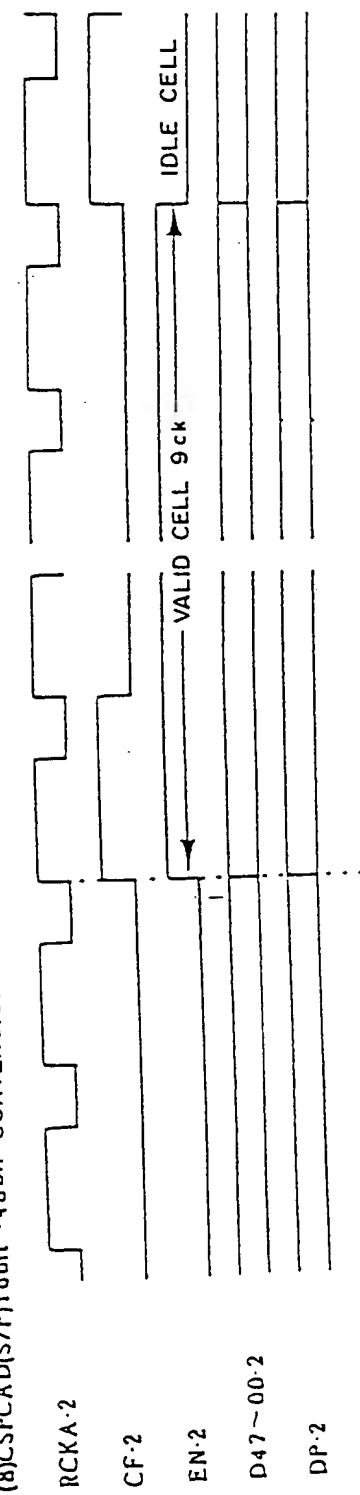
(6) SELECTING DATA IN (4) AND (5) THROUGH SWACT



(7) CSPCAD(S/P) 16bit → 48bit CONVERSION INPUT DATA



(8) CSPCAD(S/P) 16bit → 48bit CONVERSION OUTPUT DATA



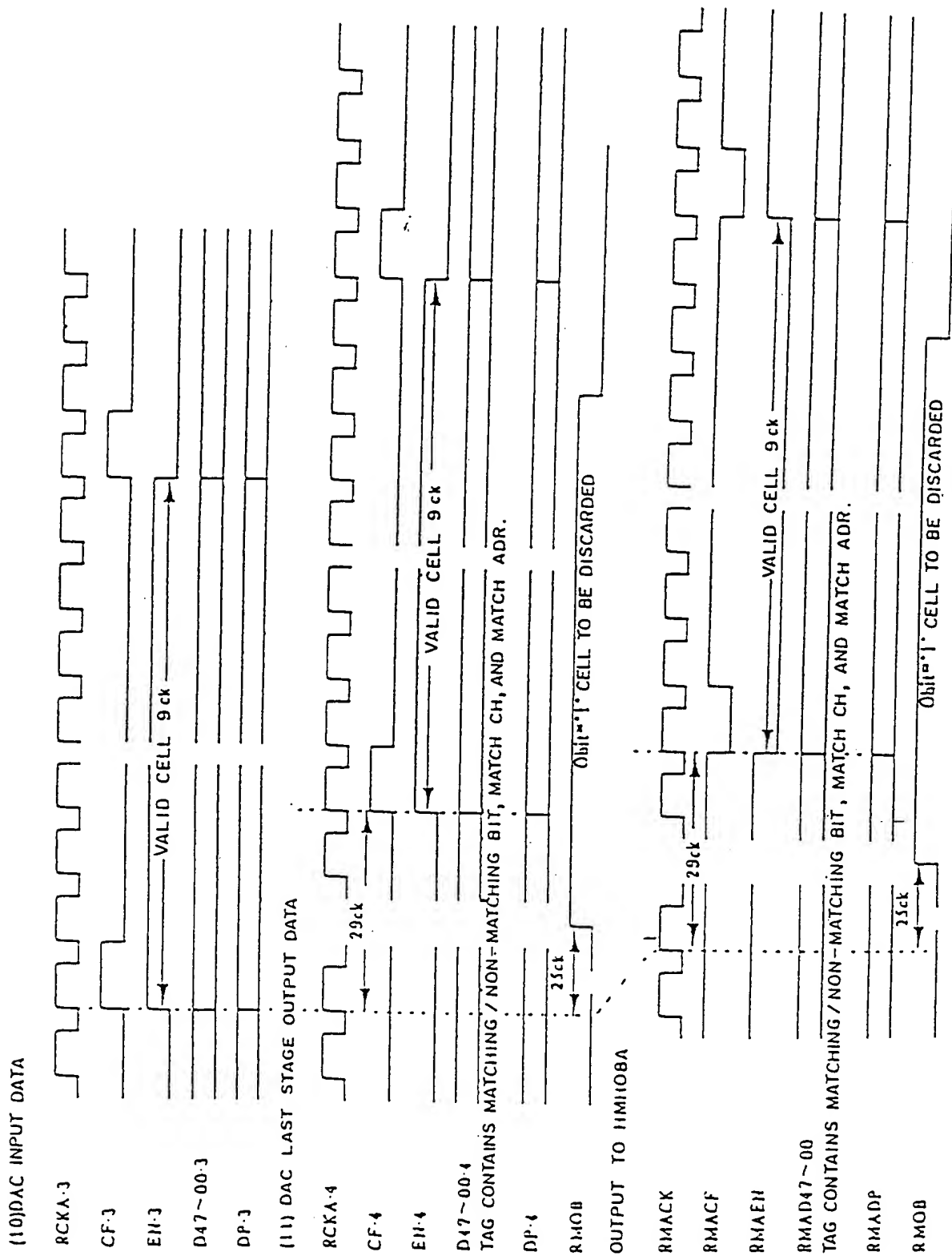


FIG. 640

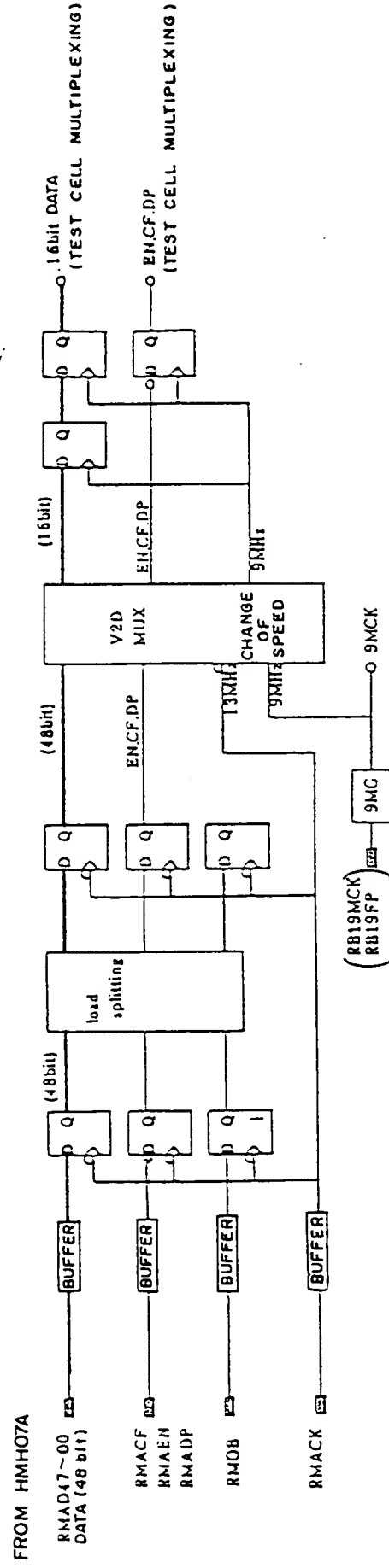


FIG. 641

Year	Age	Gender	Height (cm)	Weight (kg)	Body Fat (%)	VO ₂ max (ml/min)	VO ₂ max (ml/kg/min)	VO ₂ max (l/min)	VO ₂ max (l/kg/min)
1998	21	M	178	75	12	3.8	21.3	68.0	3.8
2000	23	M	180	78	13	4.0	22.2	71.0	4.0
2002	25	M	182	80	14	4.2	23.1	74.0	4.2
2004	27	M	184	82	15	4.4	24.0	77.0	4.4
2006	29	M	186	84	16	4.6	24.9	80.0	4.6
2008	31	M	188	86	17	4.8	25.8	83.0	4.8
2010	33	M	190	88	18	5.0	26.7	86.0	5.0
2012	35	M	192	90	19	5.2	27.6	89.0	5.2
2014	37	M	194	92	20	5.4	28.5	92.0	5.4
2016	39	M	196	94	21	5.6	29.4	95.0	5.6
2018	41	M	198	96	22	5.8	30.3	98.0	5.8
2020	43	M	200	98	23	6.0	31.2	101.0	6.0

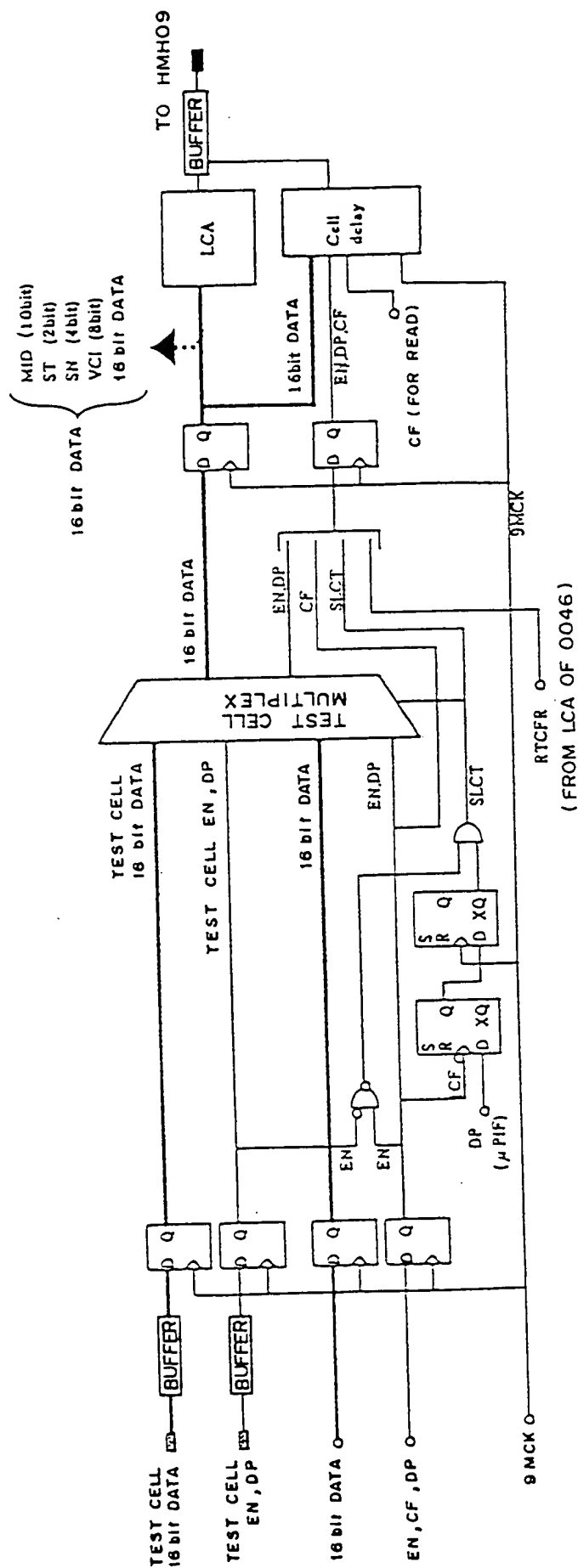


FIG. 642

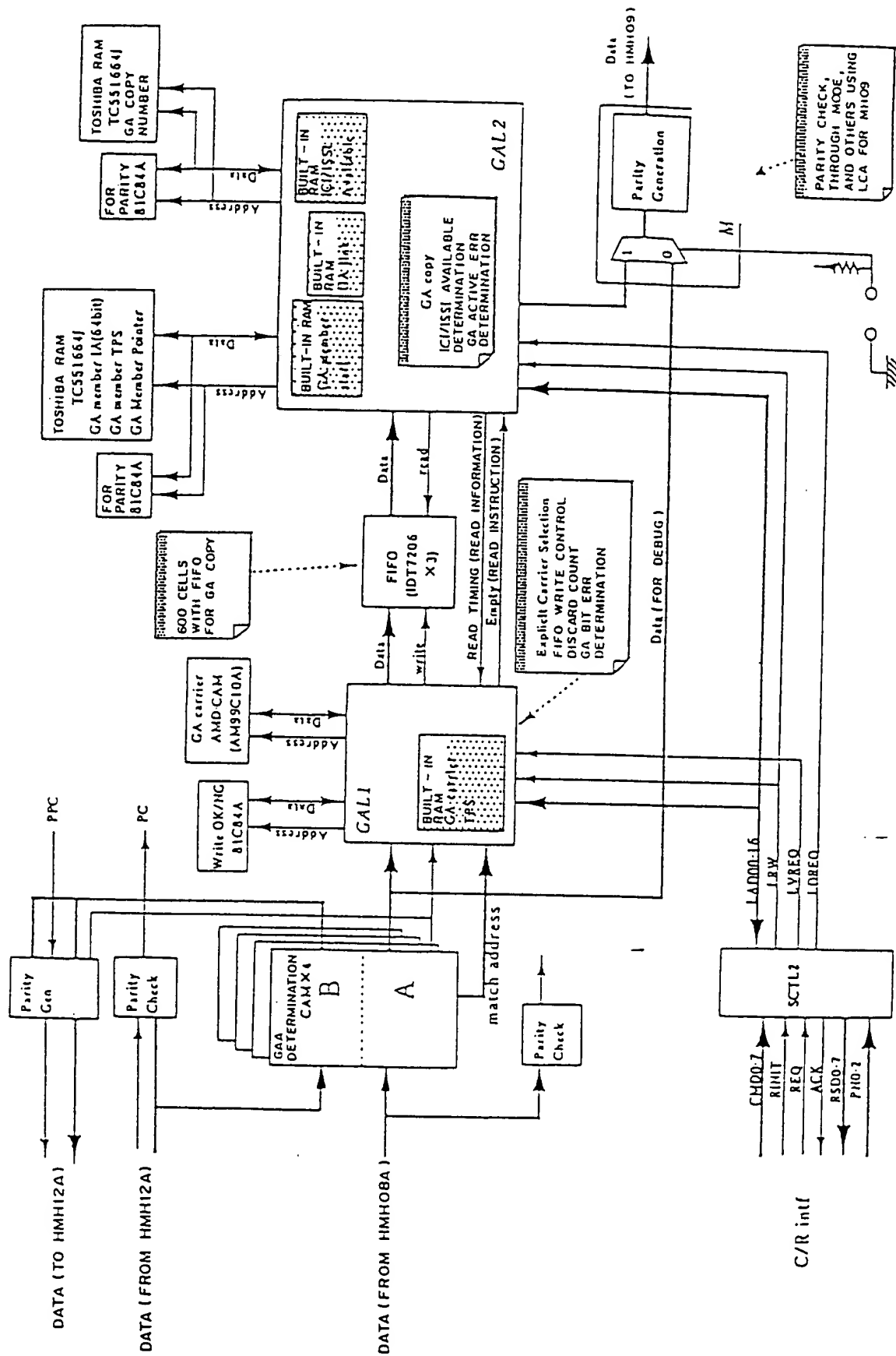


FIG. 643

0000000000000000

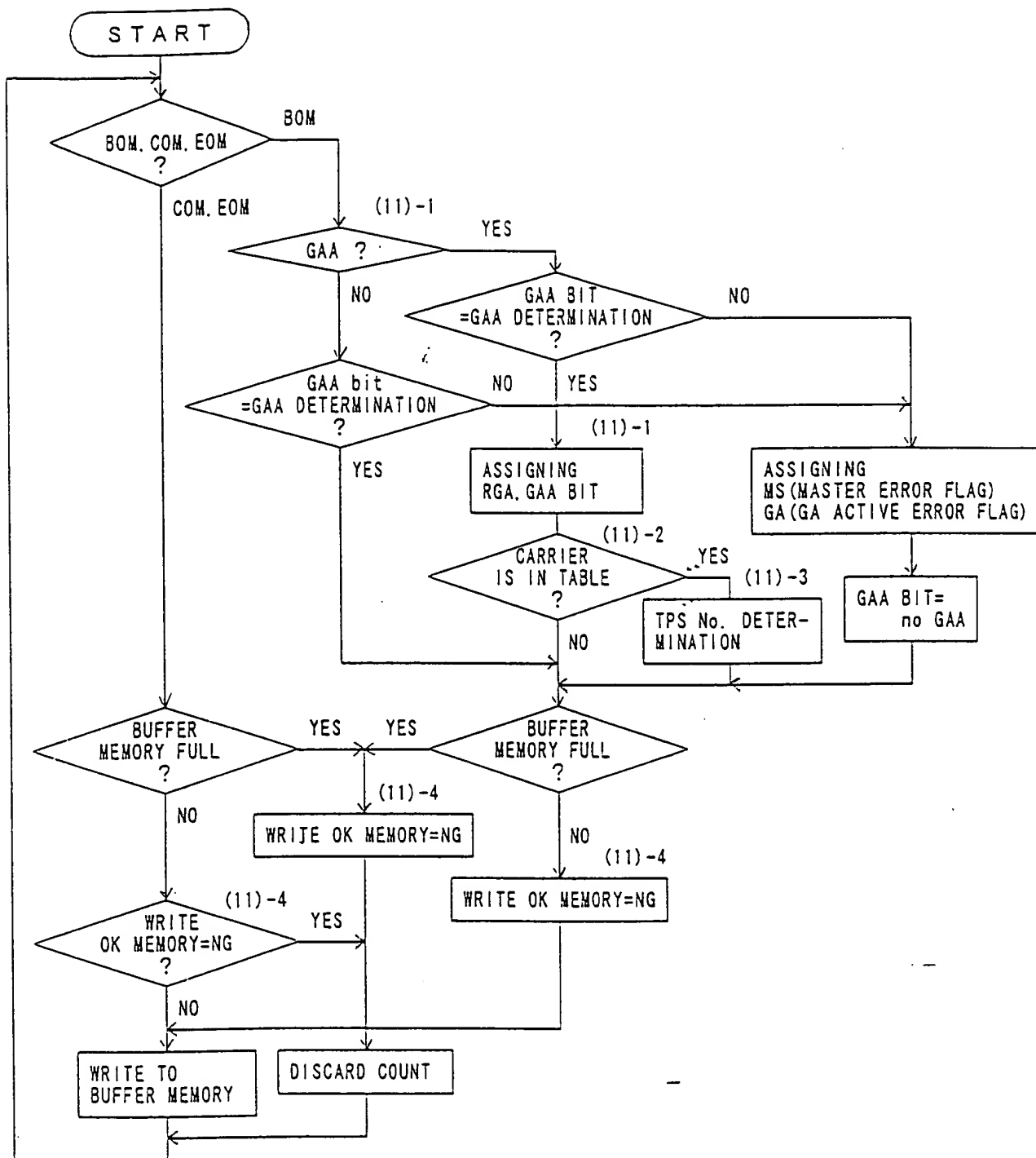


FIG. 644

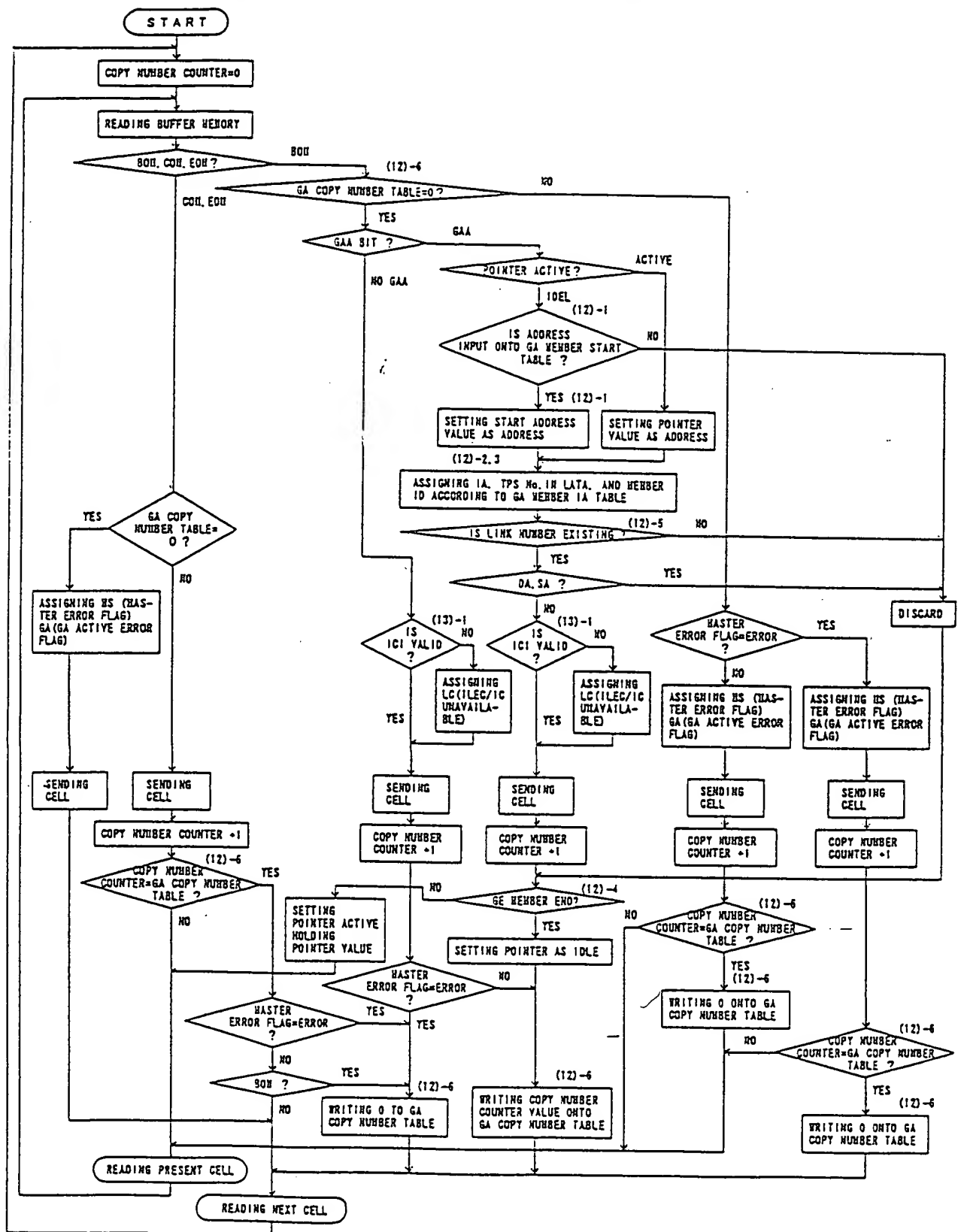


FIG. 645

ITEM	FUNCTION	REMARKS
1	PARITY CHECK	PERFORMING PARITY CHECK ON DATA AND ENABLE.
2	MRI TIMEOUT	DETERMINING MRI TIMEOUT OF MESSAGE
3	MID CONVERSION	CONVERTING INPUT MID TO VCI AND MID OF OUTPUT LINK
4	CELL DELAY	TIME DELAY REQUIRED FOR TIMEOUT PROCESS AND MID CONVERSION PROCESS.
5	ERROR CELL DISCARD	RECEIVING ERROR FLAG AND DISCARDING CELL.
6	OUTPUT BAND LIMIT	LIMITING OUTPUT BAND BASED ON LIMITED BAND.
7	FORMAT CONVERSION	CONVERTING CELL FORMAT INTO ISSI OR ICI FORMAT.
8	GENERATING AND ASSIGNING CRC-10	PERFORMING CRC-10 OPERATION ON PAYLOAD EXCLUDING HEADER AND ASSIGNING OPERATION RESULT.
9	DISCARD COUNTER	RECEIVING DISCARDED CELLS FROM HMH08A, HMH09A, AND VC-SH II, COUNTING THEM, AND PASSING THEM TO LP-COM.
10	C/R UNIT	RECEIVING COMMANDS FROM HLP07A BY SCTL2 LSI, AND RETURNING RESPONSE.
11	MSCN, MSD UNIT	RECEIVING VARIOUS CONTROL SIGNALS AND DATA FROM μP UNIT AND CONTROLLING INTERNAL UNITS.
12	CLK Gen.	GENERATING 9.72 MHz CLOCK FROM 19.44 MHz CLOCK AND FRAME PULSE.

FIG. 647

669220-6 669220

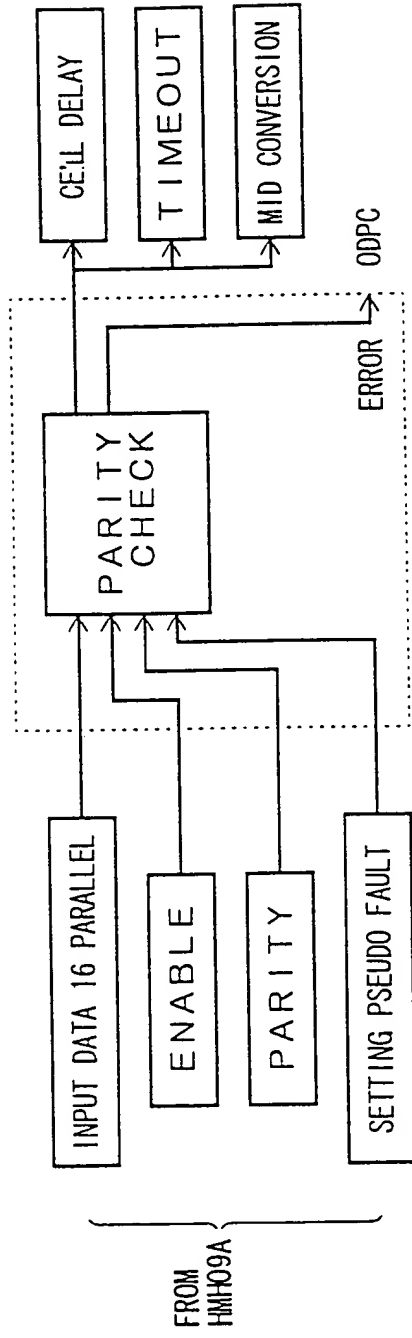


FIG. 648

66960-64260

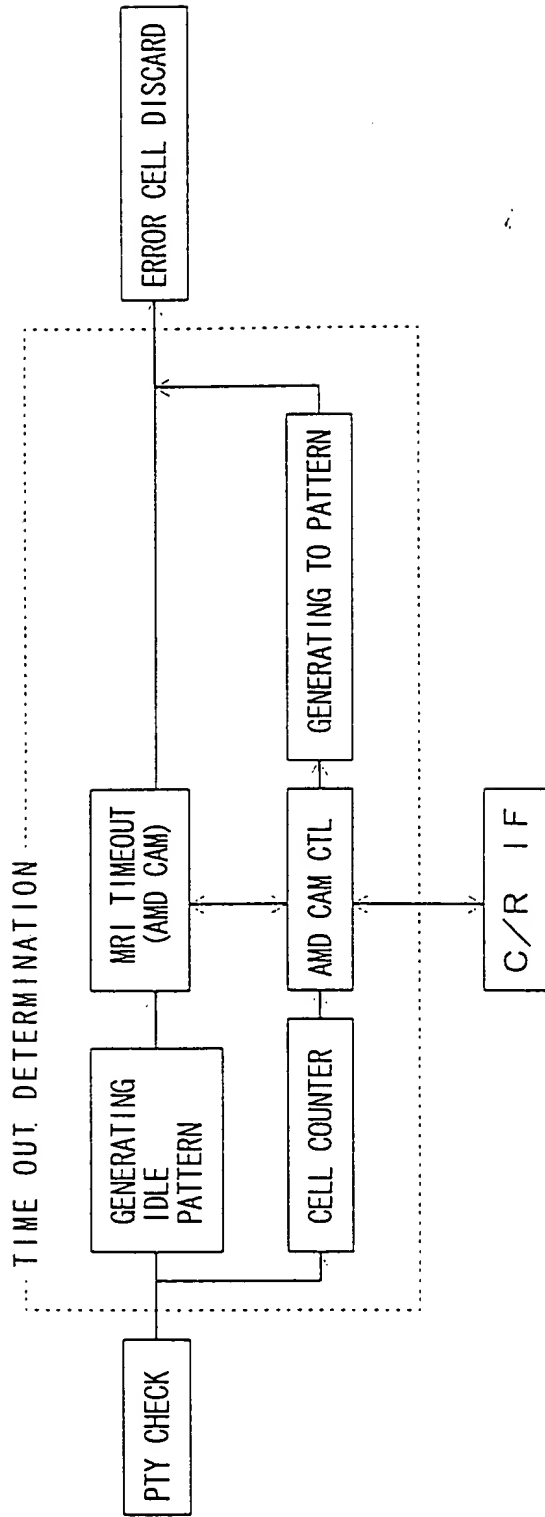


FIG. 649

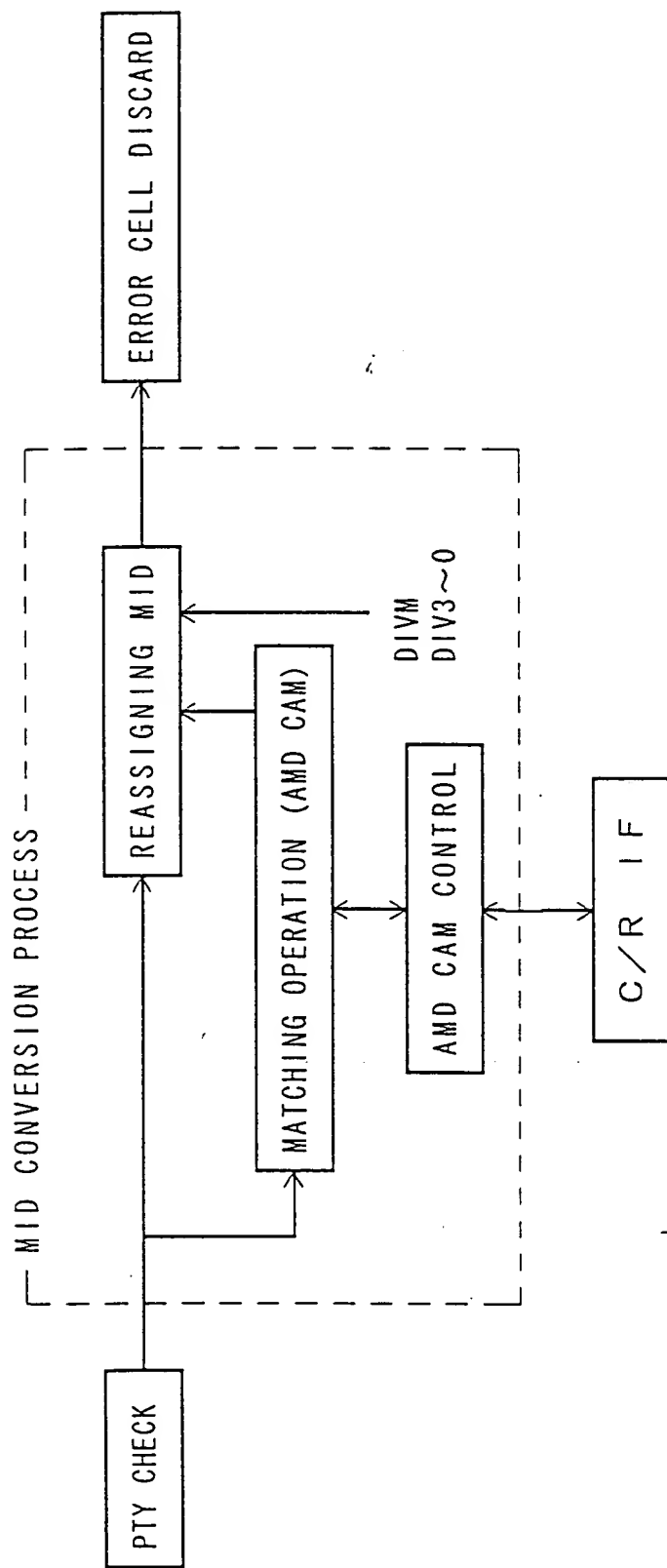


FIG. 650

66960* 6124260

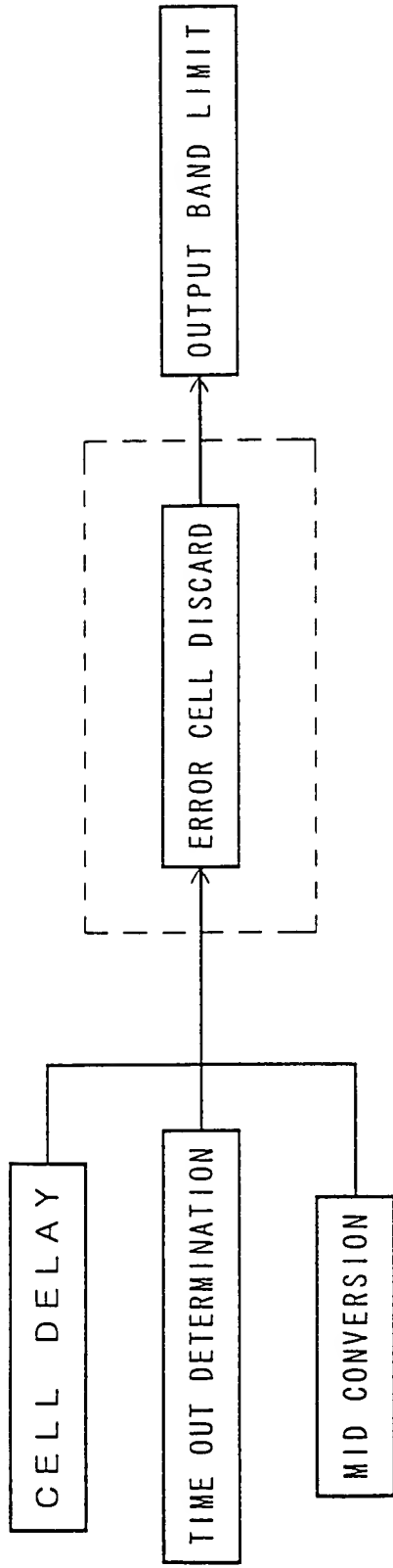


FIG. 652

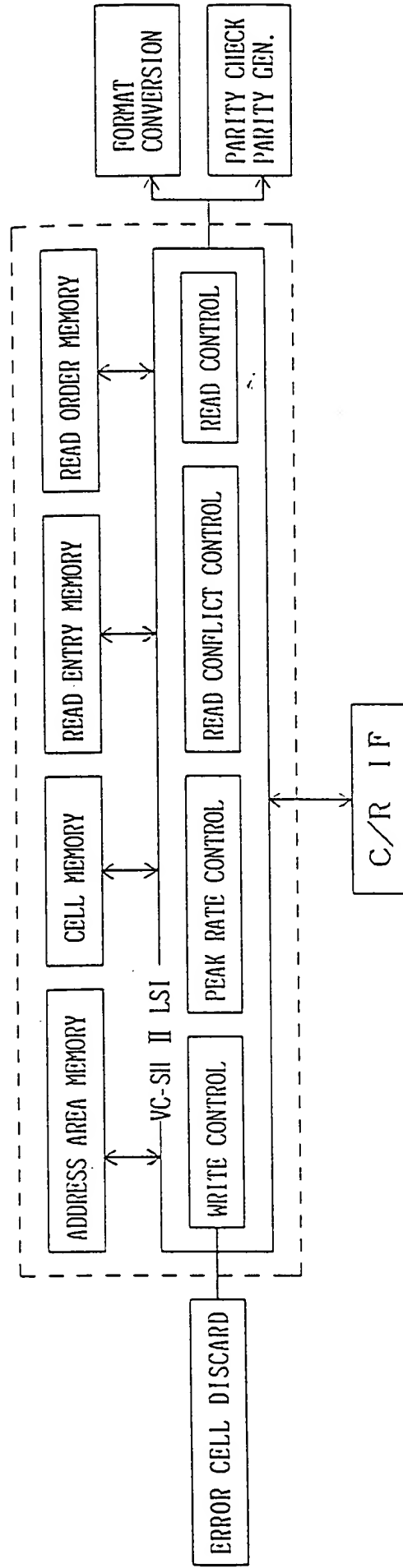
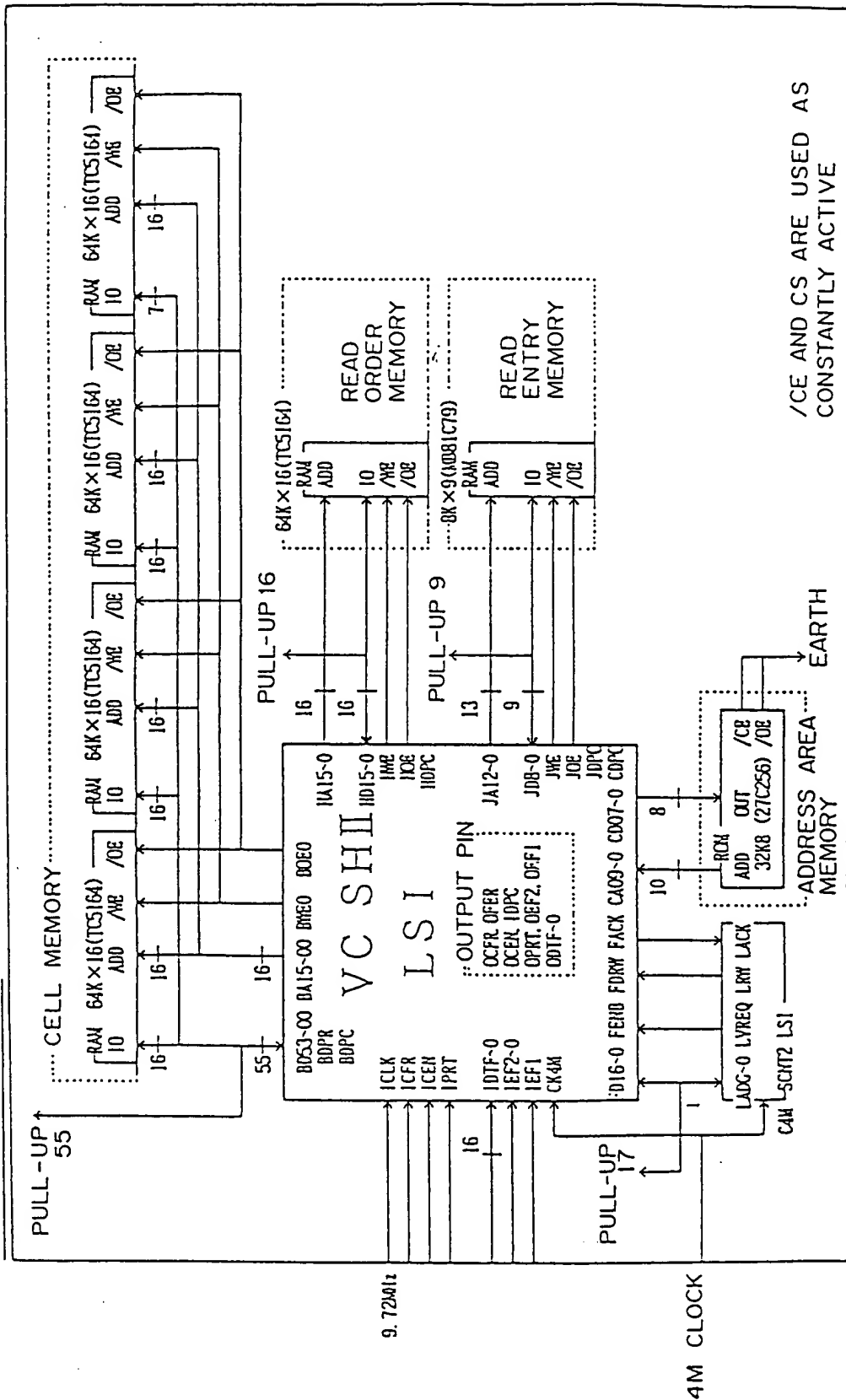


FIG. 653

669220-6122260

OUTPUT BAND LIMIT (CONNECTION TO VC-SH LSI)



GROUPING INTO VC-SH BLOCKS (IN PKG)

0 INPUT DATA AND OUTPUT DATA

1 CELL MEMORY ADDRESS, /WE, /OE

2-4 CELL MEMORY DATA AND ERROR FLAG

5 ADDRESS AREA MEMORY

6 READ ORDER MEMORY AND READ ENTRY MEMORY

7 SCNT 2 DATA AND CONTROL

8 PARITY CHECK, RESET, CONTROL
9 SCAN PIN, TEST MONITOR OUTPUT
(NOT SHOWN IN BLOCK DIAGRAM ABOVE)

FIG. 654

66360-62260

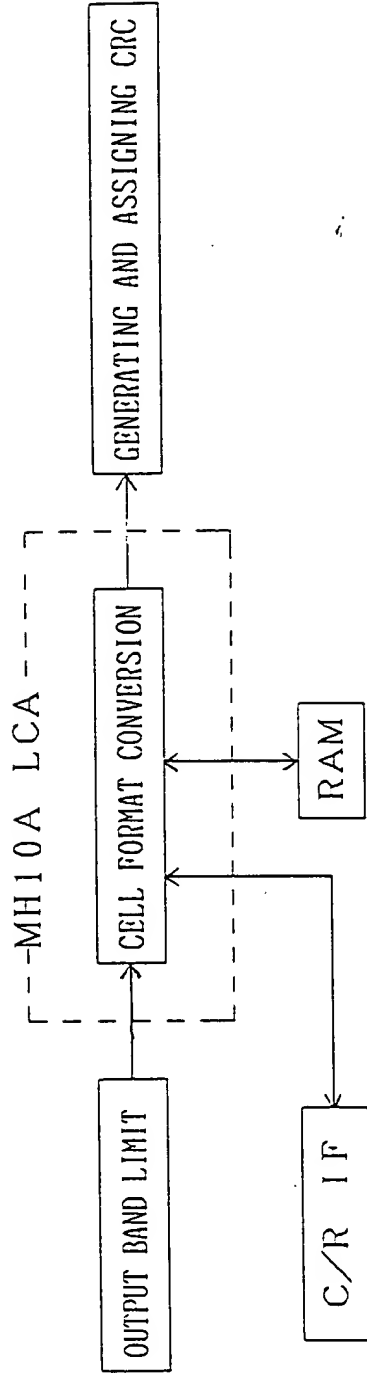
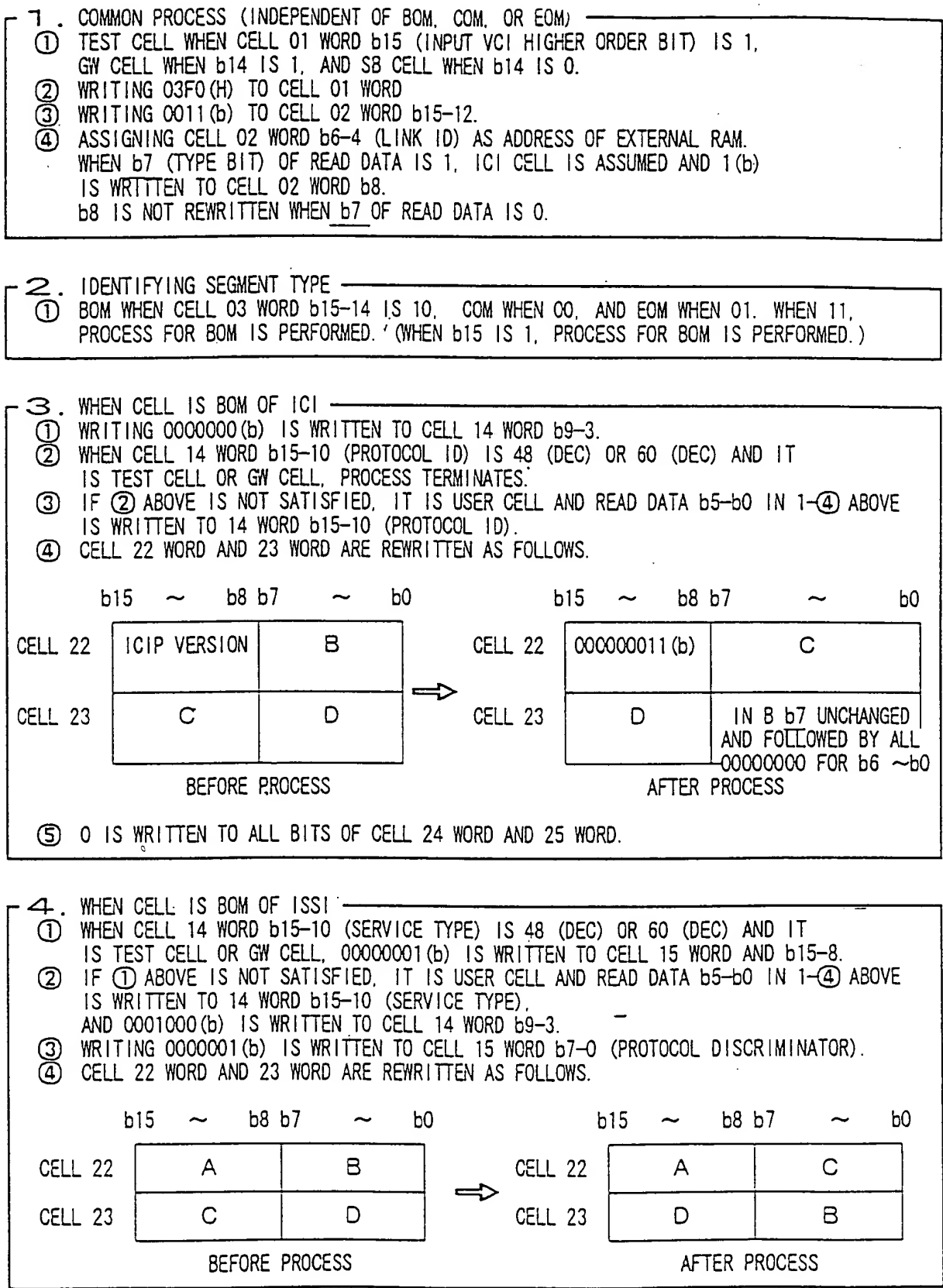


FIG. 655

66960 6 1 2 2 6 0


4. WHEN CELL IS BOM OF ISSI

- ① WHEN CELL 14 WORD b15-10 (SERVICE TYPE) IS 48 (DEC) OR 60 (DEC) AND IT IS TEST CELL OR GW CELL, 00000001(b) IS WRITTEN TO CELL 15 WORD AND b15-8.
- ② IF ① ABOVE IS NOT SATISFIED, IT IS USER CELL AND READ DATA b5-b0 IN 1-④ ABOVE IS WRITTEN TO 14 WORD b15-10 (SERVICE TYPE), AND 0001000(b) IS WRITTEN TO CELL 14 WORD b9-3.
- ③ WRITING 0000001(b) IS WRITTEN TO CELL 15 WORD b7-0 (PROTOCOL DISCRIMINATOR).
- ④ CELL 22 WORD AND 23 WORD ARE REWRITTEN AS FOLLOWS.

b15 ~ b8
b7 ~ b0

CELL 22	A	B
CELL 23	C	D

BEFORE PROCESS

b15 ~ b8
b7 ~ b0

CELL 22	A	C
CELL 23	D	B

AFTER PROCESS

FIG. 656

663660 662260

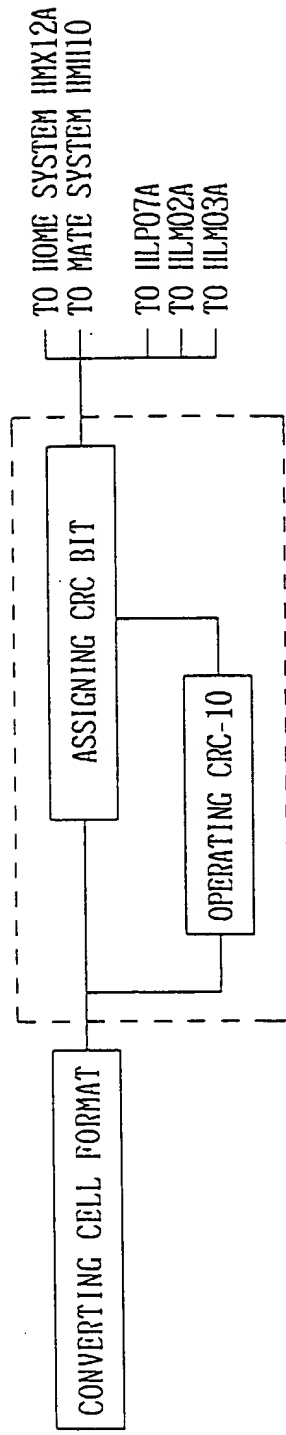


FIG. 657

GENERATION POLYNOMIAL FOR CRC-10 $\Rightarrow X^{10} + X^9 + X^5 + X^4 + X + 1$

OPERATION SCOPE FOR CRC-10
16 BITS

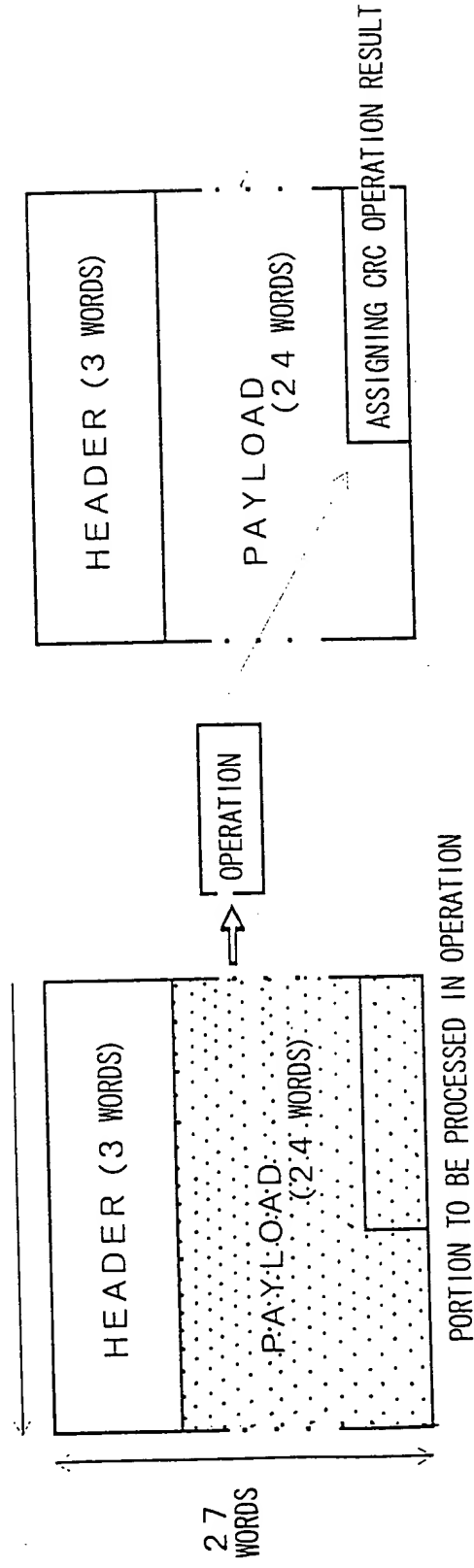


FIG. 658

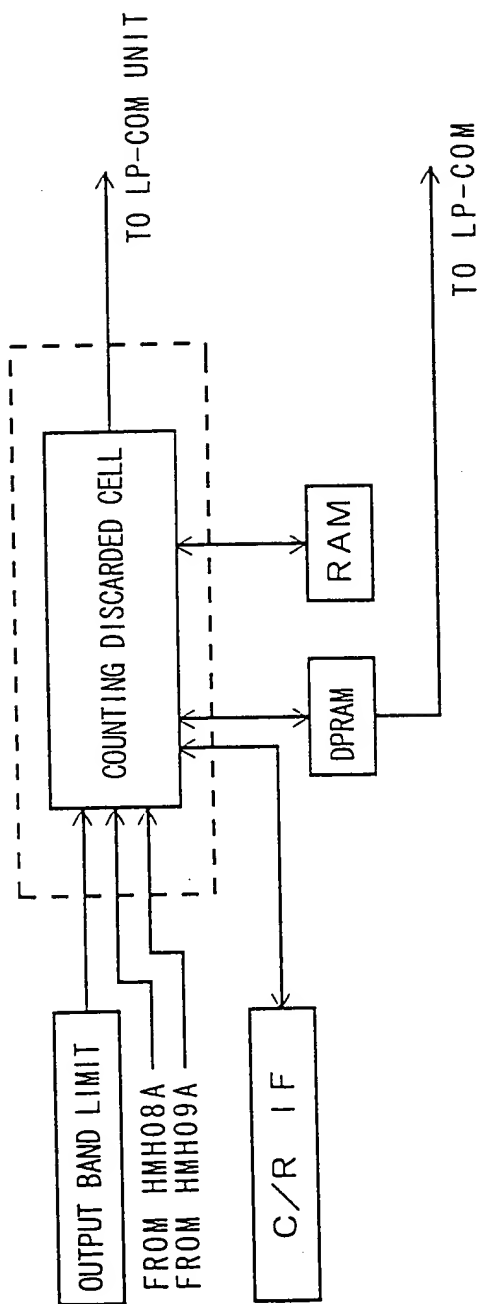


FIG. 659

669260-612260

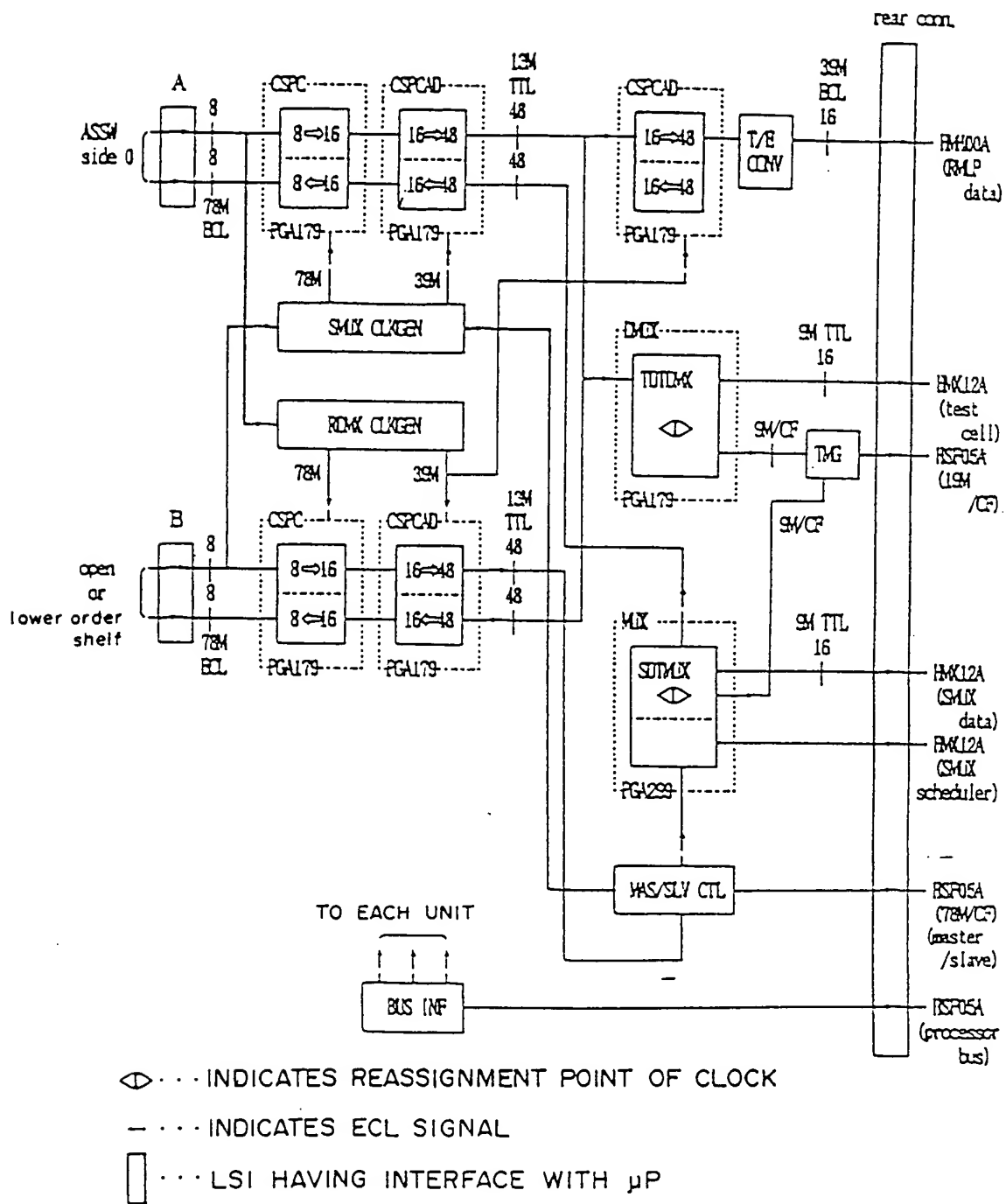


FIG. 660

6660-672000

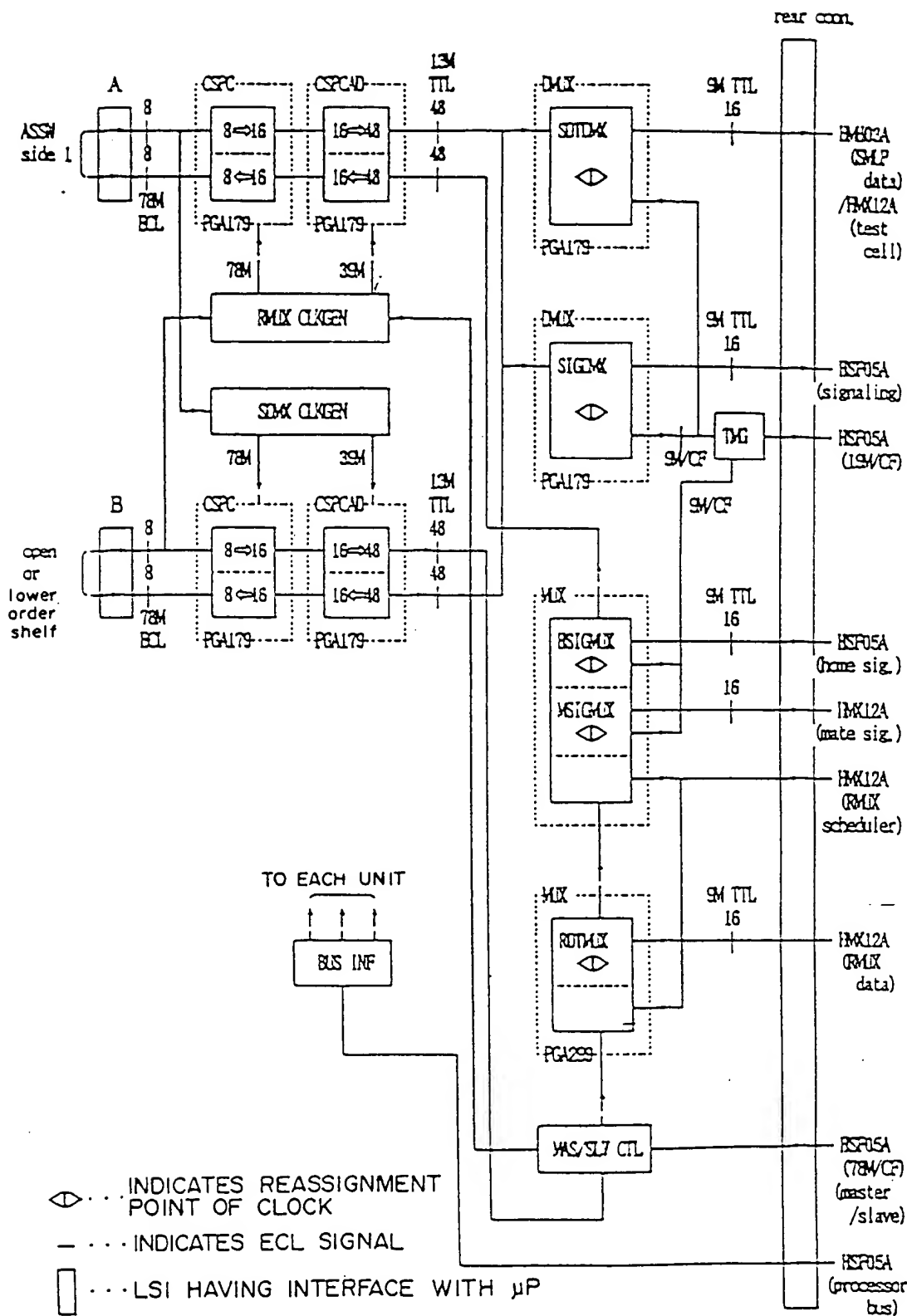


FIG. 661

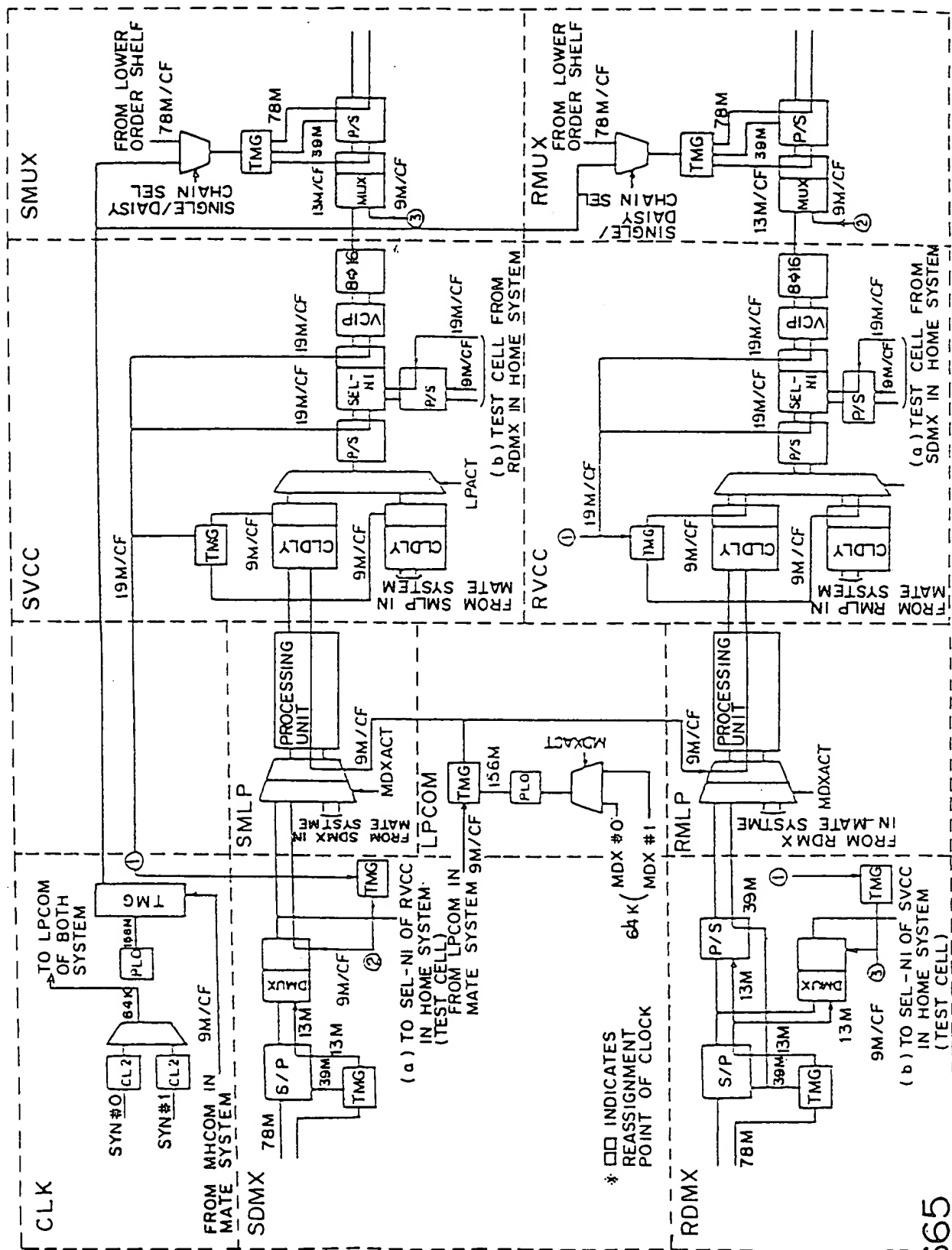


FIG. 665

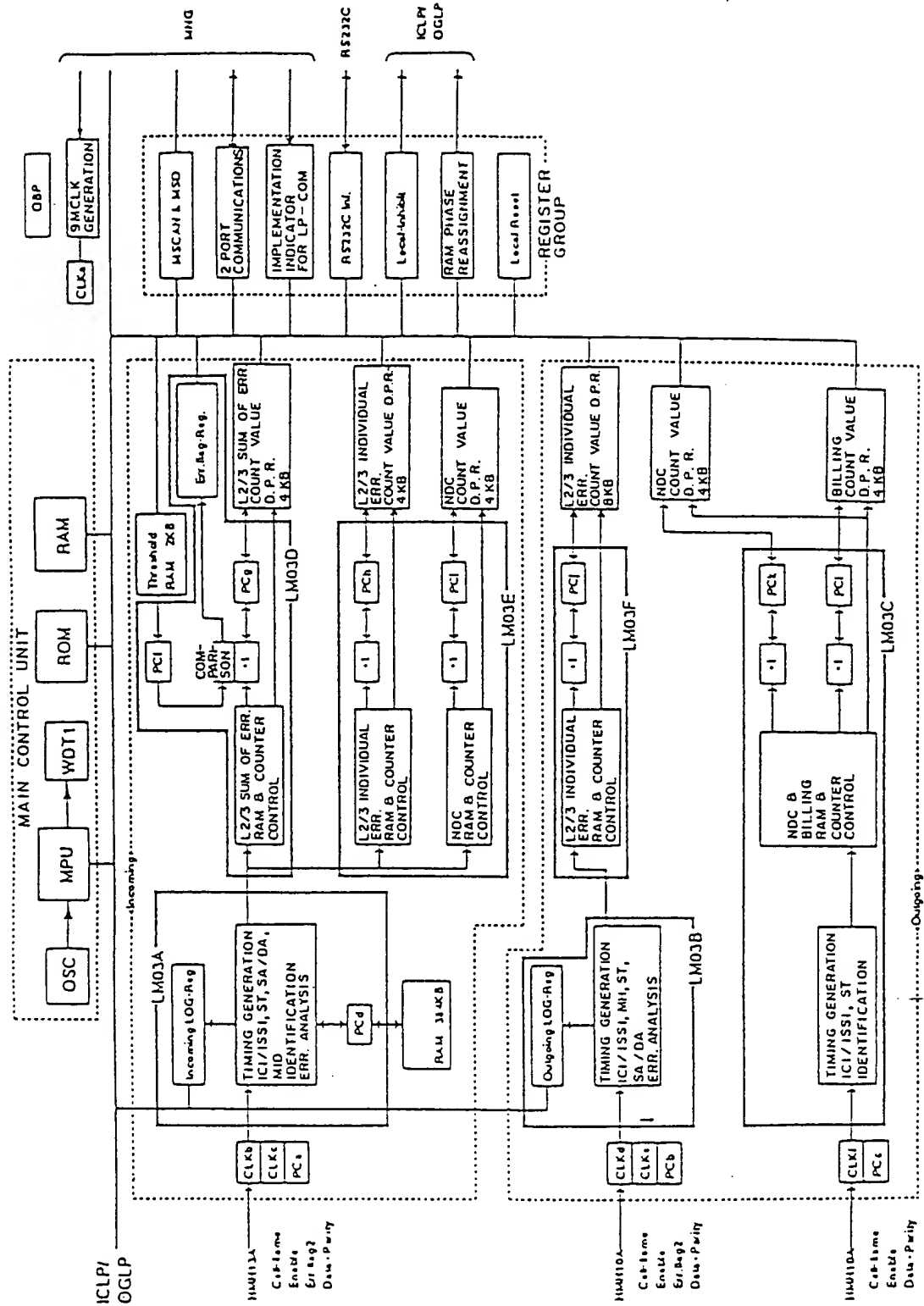


FIG. 666

BLOCK	FUNCTION
INCOMING	COUNTING L2/3 SUM OF ERROR, L2/3 INDIVIDUAL ERROR. NETWORK DATA COLLECTION AT INCOMING TERMINAL.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MFLK, CELL-FRAME (CF), AND ENABLE (EN) SIGNAL.
ICI/ISSI, ST SA/DA, MID IDENTIFICATION	IDENTIFYING SOURCE ICI/ISSI, SEGMENT TYPE, SA/DA, AND MID FROM CELL DATA.
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (EF).
INCOMING LOG-REG.	AREA THROUGH WHICH ERROR TYPE, SOURCE ICI/ISSI, SA, AND DA ARE REPORTED TO FIRMWARE WHEN LOG OBJECT ERROR HAS OCCURRED
SA/DA ACCUMULATION RAM	RAM ACCUMULATING SA AND DA TO COLLECT LOG.
THRESHOLD RAM	SETTING THRESHOLD OF L2/3 SUM OF ERROR AT INITIALIZATION.
L2/3 SUM OF ERR. COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 SUM OF ERROR.
ERR. FLAG-REG.	AREA THROUGH WHICH SUM OF ERROR VALUE EXCEEDING THRESHOLD IS REPORTED TO FIRMWARE.
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR.
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE RELATED TO NETWORK DATA COLLECTION
OUTGOING	COUNTING L2/3 INDIVIDUAL ERROR, NETWORK DATA COLLECTION, AND BILLING PROCESSES AT OUTGOING TERMINAL.
TIMING GENERATION	GENERATING EACH TIMING ACCORDING TO 9MCLK, CELL-FRAME (CF), AND ENABLE (EN) SIGNAL.
ICI/ISSI, MH ST, SA/DA, MID IDENTIFICATION	IDENTIFYING DESTINATION ICI/ISSI, DESTINATION MH, SEGMENT TYPE, SA/DA, AND MID ACCORDING TO CELL DATA.
ERR. ANALYSIS	ANALYZING ERROR TYPE ACCORDING TO ERROR FLAG (EF) SIGNAL
OUTGOING LOG-REG.	AREA THROUGH WHICH ERROR TYPE, DESTINATION ICI/ISSI, SA, AND DA ARE REPORTED TO FIRMWARE WHEN LOG OBJECT ERROR HAS OCCURRED
L2/3 INDIVIDUAL ERR. D. P. RAM	DUAL PORT RAM STORING COUNT VALUE OF L2/3 INDIVIDUAL ERROR.
NDC COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUE RELATED TO NETWORK DATA COLLECTION.
BILLING COUNT VALUE D. P. RAM	DUAL PORT RAM STORING COUNT VALUES RELATED TO BILLING OPERATIONS.

FIG. 668

CHECK NAME	CHECK OBJECT
CLK a	19M CLOCK FROM HLP07A, AND DISCONNECTION OF FRAME PULSE
CLK b	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FROM INCOMING LP
CLK c	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF ERROR FLAG 2 FROM INCOMING LP
CLK d	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FROM OUTGOING LP
CLK e	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF ERROR FLAG 2 FROM OUTGOING LP
CLK f	19M CLOCK GENERATED INTERNALLY, AND DISCONNECTION OF CELL FRAME FRAME FROM OUTGOING LP
WDT I	TIME OUT OF WATCHDOG TIMER, AND DISCONNECTION MPU OUTPUT 8M CLOCK
PC a	DATA FROM INCOMING LP, PARITY CHECK OF ENABLE
PC b	DATA FROM OUTGOING LP, PARITY CHECK OF ENABLE
PC c	DATA FROM OUTGOING LP, PARITY CHECK OF ENABLE
PC d	PARITY CHECK OF SA/DA ACCUMULATION RAM
PC f	PARITY CHECK OF THRESHOLD RAM
PC g	PARITY CHECK OF L2/3 SUM F ERR. COUNT VALUE D. P. RAM
PC h	PARITY CHECK IF INCOMING L2/3 INDIVIDUAL ERR. COUNT VALUE D. P. RAM
PC i	PARITY CHECK OF INCOMING NDC COUNT VALUE D. P. RAM
PC j	PARITY CHECK OF OUTGOING L2/3 INDIVIDUAL ERR. COUNT VALUE D. P. RAM
PC k	PARITY CHECK OF OUTGOING NDC COUNT VALUE D. P. RAM
PC I	PARITY CHECK OF BILLING COUNT VALUE D. P. RAM

FIG. 669

CHECK NAME	CHECK CONDITIONS
PC d	NOTIFICATION OF LOG-REQUIRED ERROR FROM INCOMING LP
PC f	NOTIFICATION OF ERROR RELATED TO L2/3 SUM OF ERROR FROM INCOMING LP
PC g	NOTIFICATION OF ERROR RELATED TO L2/3 SUM OF ERROR FROM INCOMING LP
PC h	NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM INCOMING LP
PC i	NOTIFICATION OF NDC INDIVIDUAL COUNT ERROR FROM INCOMING LP
PC j	NOTIFICATION OF L2/3 INDIVIDUAL COUNT ERROR FROM OUTGOING LP

FIG. 670

GROUP	ITEM	LEVEL	CHECK	No	ERROR GENE- RATING CELL	ACTION
A	1	L 2	MRI. TIME OUT	2	EOM (PSEUDO EOM)	COUNT
B	1	L 2	INVALID PAYLOAD CRC CODE	3	BOM, COM, EOM	DISCARD COUNT
C	1	L 2	PAYLOAD LENGTH REEOR	4	BOM, COM, EOM	DISCARD COUNT
D	1	L 2	BOM WITH UNEXPECTED MID	5	BOM	COUNT
	2	L 2	EOM WITH UNEXPECTED MID	5	EOM	DISCARD COUNT
E	1	L 2	UNEXPECTED SN ERROR	6	COM, EOM	DISCARD COUNT
F	1	L 3	INVALID BASIZE FIELD VALUE	7	BOM	DISCARD COUNT
	2	L 3	INVALID DA TYPE	8	BOM	DISCARD COUNT
	3	L 3	INVALID SA TYPE	9	BOM	DISCARD COUNT
	4	L 3	INVALID SERVICE TYPE (ISSI)	11	BOM	DISCARD COUNT LOG
	5	L 3	INVALID PROTOCOL ID (ICI)	11	BOM	DISCARD COUNT LOG
	6	L 3	INVALID PROTOCOL DISCRIMINATOR	13	BOM	DISCARD COUNT LOG
	7	L 3	HOP COUNT = 0	15	BOM	DISCARD COUNT LOG
	8	L 3	INVALID INGRESS INTERFACE TYPE	16	BOM	DISCARD COUNT LOG
	9	L 3	BETAG MISMATCH	18	EOM	DISCARD COUNT
G	1	UNIQUE	MID ASSIGNED ERROR	20	BOM	DISCARD COUNT
	2	UNIQUE	EXCEED MAXIMUM NUMBER OF CDU	21	BOM	DISCARD COUNT
	3	UNIQUE	ROUTING ERROR	22	BOM	DISCARD COUNT
	4	UNIQUE	BASIZE \neq LENGTH	23	EOM	DISCARD COUNT
	5	UNIQUE	ENCAPSULATION ERROR	24	SSM	DISCARD COUNT

FIG. 671

SIGNAL NAME	POLARITY	EXPLANATION
9M CLOCK	—	ALL SIGNALS STARTING WITH REFERENCE CLOCK ARE CHANGED AT RISE OF MAIN CLOCK.
CELL FRAME	↔	SIGNAL INDICATING BOUNDARY OF CELL. L FOR ONLY LAST 17 OF CELL.
ENABLE	↔	SIGNAL INDICATING VALID/INVALID CELL. ALL CELL AREAS ARE L WHEN VALID.
ERROR NOTIFICATION (2)	↔	SIGNAL INDICATING ERROR TYPE. DETAILED EXPLANATION IS GIVEN LATER AND ERROR IS REPRESENTED BY L.
DATA	PLUS	16 PARALLEL DATA + PARITY. PARITY IS ODD PARITY FOR ALL 17 BITS OF 16 BIT PARALLEL DATA + ENABLE.

FIG. 673

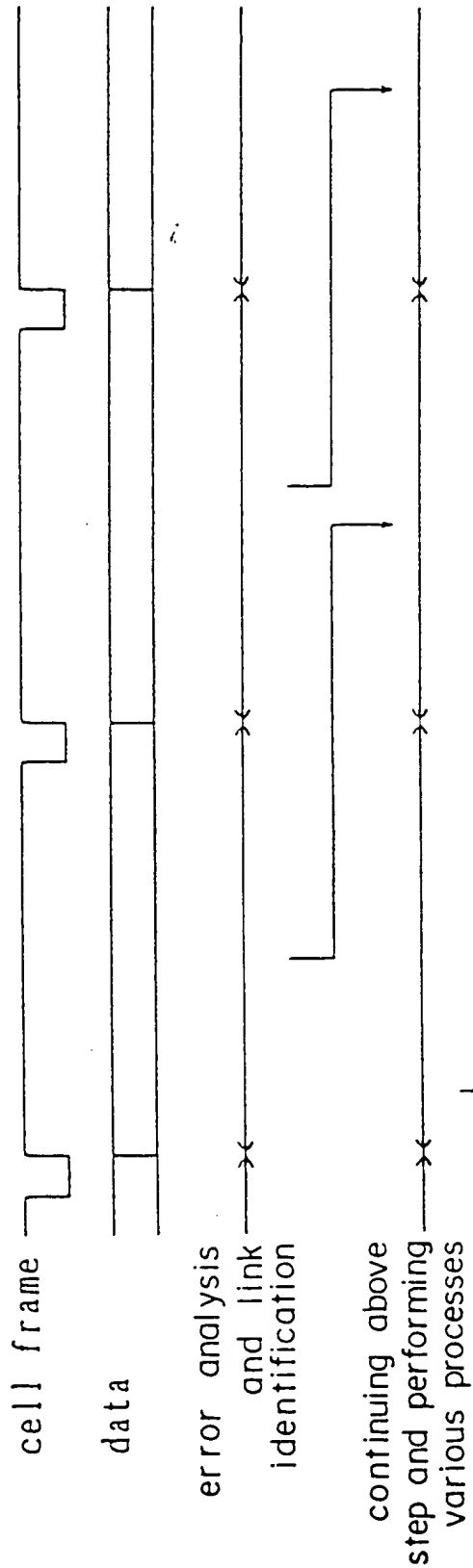


FIG. 675

Group	Item	Level	Check	No.	Error generating cell	Action
A	1	L2	MRI time out	1	EOM(Pseudo-EOM)	Count
B	1	L2	MID currently active	4	BOM	Count
	2	L2	EOM with unapproved MID	4	EOM	Count of discard
C	1	L2	Unexpected SN error	5	BOM, COM, EOM	Count of discard
D	1	L3	ISSI/ICI Unavailable	7	BOM	Count Log of discard
E	1	Unique	Exceed maximum number of CDU	8	BOM	Count of discard
	2	Unique	Encapsulation Error	1	SSM	Count of discard

FIG. 676

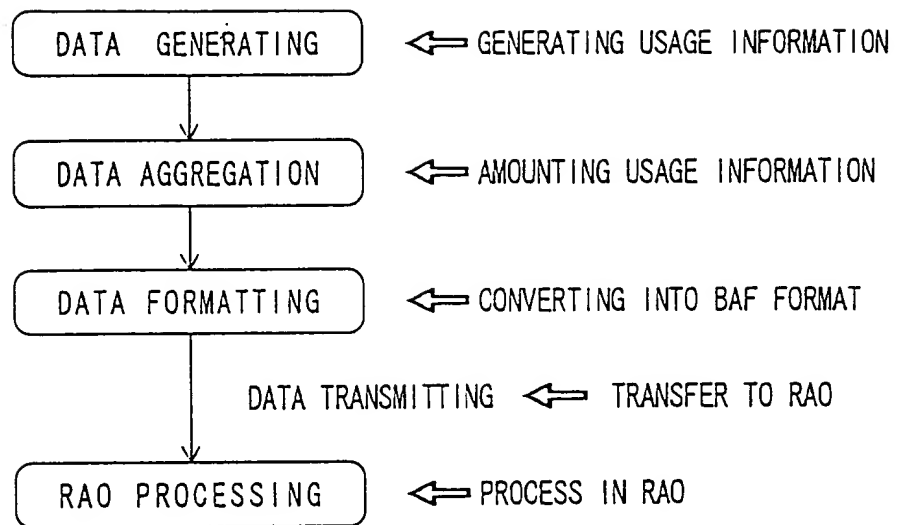


FIG. 682

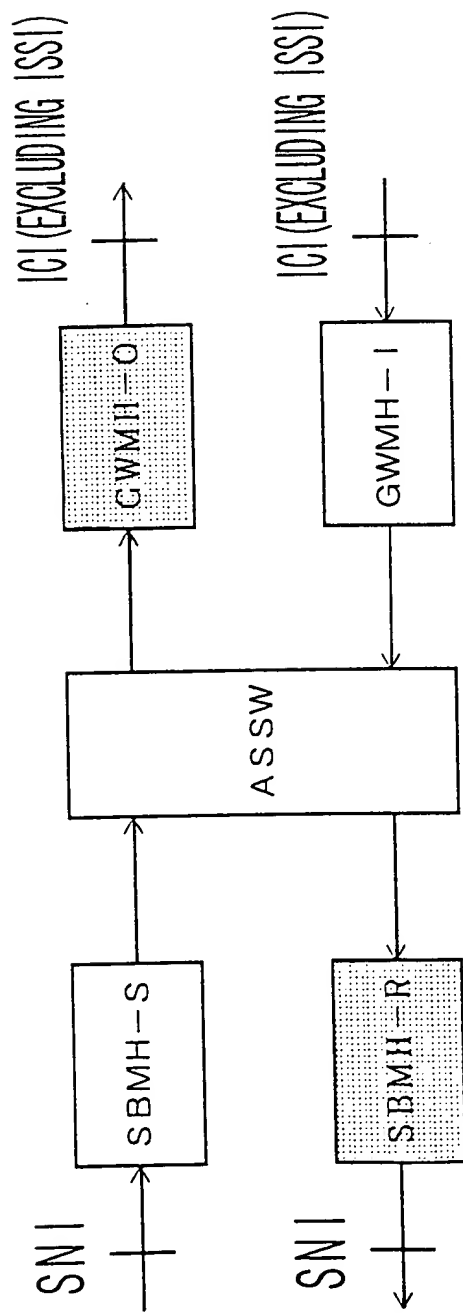


FIG. 683

FIGURE	LEC Network Function	SA	DA	SHI Add	Incoming HW ID	Incoming ICI TPS ID	Outgoing HW ID	Outgoing ICI TPS ID	Carrier ID	Cond Code	Packet Count	Seg. Count	Ingress Inf Type
INDIVIDUAL ADDRESS DATA TRANSFER	1	Orig. YA-SMDS (ICI)	O		*	*	O	O		O	O	O	O (CIC)
	2	Source Function for Exchange SMDS (ICI)	O		*	*	O	O		O	O	O	O (HBCA)
	7	Term. YA-SMDS (SHI)	O		O	O				O	O	O	O (CIC)
	8	Dest. Function for Exchange SMDS (SHI)	O		O	O				O	O	O	O (HBCA)
GROUP ADDRESS DATA TRANSFER	1	Orig. YA-SMDS (ICI)	O	O	*	*	O	O		O	O	O	O
	2	Source Function for Exchange SMDS and Orig. YA-SMDS (ICI)	O	O	*	*	O	O		O	O	O	O
	3	Term. YA-SMDS (ICI)	O	O	O	O	O	O		O	O	O	O
	4	Dest. Function for Exchange SMDS (ICI)	O	O	O	O	O	O		O	O	O	O
	5	Dest. Function for Orig. YA-SMDS (ICI)	O	O	O	O	O	O		O	O	O	O
	6	Source Function for Term. YA-SMDS (ICI)	O	O	O	O	O	O		O	O	O	O
	7	Term. YA-SMDS (SHI)	O	O	O	O			O	O	O	O	O
	8	Dest. Function for Exchange SMDS (SHI)	O	O	O	O			O	O	O	O	O
	9	Dest. Function for Term. YA-SMDS (SHI)	O	O	O	O			O	O	O	O	O

O: REQUIRED. *: SETTING O. NO MARK: NOT REQUIRED.

IP)+RDA (ICIP)+RSA+RCA

0	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
1	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
2	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
...	...
FFF	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
FFF	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit
FFF	SA 64bit, DA(SIP) 64bit, DA(ICIP) 64bit, CARRIER INFORMATION 37 bit

FIG. 685

ICI ID = 0

L2__PDU, L3__PDU
.
.
.
7 L2__PDU, L3__PDU

FIG. 686

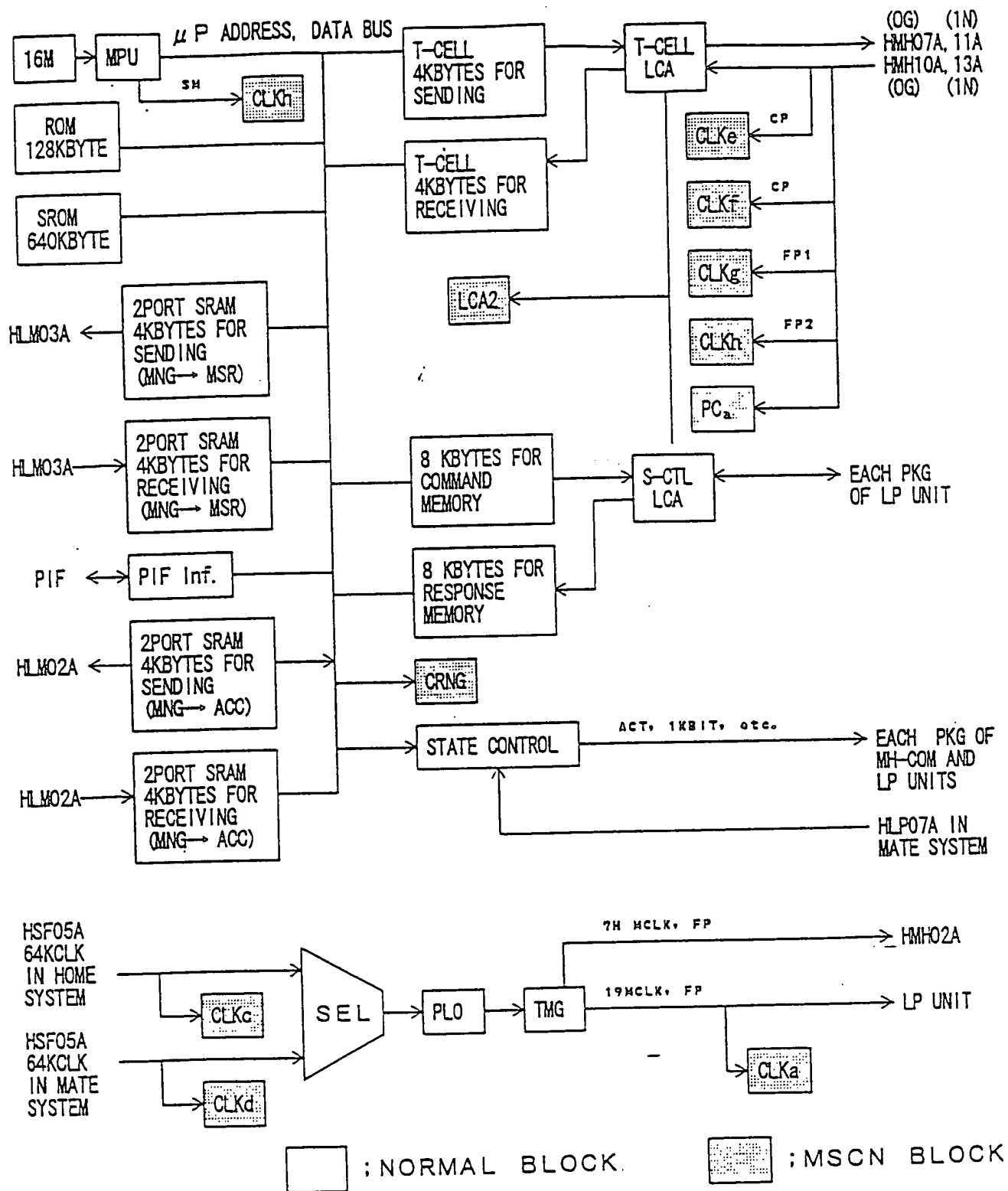


FIG. 687

BLOCK NAME	FUNCTION
16M	GENERATING 16 MHz CLOCK FOR MICROPROCESSOR
MPU	μP (80C186)
ROM	STORING FIRMWARE FOR MPU
FOR SENDING T-CELL	MEMORY FOR SENDING TEST CELL
FOR RECEIVING T-CELL	MEMORY FOR RECEIVING TEST CELL
T-CELL LCA	SENDING TEST CELL FOR HMH01A AND 03A, (ASSIGNING ODD PARITY, ADJUSTING TIMING), RECEIVING TEST CELL FROM HMH02A AND 06A, MAKING PARITY CHECK, ETC.
SRAM	WORK MEMORY FOR MPU
FOR SENDING 2 PORT SRAM MNG \rightarrow MSR	DATA SENDING MEMORY FOR MSR-FIRMWARE
FOR RECEIVING 2 PORT SRAM MNG \leftarrow MSR	DATA RECEIVING MEMORY FROM MSR-FIRMWARE
FOR SENDING 2 PORT SRAM MNG \rightarrow ACC	DATA SENDING MEMORY FOR ACC-FIRMWARE
FOR RECEIVING 2 PORT SRAM MNG \leftarrow ACC	DATA RECEIVING MEMORY FROM ACC-FIRMWARE
INF inf	CONTROLLING INTERFACE WITH INF
FOR COMMAND MEMORY	SRAM FOR SENDING COMMAND
FOR RESPONSE MEMORY	SRAM FOR RECEIVING RESPONSE
S-CTL LCA	CONTROLLING COMMAND AND RESPONSE FOR LP UNIT
STATE CONTROL	CONTROLLING ACT, INHBIT, ETC. CONTROLLING OCS TO MATE SYSTEM
SEL	SELECTING 64 KHz CLOCK RECEIVED FROM MH-COM OF HOME AND MATE SYSTEMS.
PLO	SELECTING 155 Hz CLOCK IN SYNCHRONISM WITH 64 MHz CLOCK.
TMG	GENERATING 78 MHz AND 19 MHz CLOCKS FROM 155 MHz CLOCK.

FIG. 688

669660 612260

BLOCK NAME	FUNCTION
CLK b	μ P OPERATION 8 M CLOCK DISCONNECTION
CLK e	DISCONNECTION OF SENDING CELL FRAME (COMMON BETWEEN ICLP AND OGLP)
CLK f	DISCONNECTION OF RECEIVING CELL FRAME (COMMON BETWEEN ICLP AND OGLP)
CLK g	DISCONNECTION OF ERROR FLAG 1 (COMMON BETWEEN ICLP AND OGLP)
CLK h	DISCONNECTION OF ERROR FLAG 2 (COMMON BETWEEN ICLP AND OGLP)
PC a	RECEIVING CELL DATA PARITY NG (COMMON BETWEEN ICLP AND OGLP)
LCA 2	HLP07A LCA CONFIGURATION NG
CRNG	ABNORMAL COMMAND AND RESPONSE AT S-CTL1
CLK c	HOME SYSTEM 64K CLOCK DISCONNECTION
CLK d	MATE SYSTEM 64K CLOCK DISCONNECTION
CLK a	19M CLOCK/FRAME PULSE DISCONNECTION

FIG. 689

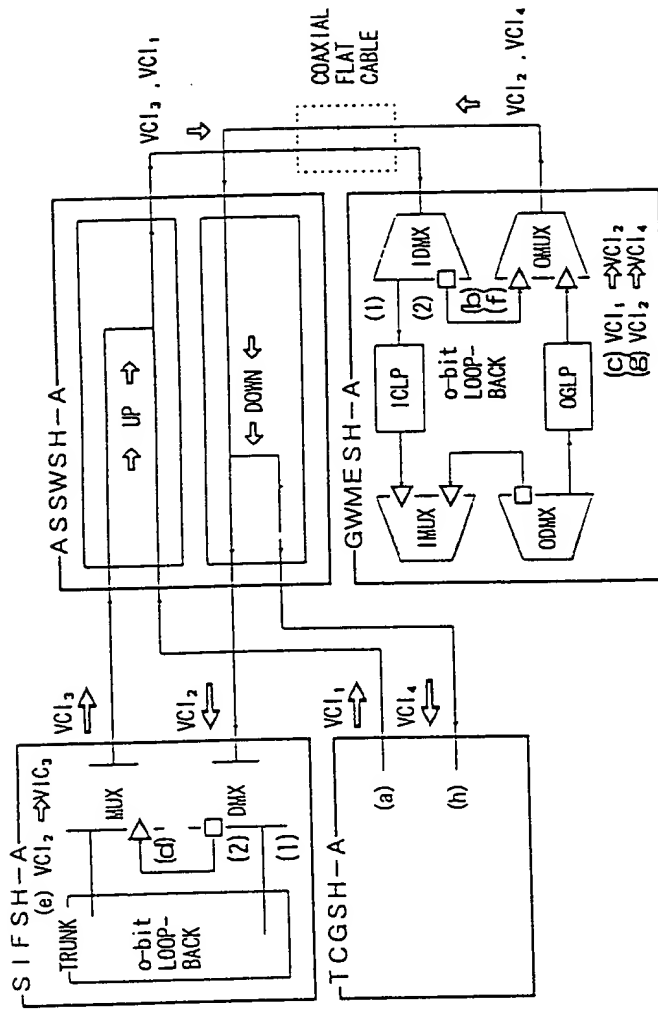
ITEM	FAULT TYPE	NOTIFICATION METHOD	NOTIFYING SYSTEM	TEST DEVICE	ACTION					PROCEDURE	REMARKS
					ASSW SYSTEM SWITCH	FAULT BLOCK	FAULT MESSAGE	ALM LIGHTING	DIAGNOSTICS PROCESS		
1	HARDWARE FAULT EXCLUDING SIGNAL PROCESSING UNIT AND OMUX.	HOME SYSTEM	ACT	ACT MFCOM	○	○	○	○	○ PREVIOUSLY ACT	②	DIAGNOSTICS IS ACTIVATED BY MATE SYSTEM.
			SBY	SBY MFCOM	—	○	○	○	○ SBY	①	
2	HARDWARE FAULT OF SIGNAL PROCESSING UNIT AND OMUX.	MATE SYSTEM E-MSCN	ACT	SBY MFCOM	—	○	○	○	○ SBY	③	
			SBY	ACT MFCOM	○	○	○	○	○ PREVIOUSLY ACT	④	
3	OBP FAULT	MATE SYSTEM E-MSCN	ACT	SBY MFCOM	—	○	○	○	○ SBY	③	
			SBY	ACT MFCOM	○	○	○	○	○ PREVIOUSLY ACT	④	
4	MATE POWER SOURCE PNCB FAULT (FUSE DIS-CONNECTION)	MATE SYSTEM E-MSCN	ACT	SBY POWER SOURCE PNCB	—	○	○	○	○ SBY	③	MFCOM PROVIDED BY POWER SOURCE PNCB IS BLOCKED, AND ASSW-A IN HOME SYSTEM IS ALSO BLOCKED.
			SBY	ACT POWER SOURCE PNCB	○	○	○	○	○ PREVIOUSLY ACT	④	

FIG. 691

0000000000000000

VPI	VC I	UL	TAGA	TAGB	TAGC	COM	SIG	0
ALL '0'	03FA	0	2.4G HW NUMBER (0-3 FOR CARD NUMBER OF ASSW HMX03A)	622M HW NUMBER (0-3 FOR HW NUMBER IN ASSW HMX03A)	155M HW NUMBER (0-3 FOR SH NUMBER OF GMMESH)	0	0	1
	OR							
	03FB							

FIG. 692



- (a) GENERATING TEST CELL (0-BIT IS 1) OF VCI₁ AND SWITCHING TAG FOR IDMX FROM TCGSH-A
- (b) DROPPING CELL OF 0-BIT=1 AT IDMX AND LOOPING IT BACK TO ODMX.
- (c) CONVERTING VCI=VCI₁ INTO VCI₂ AT ODMX AND PROCESSING IT AS TEST-CELL OF SWITCHING TAG FOR TRUNK.
- (d) DROPPING CELL OF 0-BIT=1 AT DMX OF SIFSH-A HAVING TRUNK AND LOOPING IT BACK TO MUX.
- (e) CONVERTING VCI=VCI₁ INTO VCI₂ AT MUX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR IDMX.
- (f) DROPPING CELL OF 0-BIT=1 AT IDMX AND LOOPING IT BACK TO ODMX.
- (g) CONVERTING VCI=VCI₁ INTO VCI₂ AT ODMX AND PROCESSING IT AS TEST CELL OF SWITCHING TAG FOR TCGSH-A.
- (h) CHECKING CONTENTS OF TEST CELL AT TCGSH-A.

NOTE : DROP ONLY FOR ☐ 0-BIT=1 ☐ VCC

FIG. 693

669200 6122000

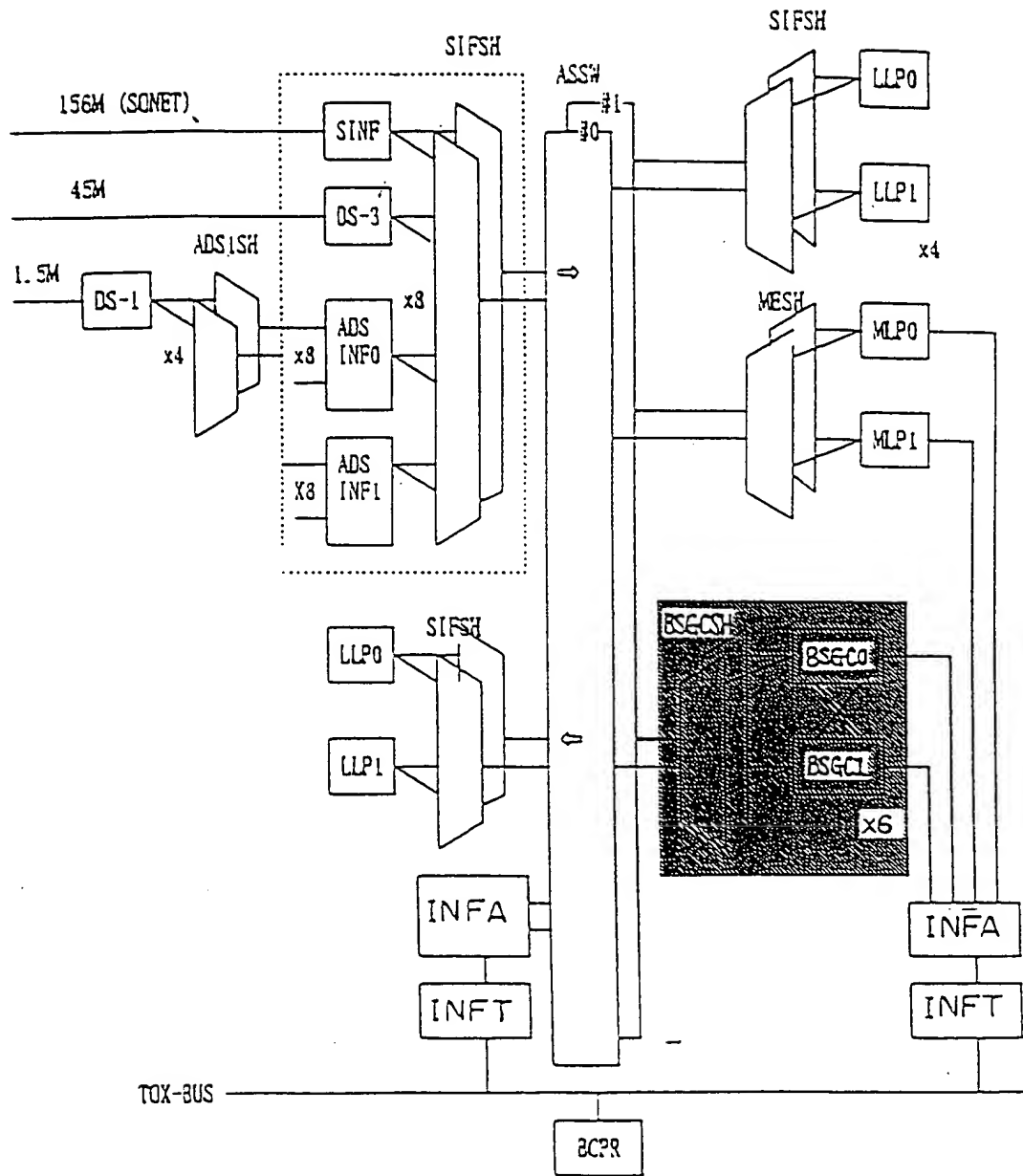


FIG. 698

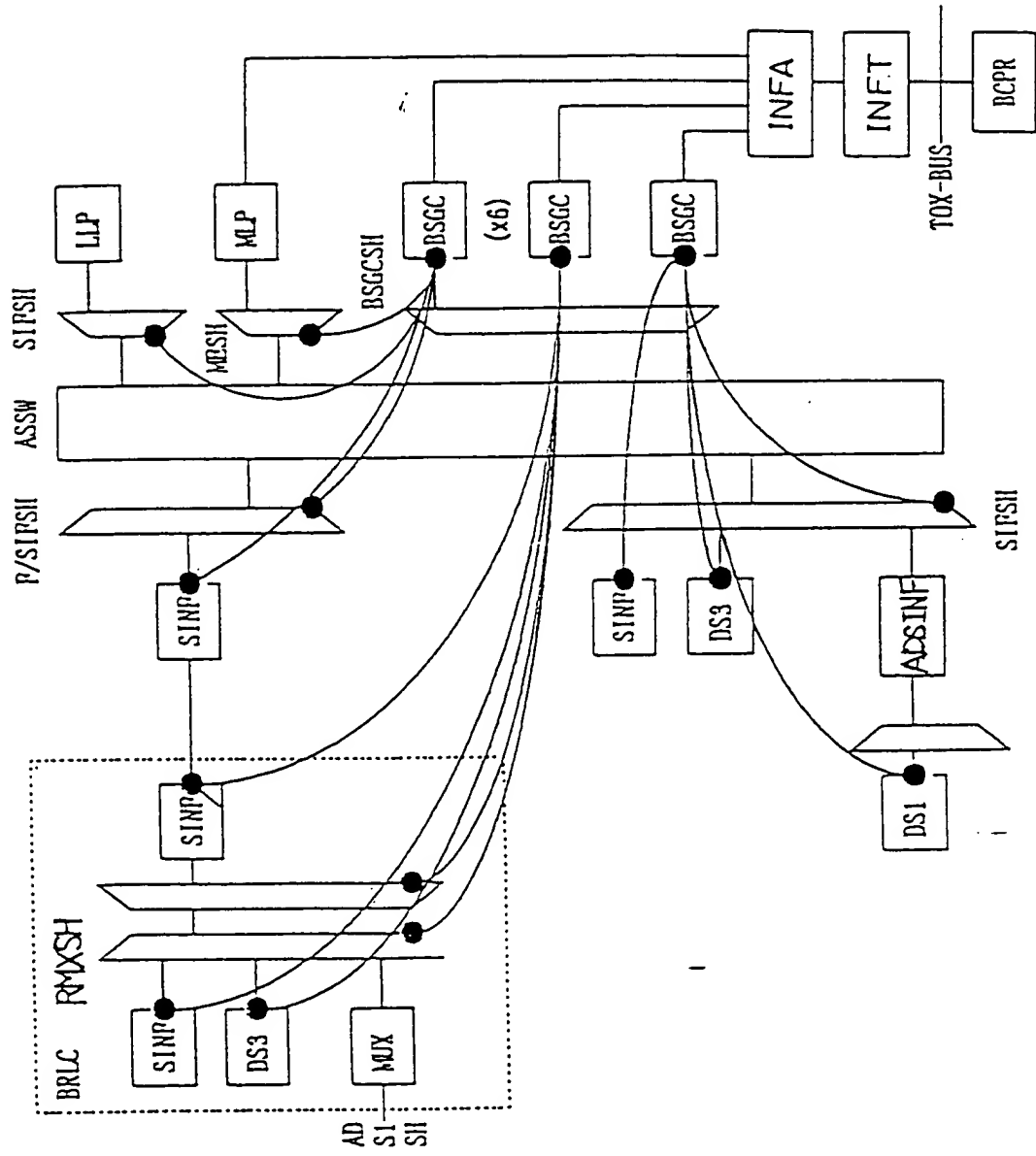


FIG. 699

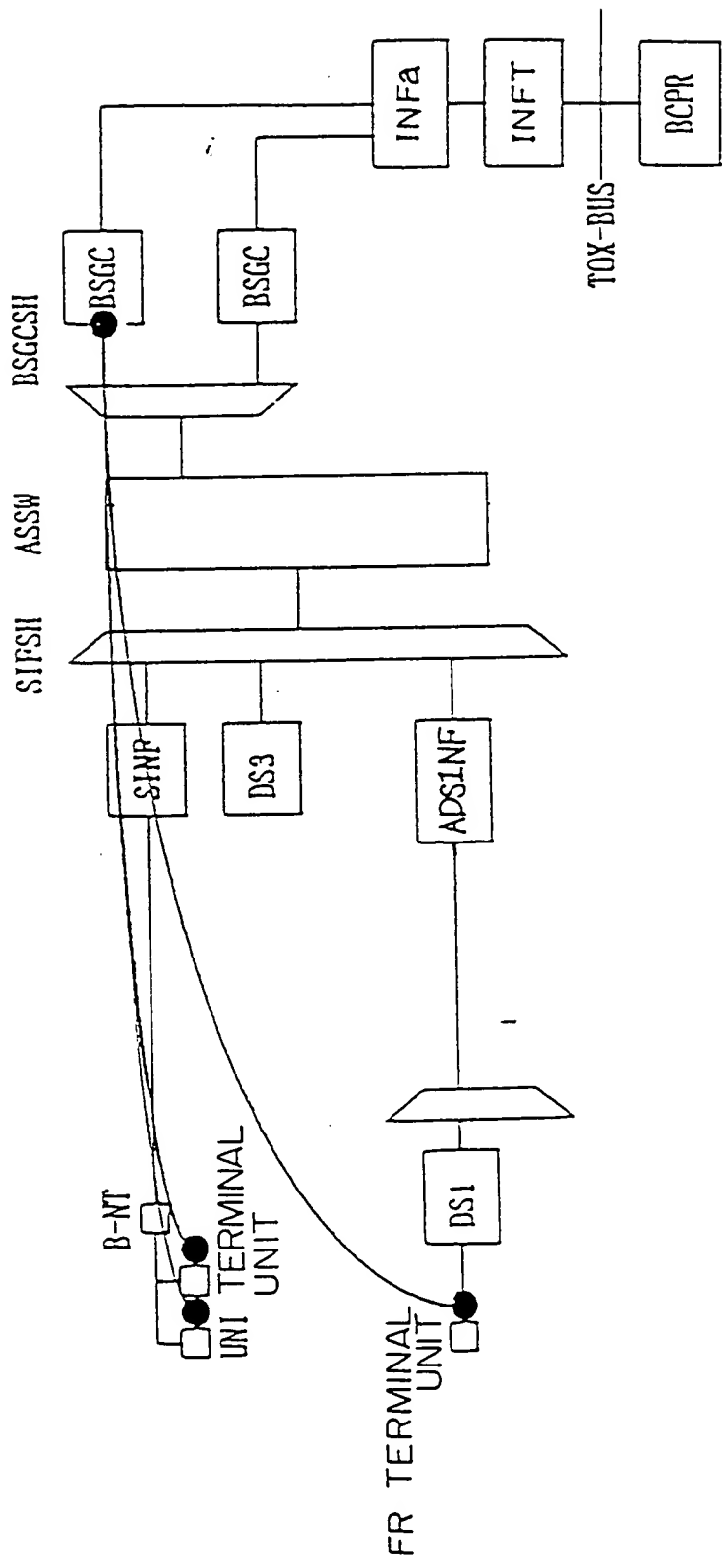


FIG. 700

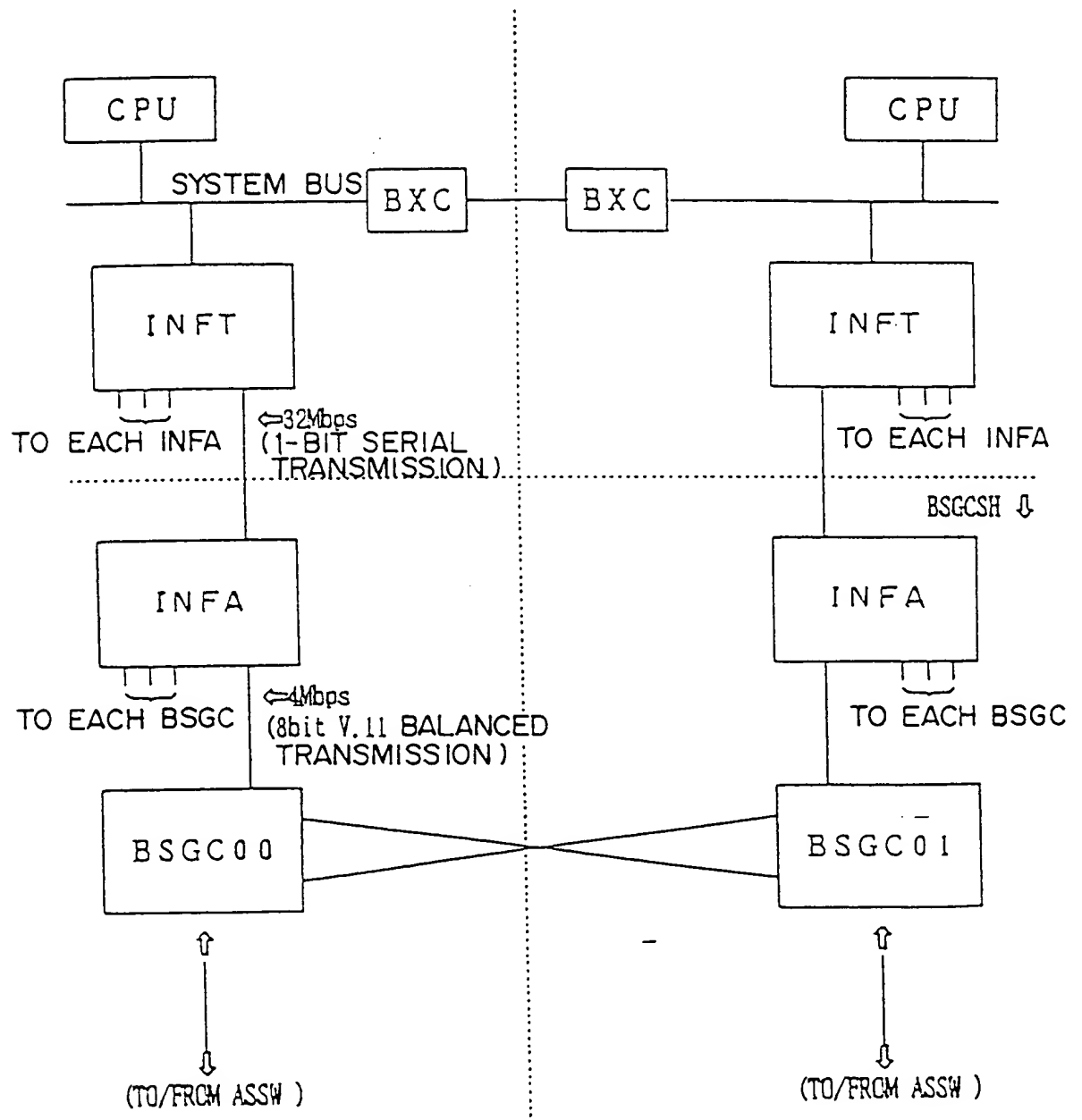
665550-672260

NO	I T E M		S P E C I F I C A T I O N	R E M A R K S
1	B S G C A R D	PROCESSOR	MBL80186(16 BIT MICRO PROCESSOR)	
2		REDUNDANCY	DUPLICATION	
3		MEMORY CAPACITY	ROM 256 K BYTE (BANK SWITCH) S-RAM 32 K BYTE D-RAM 896 K BYTE	
4		MAXIMUM NUMBER OF SIMULTANEOUS LINK CONNECTIONS	256 CHANNEL (TO BE EXTENDE INTO 1024 CHANNEL*)	
5		SBIF LSI	INF FOR CONTROLLING MB651623	
6		CARP1/2 LSI	CLAD FOR CONTROLLING MBCG31134, MB630615	
7		MUX	CELL MULTIPLEX LSI MBCG31204-639	
8		ACT CONTROL	DEPENDING ON ACT OF INF	
9		NUMBER OF PCB	1 PCB	
10	C O M	VCC	TAG CONVERSION MEMORY MBCG21503	
11		SELN1	O&M FOR CONTROLLING MBCG21XXX	
12		MUX	CELL MULTIPLEX LSI MBCG31204-639	
13		DMUX	CELL DEMULTIPLEX LSI HBCG31204-638	
14		ACT CONTROL	DEPENDING ON ACT OF SWITCH	
15		NUMBER OF PCB	5 PCB	
16	S	SHELF CONFIGURATION	LOADED WITH ONE SYSTEM 6 BSGC AND 1 COM	
17	H	DUPLEX CROSS CONNECTION	CROSS CONNECTION OF BSGC AND COM	
18	E L F	FUNCTIONS	①TERMINATING INTRA-STATION DEVICE LINK ②META-SIGNAL COMMUNICATIONS PORT CONTROL ③SUBSCRIBER TERMINAL UNIT SIGNALING PORT CONTROL ④SVC PORT CONTROL OF DS1FR ⑤SETTING VCC (ONLY STARTING NUMBER BSGC)	

F I G . 7 0 1

0 SYSTEM

1 SYSTEM



※ FOUR BSGCs ARE CONNECTABLE FOR AN INFA.
BSGCSH ACCOMMODATES 6BSGCs

FIG. 702

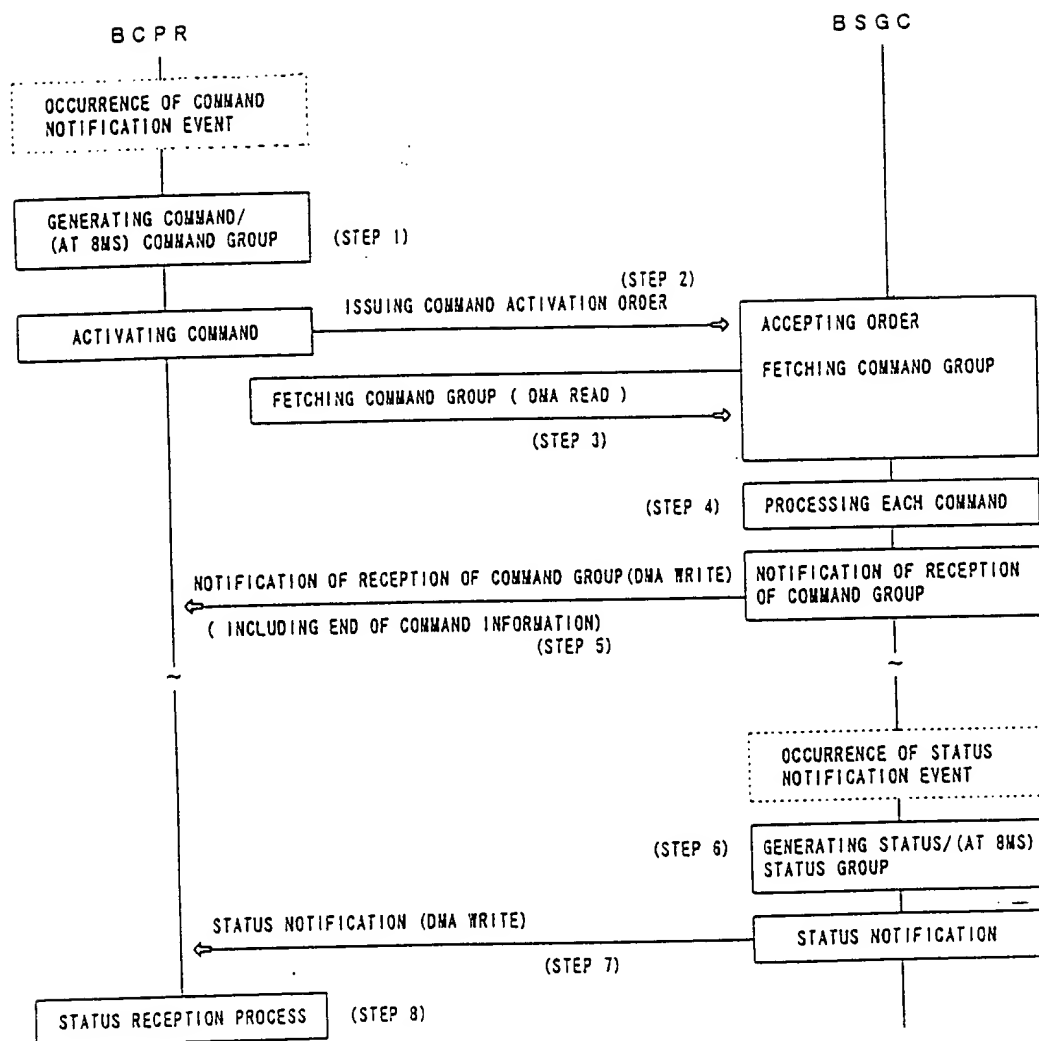
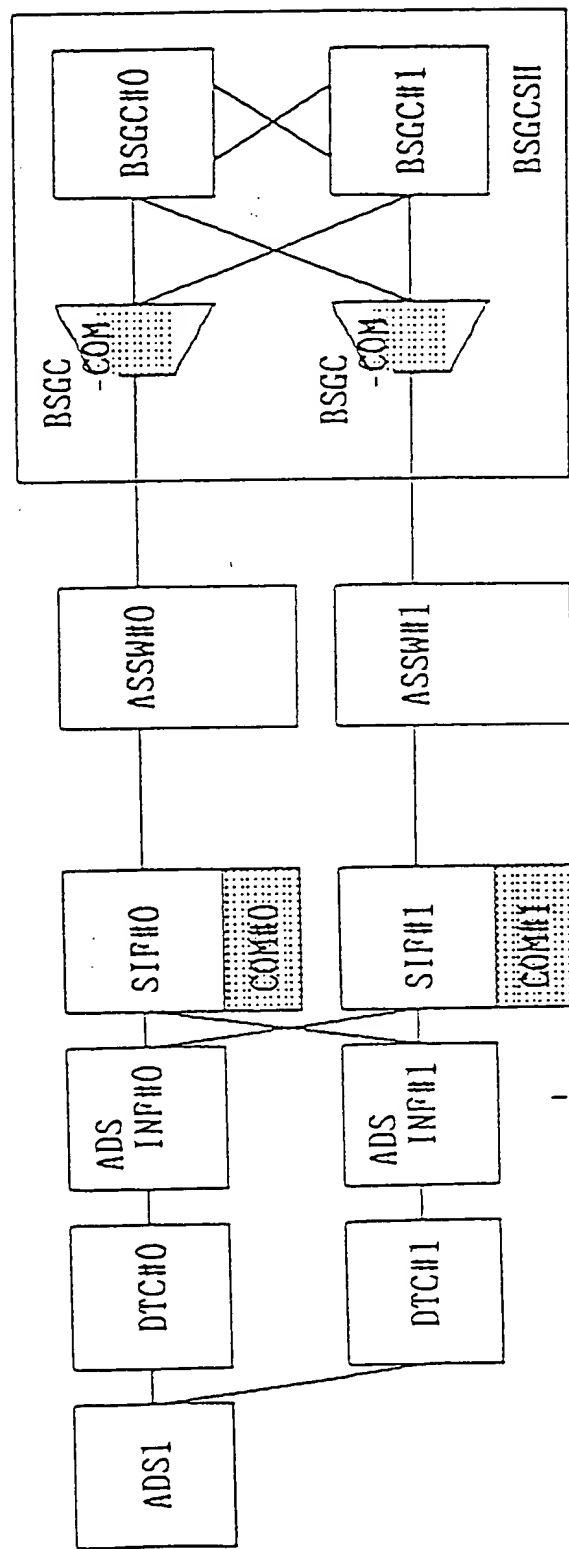


FIG. 703



- note) 1. : LOADED BY VCC
 2. ACT OF BSGCCOM IS DEPENDENT ON SWITCH
 3. ACT OF BSGC IS DEPENDENT ON INDIVIDUAL SYSTEM SPECIFICATION OF INF.

FIG. 704

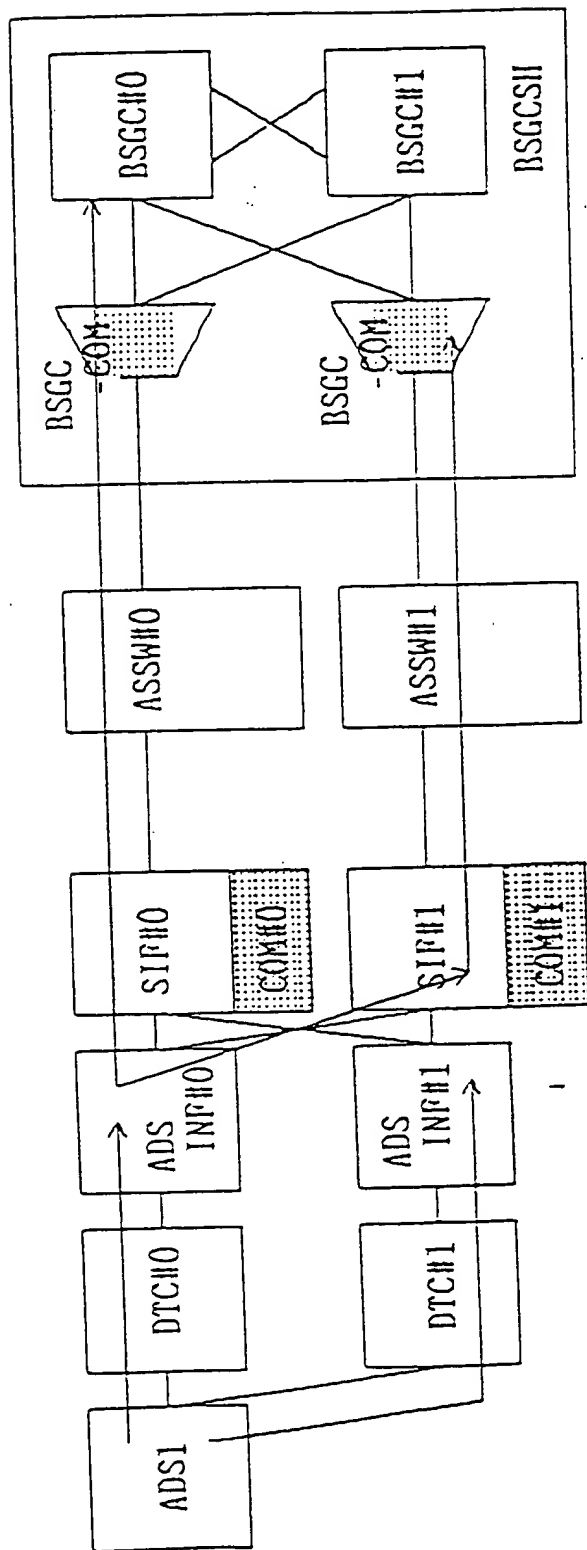


FIG. 705

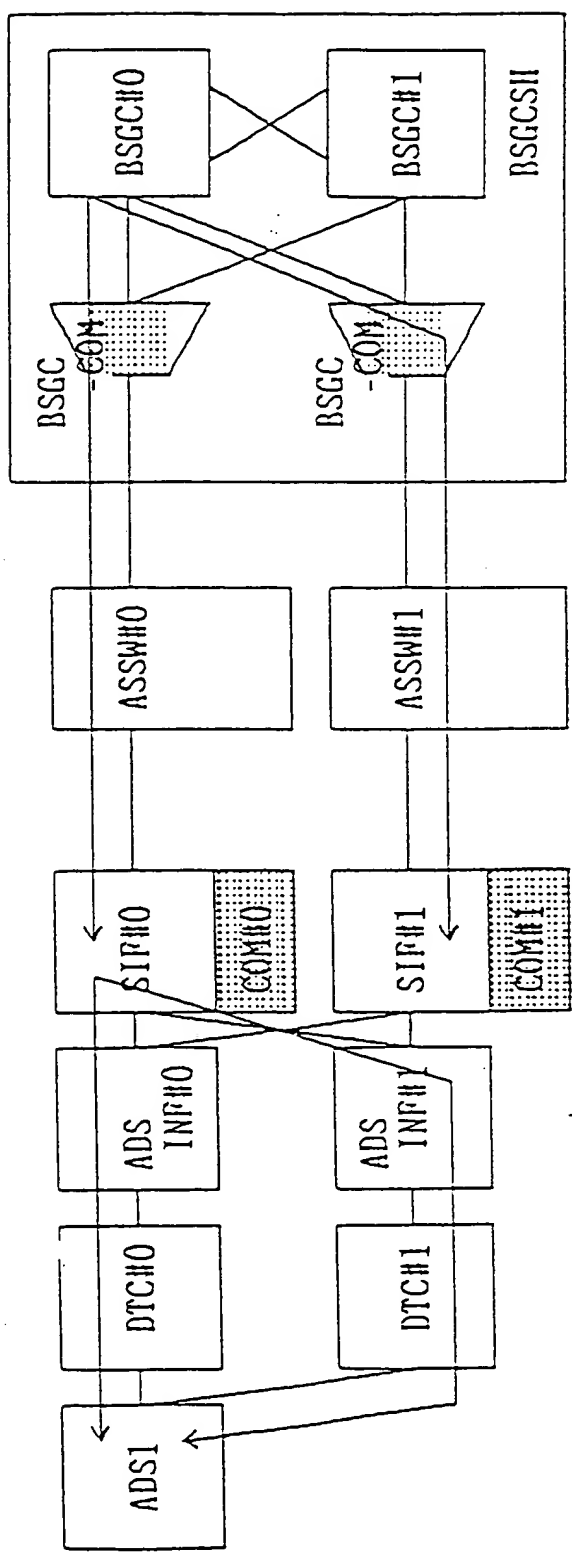


FIG. 706

66960-672260

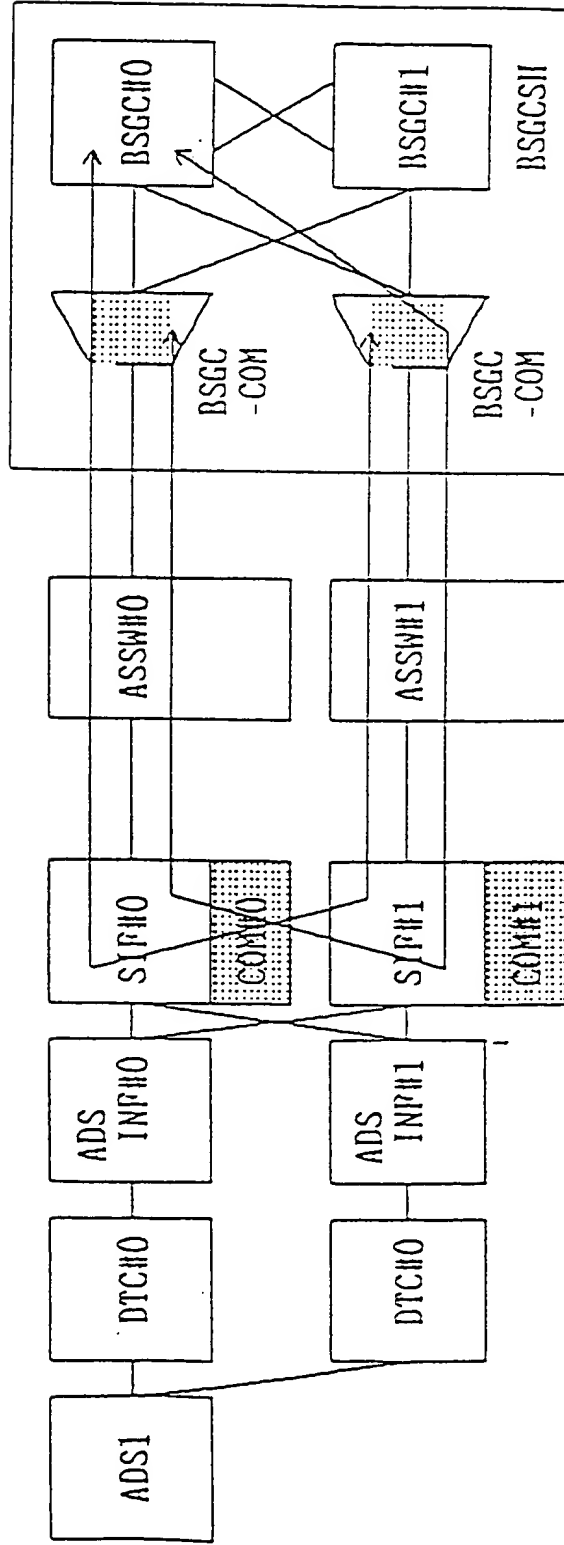


FIG. 707

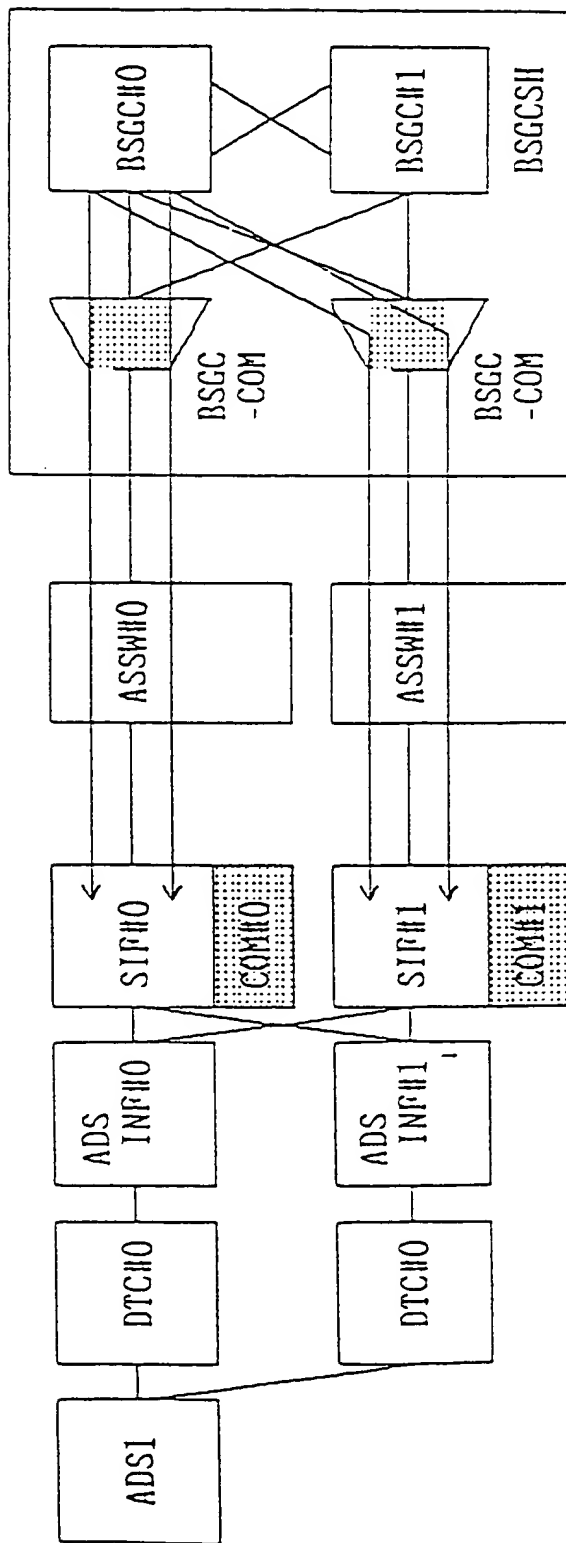


FIG. 708

669660-672260

(a) IN HOST/BRLC

VPI (H)	VCI (H)	U S E
FROM 00 TO 3F	FROM 0000 TO 001F	REQUIREMENT RESERVE E. G. FOR SIGNALING FOR OAM CELL
	FROM 0020 TO 03EF	USER CELL E. G. FOR ATM-UNI, CE, FR
	FROM 03F0 TO 03FE	SYSTEM RESERVE FOR INTRA-STATION LAP SIF-COM #0 : VPI=00, VCI=03FC SIF-COM #1 : VPI=00, VCI=03FD RMX-COM #0 : VPI=3F, VCI=03F0 RMX-COM #1 : VPI=3F, VCI=03F1 DS3, SINF : VPI=00, VCI=03FE DS1 : VPI=AA, VCI=03FE AA: 5 LOWER ORDER BITS ARE FOR DS1 UNIT NUMBER FOR TEST : VPI=00, VCI=03FA, 03FB
	03FF	USER CELL (EXCLUSIVELY FOR SMDS)

(b) IN UNBILICAL LINK

VPI (H)	VCI (H)	U S E
FROM 00 TO XX	FROM 0000 TO 001F	REQUIREMENT RESERVE E. G. FOR SIGNALING FOR OAM CELL
	FROM 0020 TO 03EF	USER CELL E. G. FOR ATM-UNI, CE, FR
3 F	FROM 0020 TO 03EF	FOR INTRA LAP OF SIMPLEX DEVICE IN BRLC
	FROM 03F0 TO 03F7	FOR INTRA LAP OF DUPLEX DEVICE IN BRLC

F I G. 7 1 0

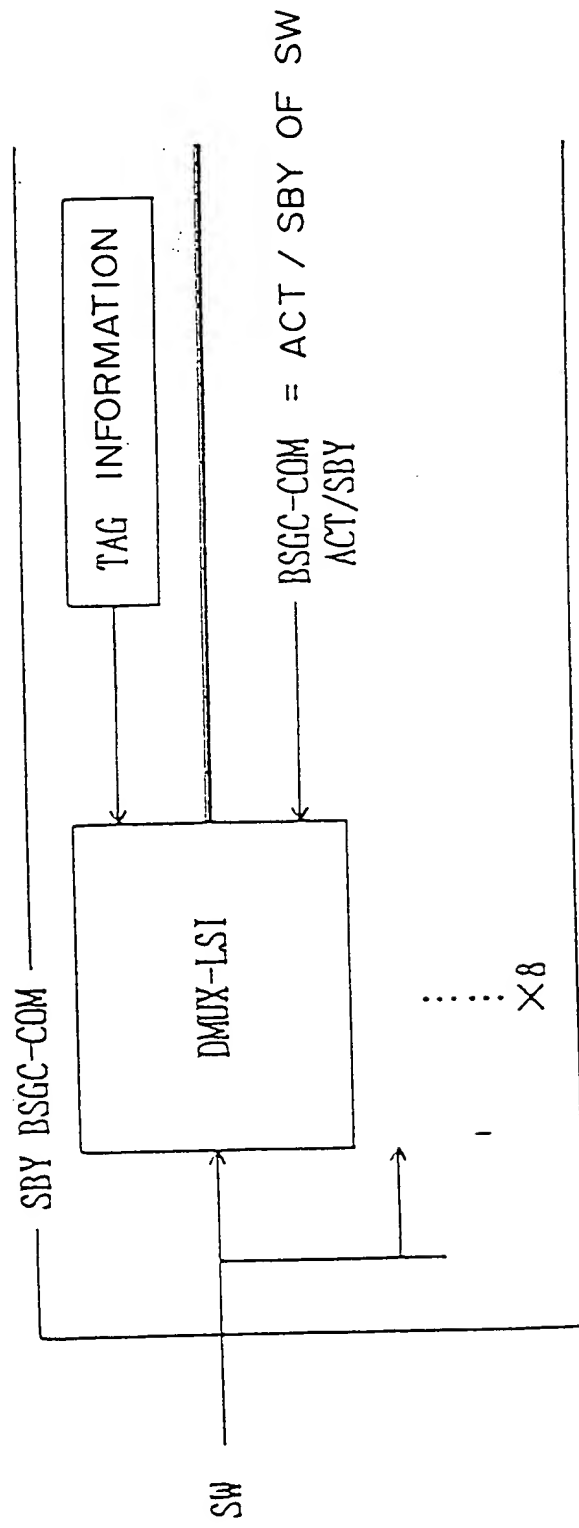


FIG. 711

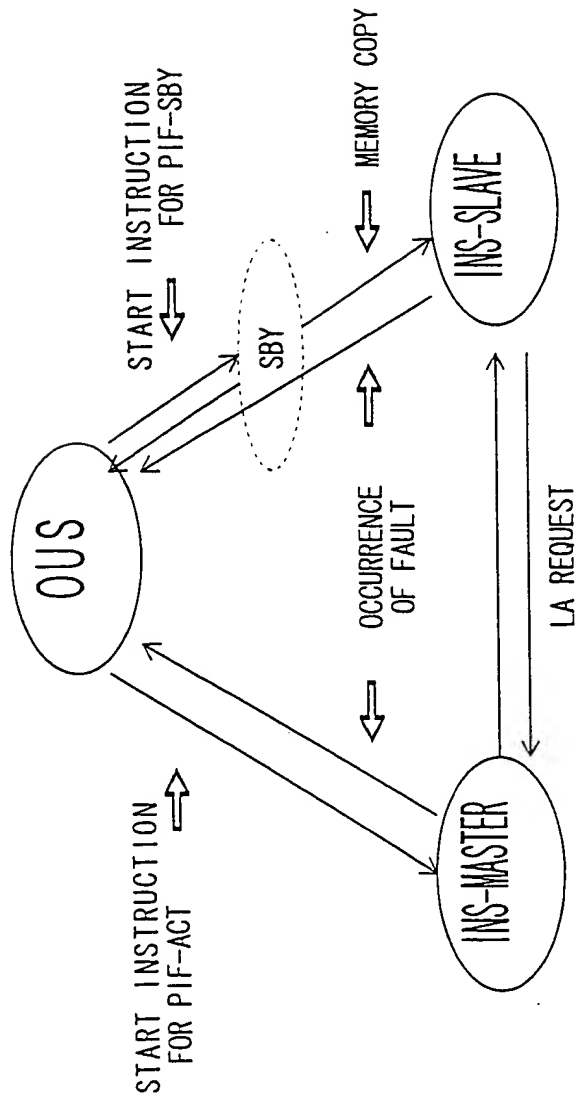


FIG. 712

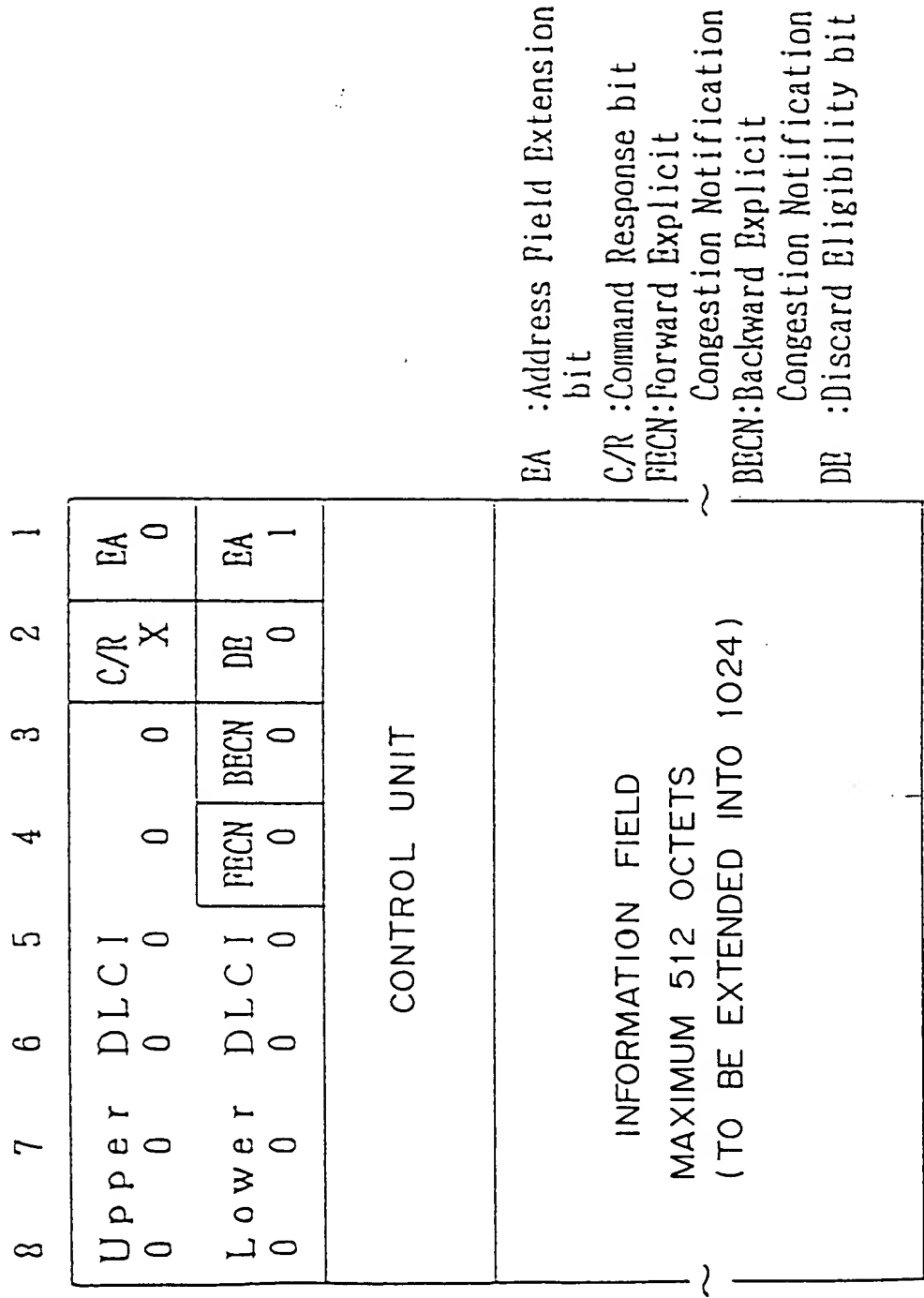
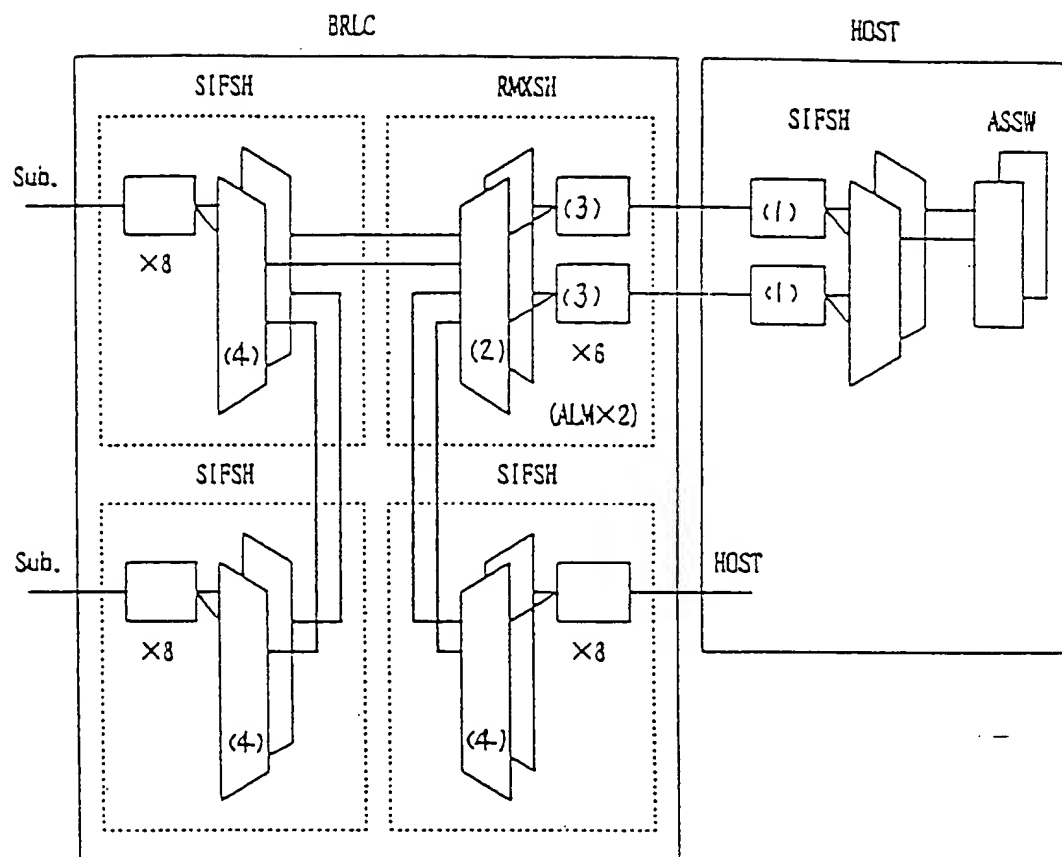


FIG. 713



(1) - (4) : INDICATES LAP LINK SETTING NUMBER
 (1) AND (3) : SIMPLEX COMMUNICATIONS PORT
 (2) AND (4) : 2 LINKS OF ACT/SBY ARE ESTABLISHED FOR DUPLEX COMMUNICATIONS PORT.
 LINK ESTABLISHING PROCEDURE IS SAME AS THAT FOR SIFCOM COMMON UNIT

FIG. 715

669260-272260

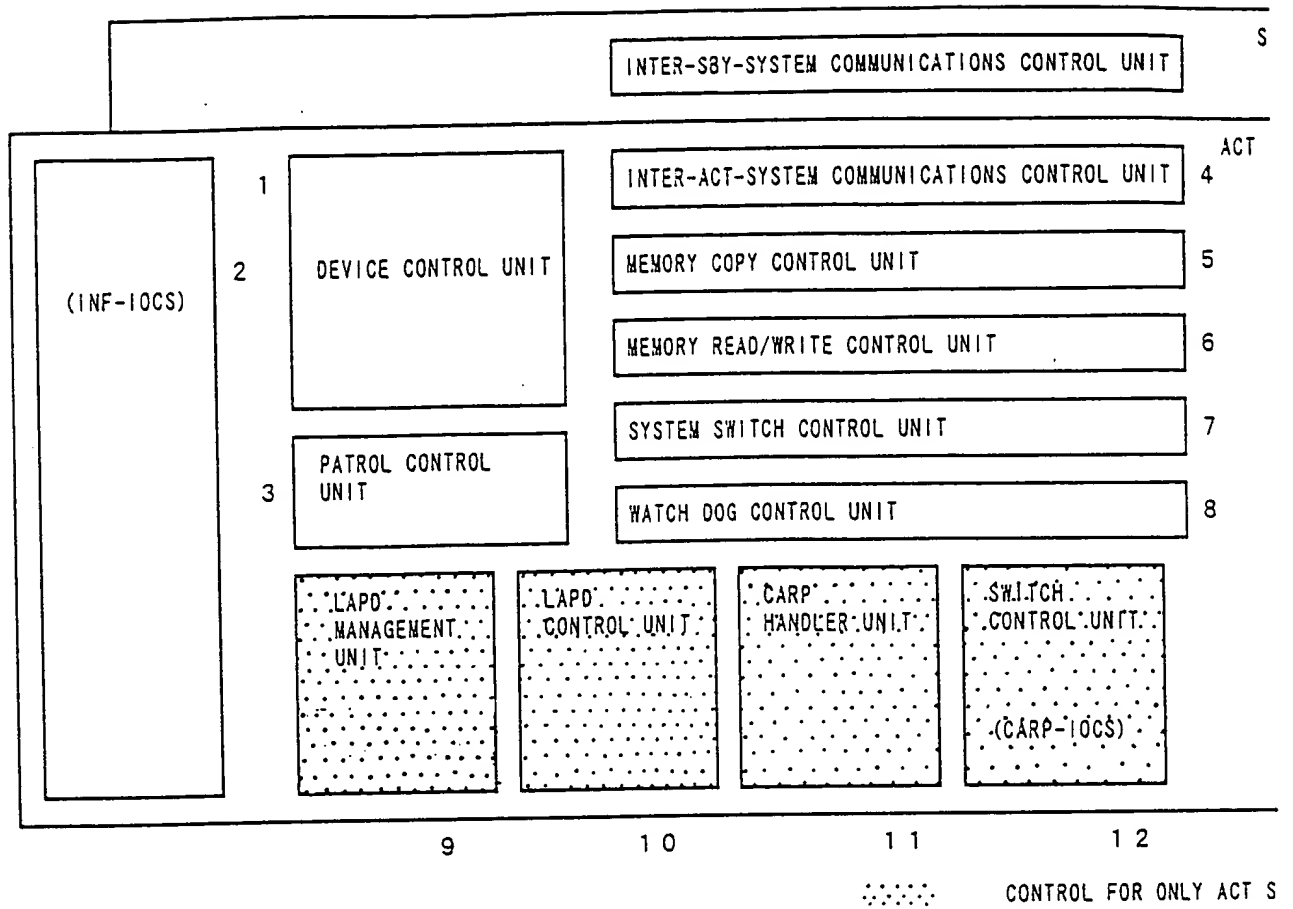


FIG. 716

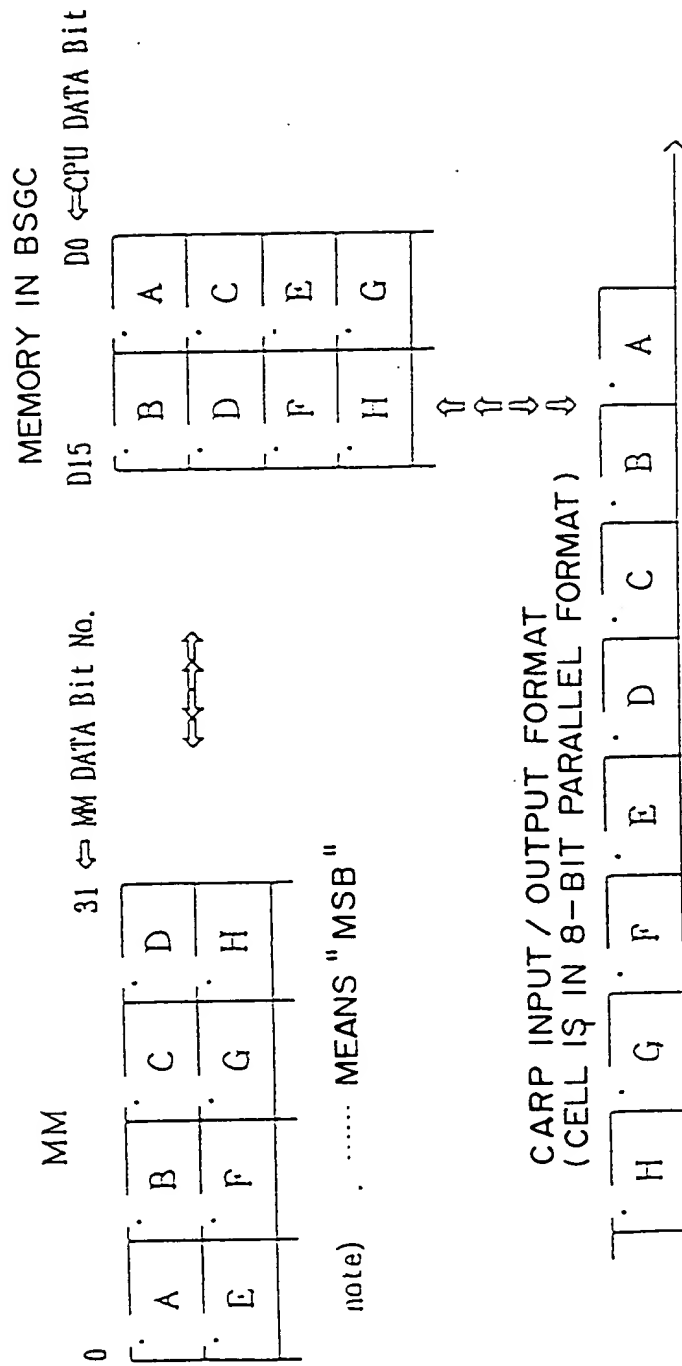


FIG. 718

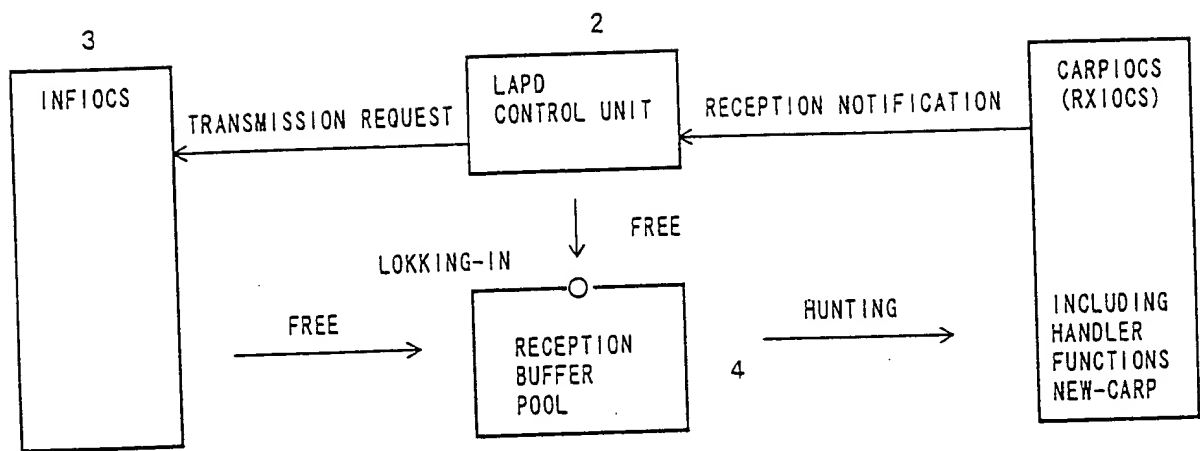


FIG. 719

NUMBER OF PROCESSED SIGNALS

200 MSG/S
* (35KBHCA)

FIRST, SECOND, AND THIRD RESTRICTIONS ARE ABNORMAL PROCESSES.

*) 5 MSG X 2 T/R X 2 O/T = 20 MSG FOR 1 CALL
100 KBHCA = 556 MSG/S NUMBER OF CALLS PER BCPR
(20 MSG/CALL X 100,000 BHCA ÷ 3600 SEC)
PROCESSES OF 200 MSG/S PER BSGC

BSGC CPU USE RATE

FIG. 720

0		16		31	
COMMAND TYPE				COMMAND CODE	
D. C				D. C	
INF INITIAL INFORMATION SETTING TABLE SIZE					
INF INITIAL INFORMATION SETTING TABLE ADDRESS					

INITIAL-
ZATION
COMMAND

FIG. 721

SIG	UL	TAGC	COM	PATH
0/1	0	000	0	SIFSH#0 LINE0/SIGNALING
0/1	0	001	0	SIFSH#0 LINE1/SIGNALING
		1		1
0/1	0	111	0	SIFSH#0 LINE7/SIGNALING
0/1	1	000	0	SIFSH#1 LINE0/SIGNALING
0/1	1	001	0	SIFSH#1 LINE1/SIGNALING
		1		1
0/1	1	111	0	SIFSH#1 LINE7/SIGNALING
1	0	000	1	SIFSH#0 COM SIGNALING
1	1	000	1	SIFSH#1 COM SIGNALING

1

SIG	UL	TAGB	TAGC	COM	PATH
0/1	0	0	000	0	RMUXSH#0 LINE0 / SIGNALING
0/1	0	0	001	0	RMUXSH#0 LINE1 / SIGNALING
			}		}
0/1	0	0	111	0	RMUXSH#0 LINE7 / SIGNALING
0/1	1	0	000	0	RMUXSH#1 LINE0 / SIGNALING
0/1	1	0	001	0	RMUXSH#1 LINE1 / SIGNALING
			}		}
0/1	1	0	111	0	RMUXSH#1 LINE7 / SIGNALING
0/1	1	1	000	0	RMUXSH#2 LINE0 / SIGNALING
0/1	1	1	001	0	RMUXSH#2 LINE1 / SIGNALING
			}		}
0/1	1	1	111	0	RMUXSH#2 LINE7 / SIGNALING
1	0	0	000	1	RMUXSH#0 COM SIGNALING
1	1	0	000	1	RMUXSH#1 COM SIGNALING
1	1	1	000	1	RMUXSH#2 COM SIGNALING

1

SIG	ADS1 BLK	ADS1 SEL	
0	0 0 0	0 0 1 1	USER CELL TO DTC 0/LINE 0 USER CELL TO DTC 0/LINE 3
0	1 1 1	0 0 1 1	USER CELL TO DTC 7/LINE 0 USER CELL TO DTC 7/LINE 3
1	0 0 0	0 0 1 1	LAP CELL TO DTC 0/LINE 0 LAP CELL TO DTC 0/LINE 3
1	1 1 1	0 0 1 1	LAP CELL TO DTC 7/LINE 0 LAP CELL TO DTC 7/LINE 3

FIG. 724

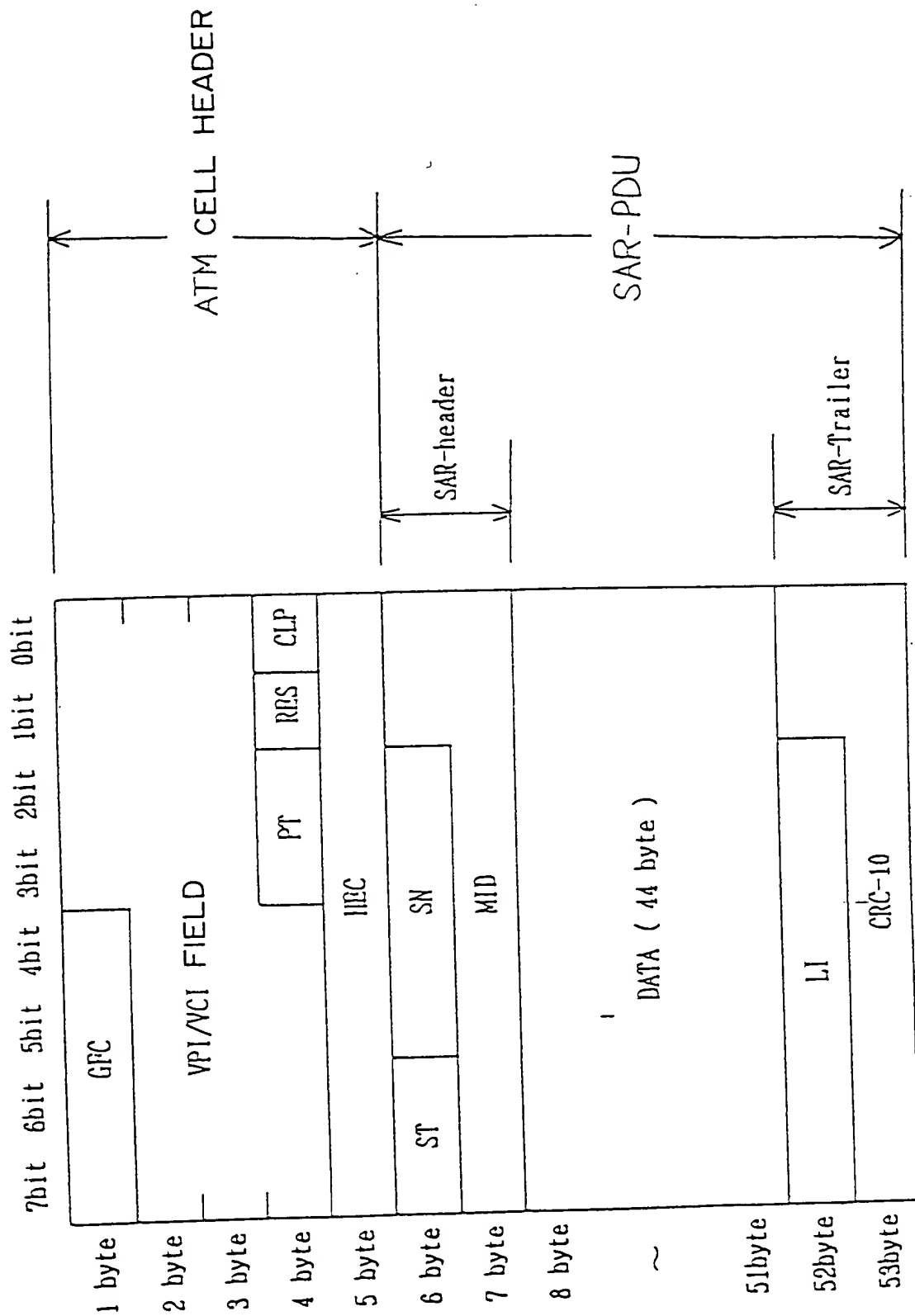


FIG. 726

32bit

1bit

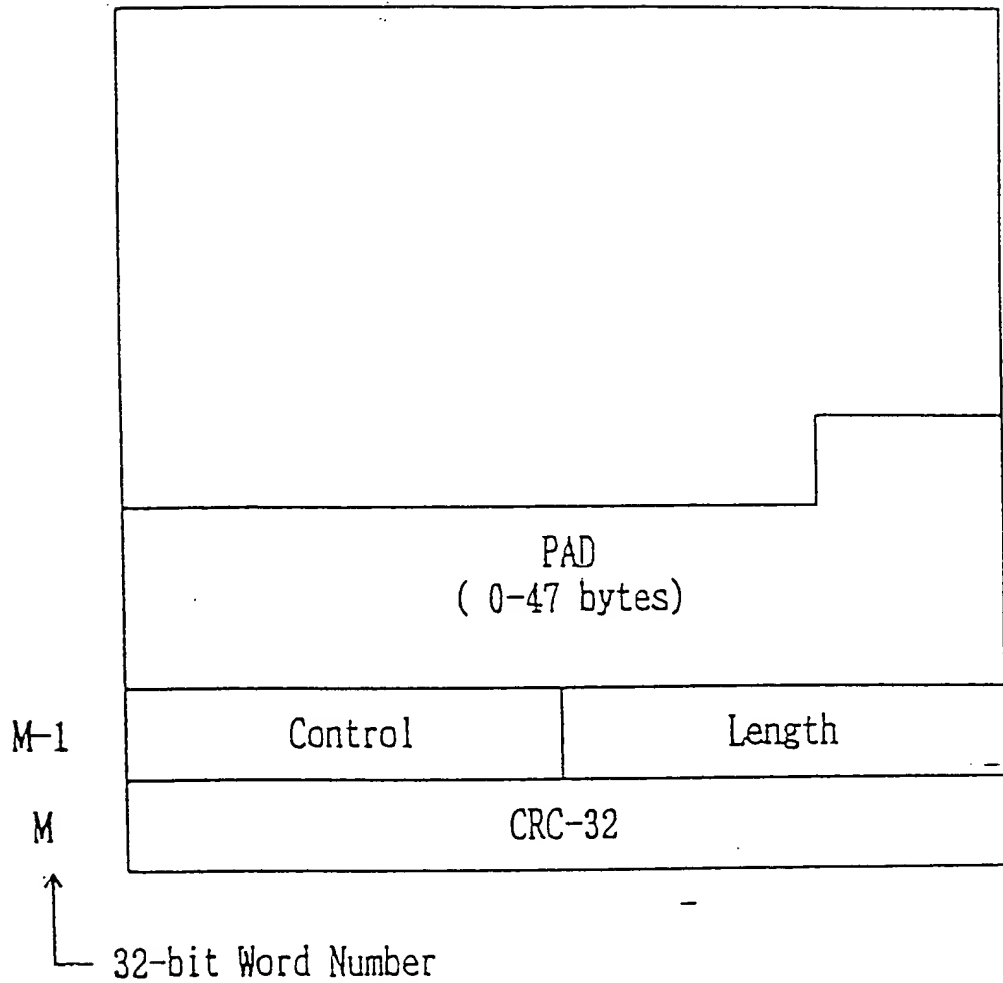


FIG. 727

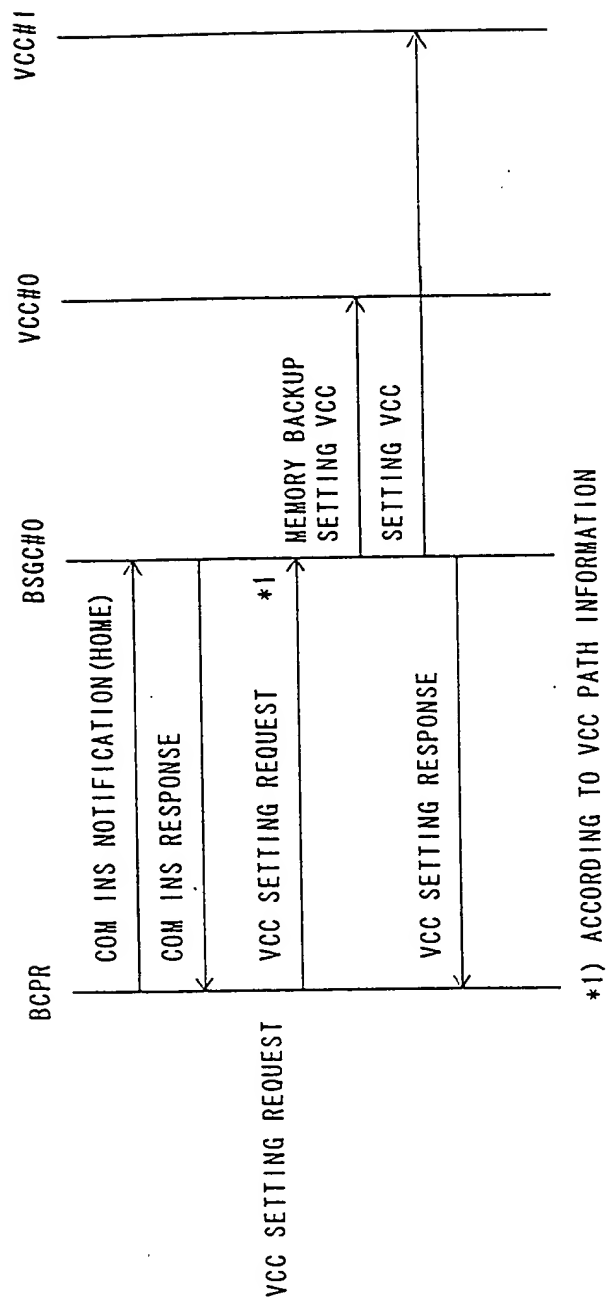
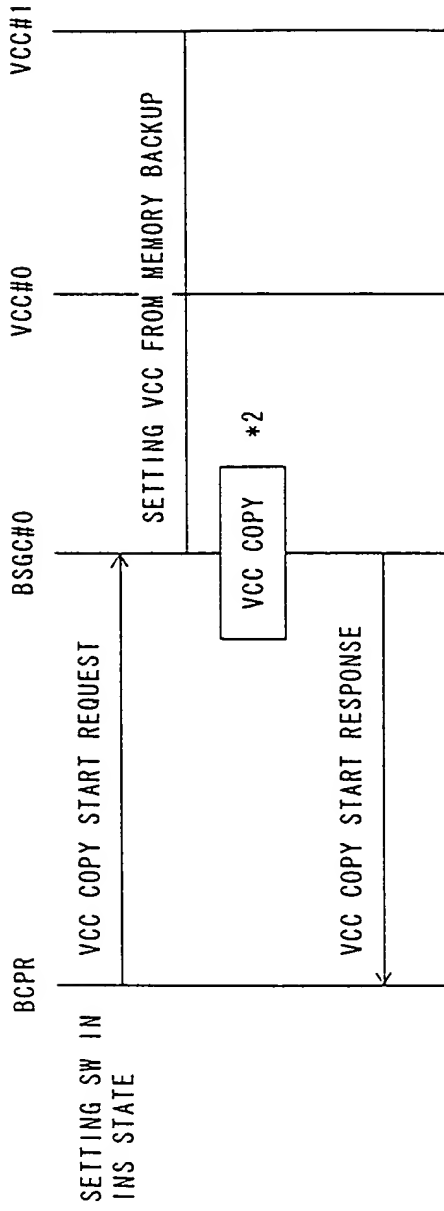
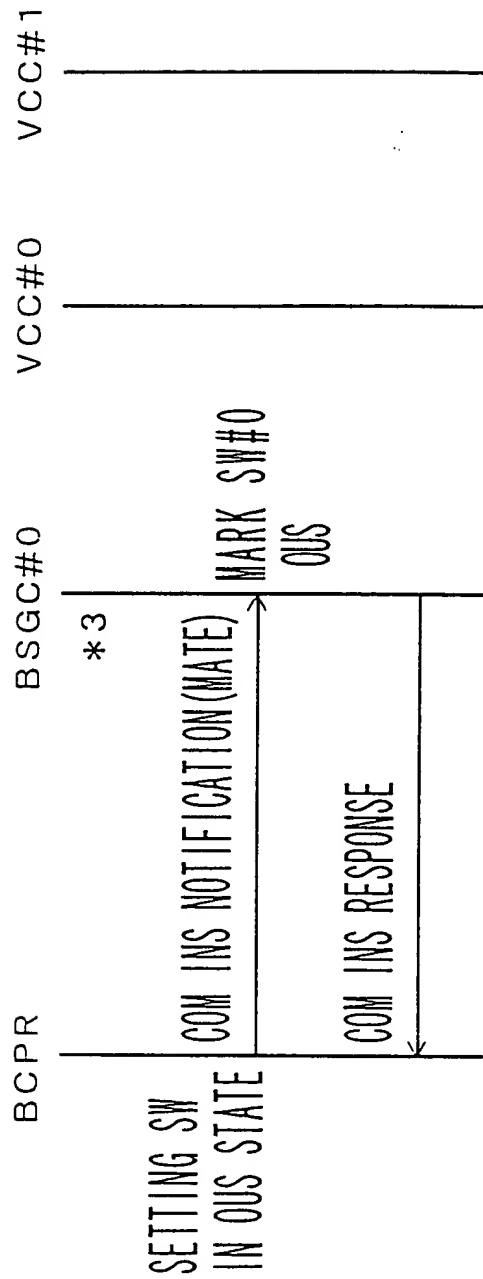


FIG. 728



*2) VCC CAN BE SET DURING VCC COPY PROCESS
AFTERWARDS, VCC IS WRITTEN IN BOTH SYSTEMS.

FIG. 729



*3) AFTERWARDS, VCC IS WRITTEN IN ONLY INS SYSTEM(#1)

FIG. 730

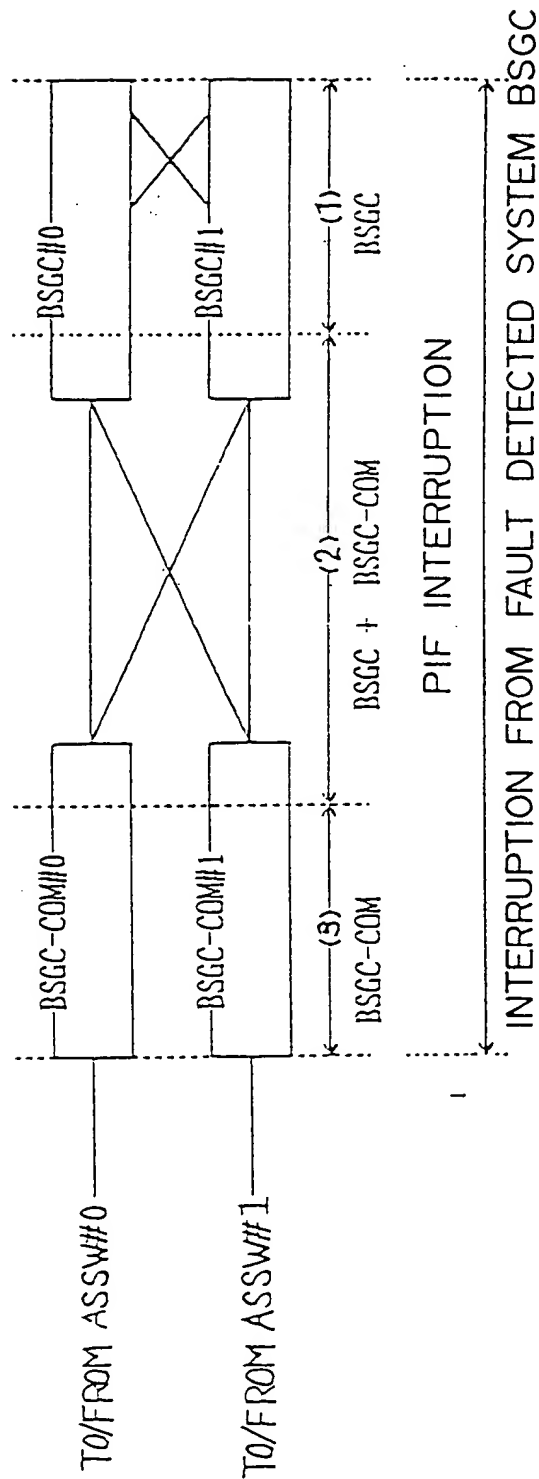
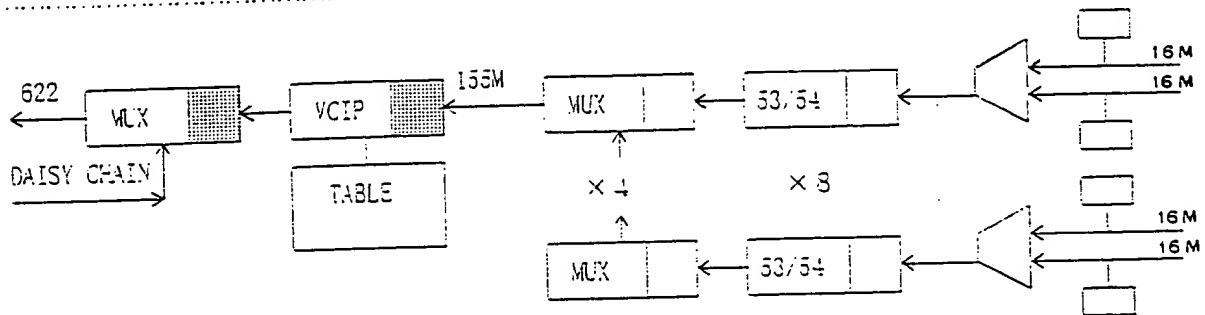
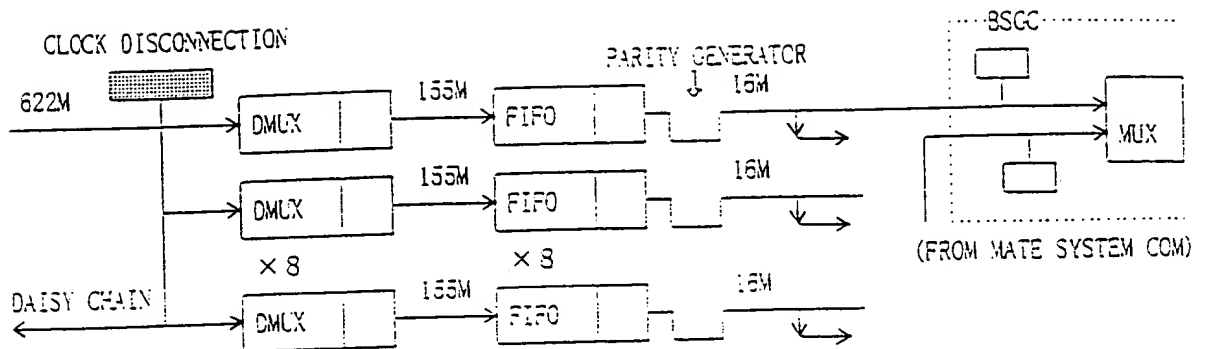




FIG. 731

0927243-03699
66920-ET2260



-  BSGC-PKG UNIT FAULT NOTIFICATION POINT
-  NOTIFICATION POINT FOR STARTING NUMBER BSGC-PKG
(FAULT POINT OF ONE PORTION OF COM UNIT)

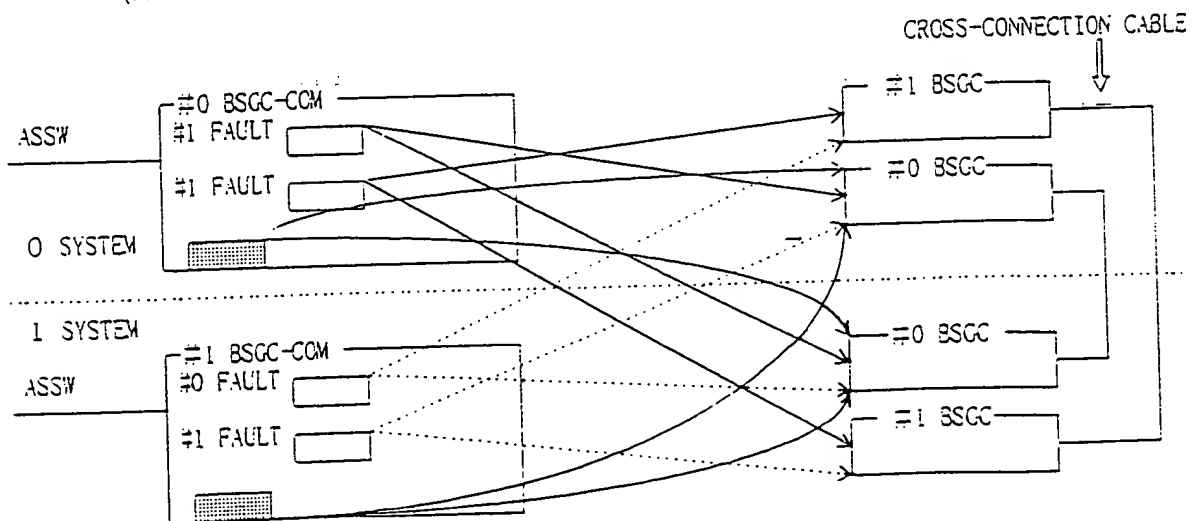


FIG. 732

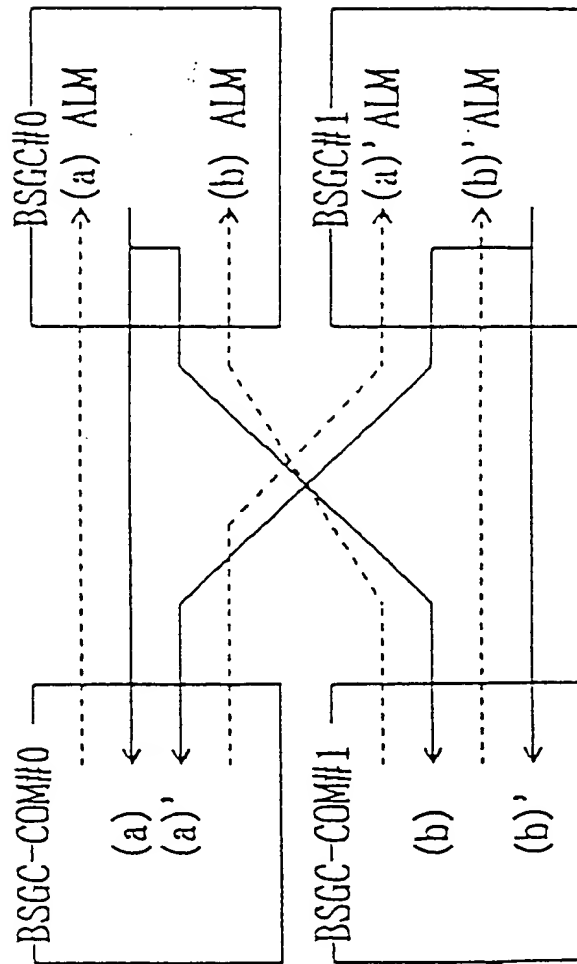


FIG. 733

FAULT POINT				AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTER- RUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN		BSGC#1SCN		# 0	# 1	# 0	# 1		
(a)	(b)	(a)'	(b)'						
1	0	0	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#1 → COM#0, COM#1 AVAILABLE
0	1	0	0	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#0 → COM#0, COM#1 AVAILABLE
0	0	1	0	OUS	ACT	ACT/SBY	NO AMENDMENT	BSGC#1	BSGC#1 → COM#0, COM#1 AVAILABLE
0	0	0	1	ACT	OUS	ACT/SBY	NO AMENDMENT	BSGC#1	BSGC#0 → COM#0, COM#1 AVAILABLE

FIG. 734

FAULT POINT			AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTER- RUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN	BSGC#1SCN		# 0	# 1	(NOTE 1) ACT/SBY	(NOTE 2) ACT/SBY		
(a)	(b)	(a)'	(b)'	# 1	# 0	# 1		
1	1	0	0	ACT	(NOTE 1) ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#1 → COM#0, COM#1 AVAILABLE
0	0	1	1	ACT	(NOTE 2) ACT/SBY	NO AMENDMENT	BSGC#0	BSGC#0 → COM#0, COM#1 AVAILABLE
1	0	1	0	(NOTE 3) ACT/SBY NO AMENDMENT	OUS	ACT	BSGC#0 BSGC#1	BSGC#0 → COM#1, BSGC#1 → COM#1, AVAILABLE
0	1	0	1	(NOTE 4) ACT/SBY NO AMENDMENT	ACT	OUS	BSGC#0 BSGC#1	BSGC#0 → COM#0, BSGC#1 → COM#0, AVAILABLE

FIG. 735

CASE-2

(a) — FAULT IN BSGC#0 (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
OUS	ACT	ACT	OUS	

BSGC-COM-PKG=XXXXXX

CASE-3

(a) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ AFTER SWITCHING BSGC-COM xxxxx-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
OUS	ACT	ACT	OUS	

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 736

CASE-1

(a)' — FAULT IN BSGC-COM#0, (b)' — FAULT IN BSGC#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
ACT	OUS	OUS	ACT	

BSGC-COM-PKG=XXXXXX

CASE-3

(a) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ AFTER SWITCHING BSGC-COM XXXXX-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
ACT	OUS	OUS	ACT	

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

CASE-2

(a)' — FAULT IN BSGC#1 (b)' — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
ACT	OUS	ACT	OUS	

BSGC-COM-PKG=XXXXXX

⇒ AFTER SWITCHING
BSGC-COM
XXXXX-PKG
AND CONFIRMING
NORMALITY ;

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ AFTER SWITCHING BSGC-COM XXXXX-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
ACT	OUS	ACT	OUS	

FIG. 737

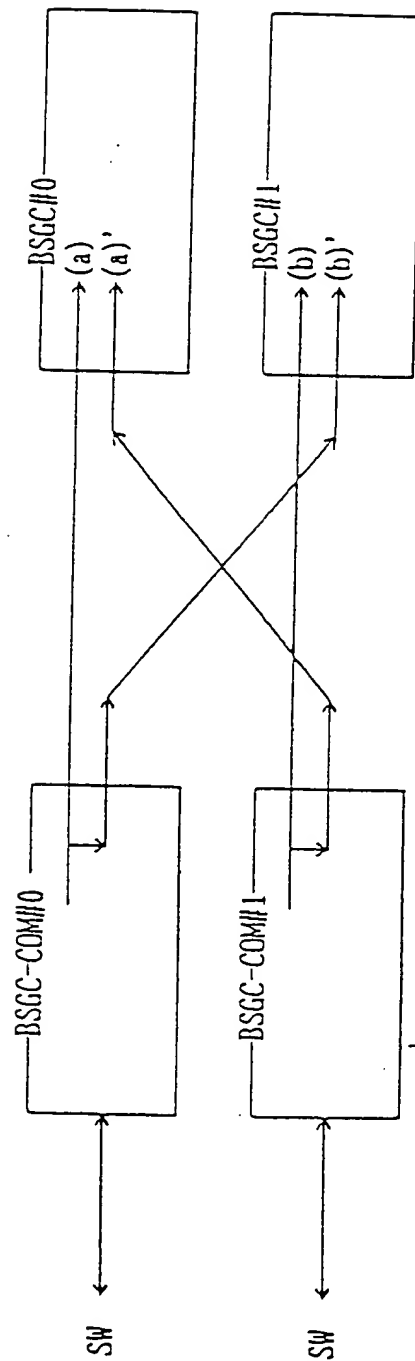


FIG. 738

FAULT POINT			AFTER-FAULT STATE OF BSGC SYSTEM		AFTER-FAULT STATE OF BSGC-COM SYSTEM		INTER- RUPTED BSGC SYSTEM	REMARKS
BSGC#0SCN	(b)	(a)'	(b)'	#0	#1	#0	#1	
1	0	0	0	OUS	ACT	ACT/SBY ↓ OUS	NO AMENDMENT	BSGC#0 DIAGNOSTICS EXECUTED : FORFLOWING STATE IS ENTERED WHEN N. G. IS SPECIFIED FOR BSGC-COM #0 WHEN N. G. IS SPECIFIED FOR BSGC#0, BSGC#0 IS MAINTAINED ONLY.
				SBY	ACT	↓ OUS	ACT	BSGC-COM#0 MAINTENANCE
0	1	0	0	ACT	OUS	ACT/SBY ↓ OUS	NO AMENDMENT	BSGC#1 DIAGNOSTICS EXECUTED : FORFLOWING STATE IS ENTERED WHEN N. G. IS SPECIFIED FOR BSGC-COM #0 WHEN N. G. IS SPECIFIED FOR BSGC#1, BSGC#1 IS MAINTAINED ONLY.
				ACT	SBY	↓ OUS	ACT	BSGC-COM#0 MAINTENANCE
0	0	1	0	OUS	ACT	ACT/SBY ↓ OUS	NO AMENDMENT	BSGC#0 DIAGNOSTICS EXECUTED : FORFLOWING STATE IS ENTERED WHEN N. G. IS SPECIFIED FOR BSGC-COM #1 WHEN N. G. IS SPECIFIED FOR BSGC#0, BSGC#0 IS MAINTAINED ONLY.
				SBY	ACT	↓ ACT	OUS	BSGC-COM#1 MAINTENANCE
0	0	0	1	ACT	OUS	ACT/SBY ↓ ACT	NO AMENDMENT	BSGC#1 DIAGNOSTICS EXECUTED : FORFLOWING STATE IS ENTERED WHEN N. G. IS SPECIFIED FOR BSGC-COM #1 WHEN N. G. IS SPECIFIED FOR BSGC#1, BSGC#1 IS MAINTAINED ONLY.
				ACT	SBY	↓ ACT	OUS	BSGC-COM#1 MAINTENANCE

FAULT POINT			AFTER-FAULT STATE OF BSGC SYSTEM				INTERRUPTED BSGC SYSTEM	REMARKS
BSGC#OSCN	BSGC#ISCN		#0	#1	#0	#1		
1	(b) 1	(a) 0	(NOTE1) ACT/SBY	NO AMENDMENT	OUS	ACT	BSGCH0 BSGCH1	BSGCH0 → COMH1 BSGCH1 → COMH1 AVAILABLE AVAILABLE
0	(b) 0	(a) 1	(NOTE2) ACT/SBY	NO AMENDMENT	ACT	OUS	BSGCH0 BSGCH1	BSGCH0 → COMH0 BSGCH1 → COMH0 AVAILABLE AVAILABLE
1	(b) 0	(a) 1	OUS	ACT	(NOTE3) ACT/SBY	NO AMENDMENT	BSGCH0	BSGCH1 → COMH0, COMH1 AVAILABLE
0	(b) 1	(a) 1	ACT	OUS	(NOTE4) ACT/SBY	NO AMENDMENT	BSGCH1	BSGCH0 → COMH0, COMH1 AVAILABLE

FIG. 740

CASE-2

(a) — FAULT IN BSGC#0 (a)' — FAULT IN BSGC-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	ACT	OUS

⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE-1

(a) — FAULT IN BSGC-COM#0, (a)' — FAULT IN BSGC#0

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	OUS	ACT

⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.

BSGC-COM-PKG=XXXXXX

CASE-3

(a) — FAULT IN BSGC-COM#0, (a)' — FAULT IN BSG-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	OUS	ACT

⇒ AFTER SWITCHING COM#0 xxxxx-PKG AND CONFIRMING NORMALITY ;

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM	
#0	#1	#0	#1
OUS	ACT	ACT	OUS

⇒ AFTER SWITCHING COM#1 xxxxx-PKG AND CONFIRMING NORMALITY ;

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

FIG. 741

CASE-1

(b) — FAULT IN BSGC-COM#1, (b)' — FAULT IN BSGC#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
ACT	OUS	OUS	ACT	

BSGC-COM-PKG=XXXXXX

CASE-3

(b) — FAULT IN BSGC-COM#0, (b) — FAULT IN BSG-COM#1

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ AFTER SWITCHING COM#0 xxxxx-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
ACT	OUS	OUS	ACT	

RETURNING BSGC/BSGC-COM=SW TO MASTER/SLAVE.

CASE-2

(b) — FAULT IN BSGC#1 (b)' — FAULT IN BSGC-COM#0

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ SETTING SYSTEM AS MASTER/SLAVE AFTER SWITCHING BSGC/COM-PKG AND CONFIRMING NORMALITY.
#0	#1	#0	#1	
ACT	OUS	ACT	OUS	

BSGC-COM-PKG=XXXXXX

AFTER-DIAGNOSTICS STATE OF BSGC SYSTEM		AFTER-DIAGNOSTICS STATE OF BSGC-COM SYSTEM		⇒ AFTER SWITCHING COM#1 xxxxx-PKG AND CONFIRMING NORMALITY ;
#0	#1	#0	#1	
ACT	OUS	ACT	OUS	

FIG. 742

No	CONTENTS	CC INTERRUPTION	F I R M INTERRUPTION	MSCN- BIT	FAULT CORRECTING PROCESS	REMARKS
1	INF DMA ACCESS ERROR 1	EXISTING	EXISTING	2 8	RETRIAL PROCESS FAULT IF NG	ANSWER SBER1- BIT=1. AT DMA-TRANSFER, INF T PARITY CHECKER GENERATES N. G. IN BSGC → PFT DIRECTION.
2	INF DMA ACCESS ERROR 2	EXISTING	EXISTING	2 7	RETRIAL PROCESS FAULT IF NG	ANSWER SBER2-BIT=1. AT DMA-TRANSFER, INF T BECOMES BERR THROUGH ACCESS TO TOXBUS AND DMA ADDRESS GUARD ERROR OCCURS.
3	INF DMA PARITY ERROR	EXISTING	EXISTING	2 6	RETRIAL PROCESS FAULT IF NG	ERROR OCCURS IN PARITY CHECK OF ANSWER RECEPTION DATA.
4	INF DMA TIMEOVER	EXISTING	EXISTING	2 5	RETRIAL PROCESS FAULT IF NG	TIME MONITOR TIMER INDICATES "OVER" DURING PERIOD FROM DMA ACCESS TERMINATION TO ANSWER (NO ANSWER)
5	BSGC FAULT	EXISTING	EXISTING	2 3	SETTING AS OUS STATE SYSTEM SWITCH FOR ACT SYSTEM	BSGC FAULT ① WATCH DOG TIMER OVER ② DRAM PARITY N. G ③ WRITE PROTECT ERROR

FIG. 744

66960-02220

BIT	C O N T E N T S	
31	RESET COMPLETION INDICATOR	
30	(DON'T CARE)	
29	BSGC FAULT	(1)
28	DMA ACCESS ERROR 1 (OCCURRENCE OF ANSWER ER1)	(1)
27	DMA ACCESS ERROR 2 (OCCURRENCE OF ANSWER ER2)	(1)
26	DMA PARITY ERROR	(1)
25	DMA TIME OVER	(1)
24	HPAL : HOME BSGC-COM OBP FAULT	(3)
23	MPAL : MATE BSGC-COM OBP FAULT	(3)
22	MFAL : MATE FUSE ALARM (MATE SYSTEM HPT01A LOADED FUSE DISCONNECTION STATE)	(3)
21	HOME SYSTEM BSGC-COM FAULT-1 ☆VALID BIT FOR ONLY STARTING NUMBER BSGC	(3)
20	MATE SYSTEM BSGC-COM FAULT-1 ☆VALID BIT FOR ONLY STARTING NUMBER BSGC	(3)
19	HOME SYSTEM BSGC-COM FAULT-2	(3)
18	MATE SYSTEM BSGC-COM FAULT-2	(3)
17	(DON'T CARE)	
16	(DON'T CARE)	
15	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN HOME SYSTEM DATA PARITY N.G	(2)
14	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN HOME SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
13	(DON'T CARE)	
12	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM DATA PARITY N.G	(2)
11	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
10	(DON'T CARE)	
09	BSGC—BSGC-COM DETECTION FAULT AT BSGC IN HOME SYSTEM DATA PARITY N.G	(2)
08	BSGC—BSGC-COM DETECTION FAULT AT BSGC IN HOME SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
07	(DON'T CARE)	
06	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM DATA PARITY N.G	(2)
05	BSGC—BSGC-COM DETECTION FAULT AT BSGC-COM IN MATE SYSTEM CELL FRAME DISCONNECTION OR CLOCK DISCONNECTION	(2)
04	(DON'T CARE)	
03	(DON'T CARE)	
02	(DON'T CARE)	
01	(DON'T CARE)	
00	(DON'T CARE)	

☆---BITS 21-16 RECEIVES REPORT FROM STARTING NUMBER BSGC ONLY . OTHER BSGCs ARE "DON'T CARE".

FIG. 745

	BSGC FAULT	29	WATCH DOG TIME OVER, DRAM PARITY N.G, DRAM WRITE PROTECT ERR MUX LSI ALM FOR ACT/SBY-LINK MULTIPLEX, 54/53 CNV ALM, PIF RETRY OUT
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FIG. 746

NO	MSCN CONTENTS	BIT NO	DETAILED FACTOR LISTING
2	HOME-SYSTEM BSGC-COM FAULT-1	21	BIT INDICATING ONLY STARTING NUMBER BSGC ALL SUBSEQUENT BITS ARE FAULT BITS IN HOME SYSTEM BSGC-COM. 1)MUX UNIT IN HOME SYSTEM IS FAULTY.
3	MATE-SYSTEM BSGC-COM FAULT-1	20	BIT INDICATING ONLY STARTING NUMBER BSGC ALL SUBSEQUENT BITS ARE FAULT BITS IN MATE SYSTEM BSGC-COM. 1)MUX UNIT IN MATE SYSTEM IS FAULTY.
4	HOME-SYSTEM BSGC-COM FAULT-2	19	FAULT NOTIFICATION FROM EACH BSGC. ALL FAULT ARE FROM BSGC-COM IN HOME SYSTEM. EACH BSGC-PKG CORRESPONDING UNIT 1)MUX UNIT IN HOME SYSTEM IS FAULTY. 2)DMUX-VCC UNIT IN HOME SYSTEM IS FAULTY. 3)BSGC-CORRESPONDING MUX UNIT IN HOME SYSTEM IS FAULTY.
5	MATE-SYSTEM BSGC-COM FAULT-2	18	FAULT NOTIFICATION FROM EACH BSGC. ALL FAULTS ARE FROM BSGC-COM IN MATE SYSTEM. EACH BSGC-PKG CORRESPONDING UNIT 1)MUX UNIT IN MATE SYSTEM IS FAULTY. 2)DMUX-VCC UNIT IN MATE SYSTEM IS FAULTY. 3)BSGC-CORRESPONDING MUX UNIT IN MATE SYSTEM IS FAULTY.

FIG. 747

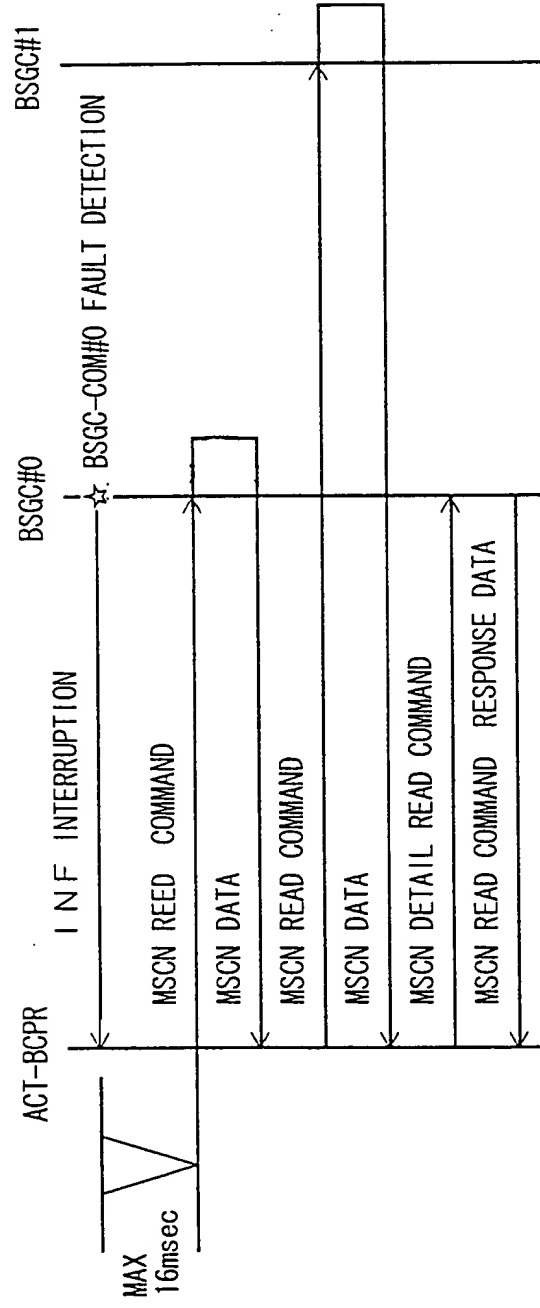


FIG. 748

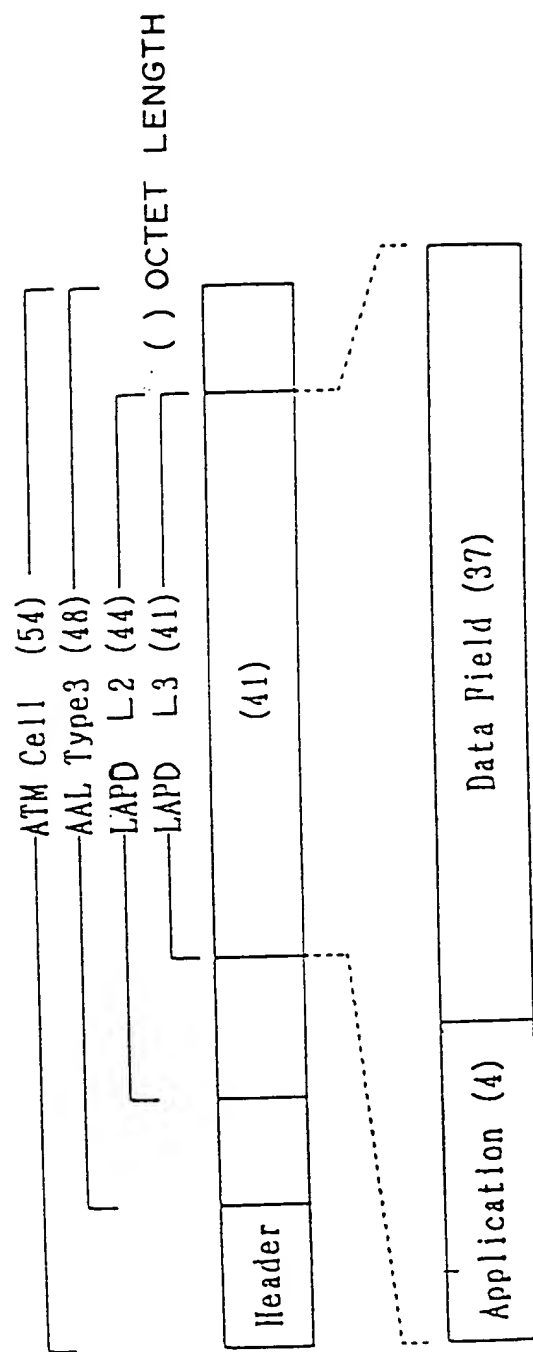
[illegible]

FIG. 749

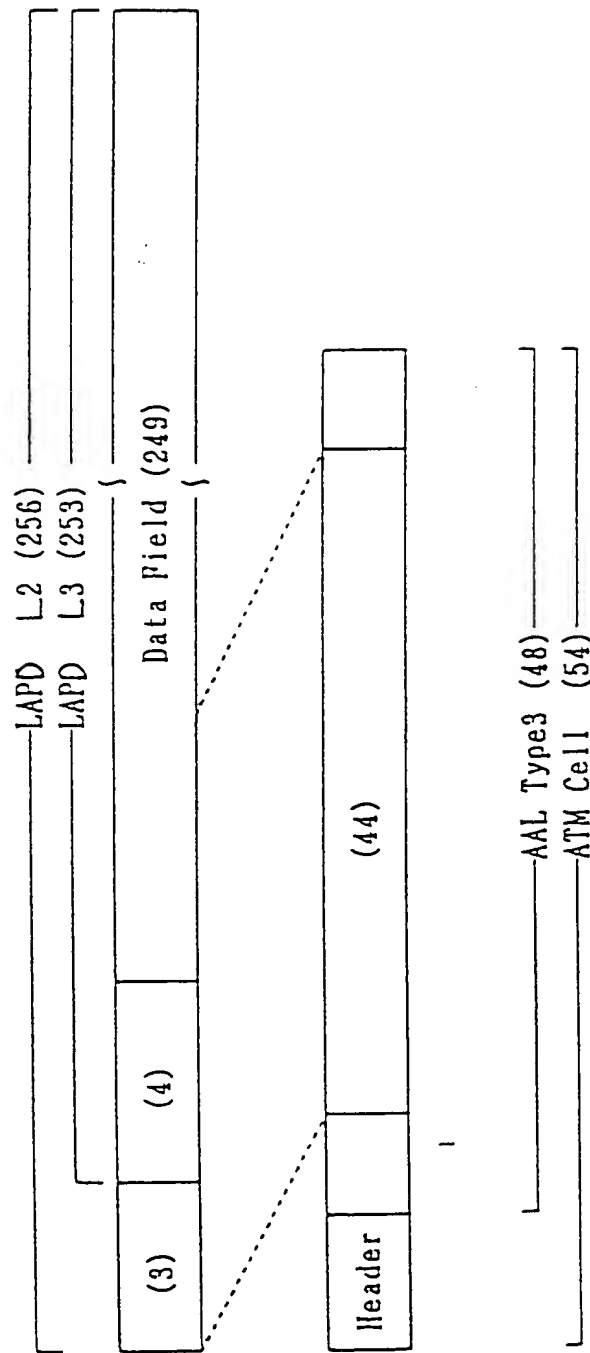


FIG. 750

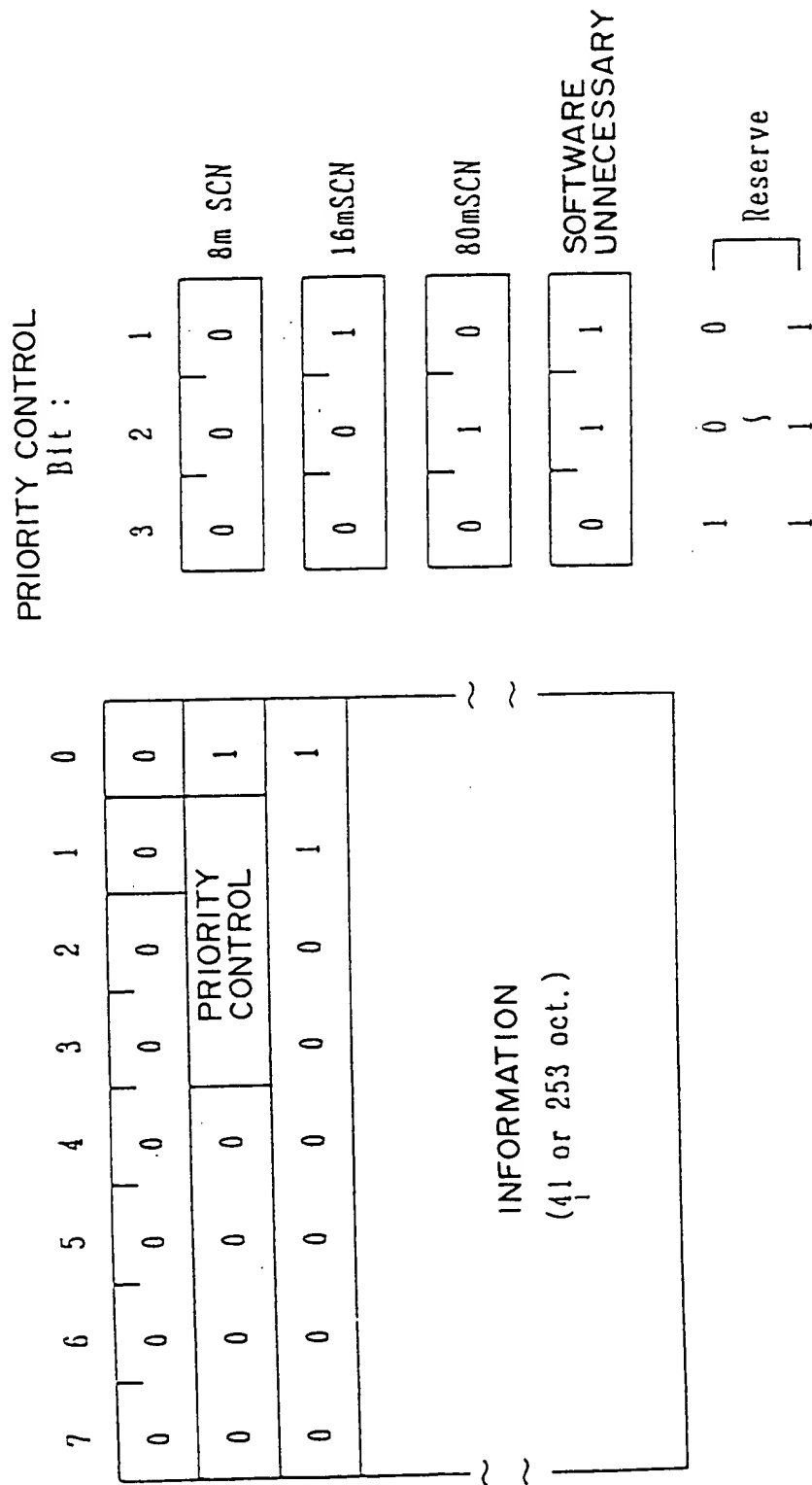
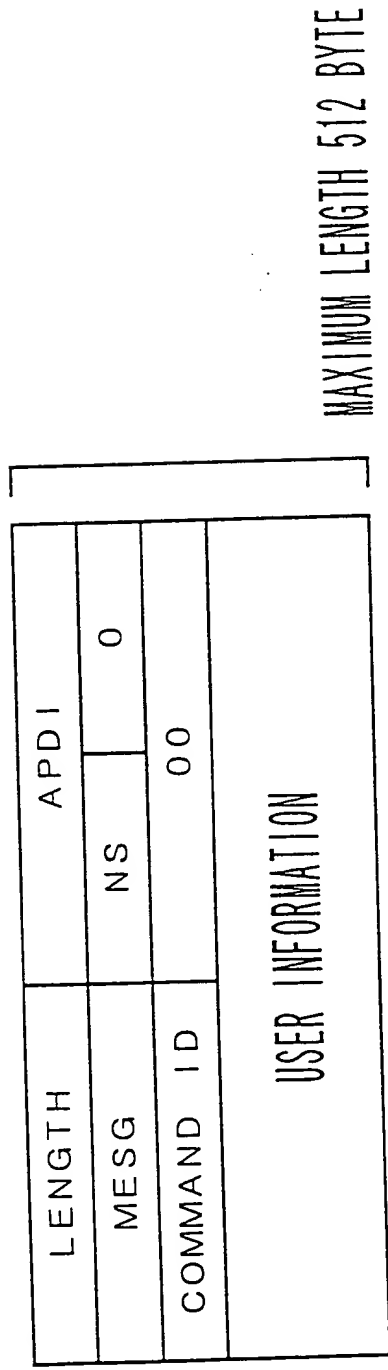


FIG. 751

Fig 6. 1. 3 UI FORMAT (SIFSH→BSGC)



THIS FORMAT IS DIFFERENT IN SIMPLE LAP AND FULL LAPD IN THE FOLLOWING POINTS.

1. MAXIMUM MESSAGE LENGTH IS 509 BYTES FOR SIMPLE LAP.
 2. NS FIELD IS FIXED AT 0 FOR FULL LAPD.
- APID/MSG VALUE IS CENTRALLY MANAGED BY SOFTWARE FOR ALL DEVICES.

000749.0000

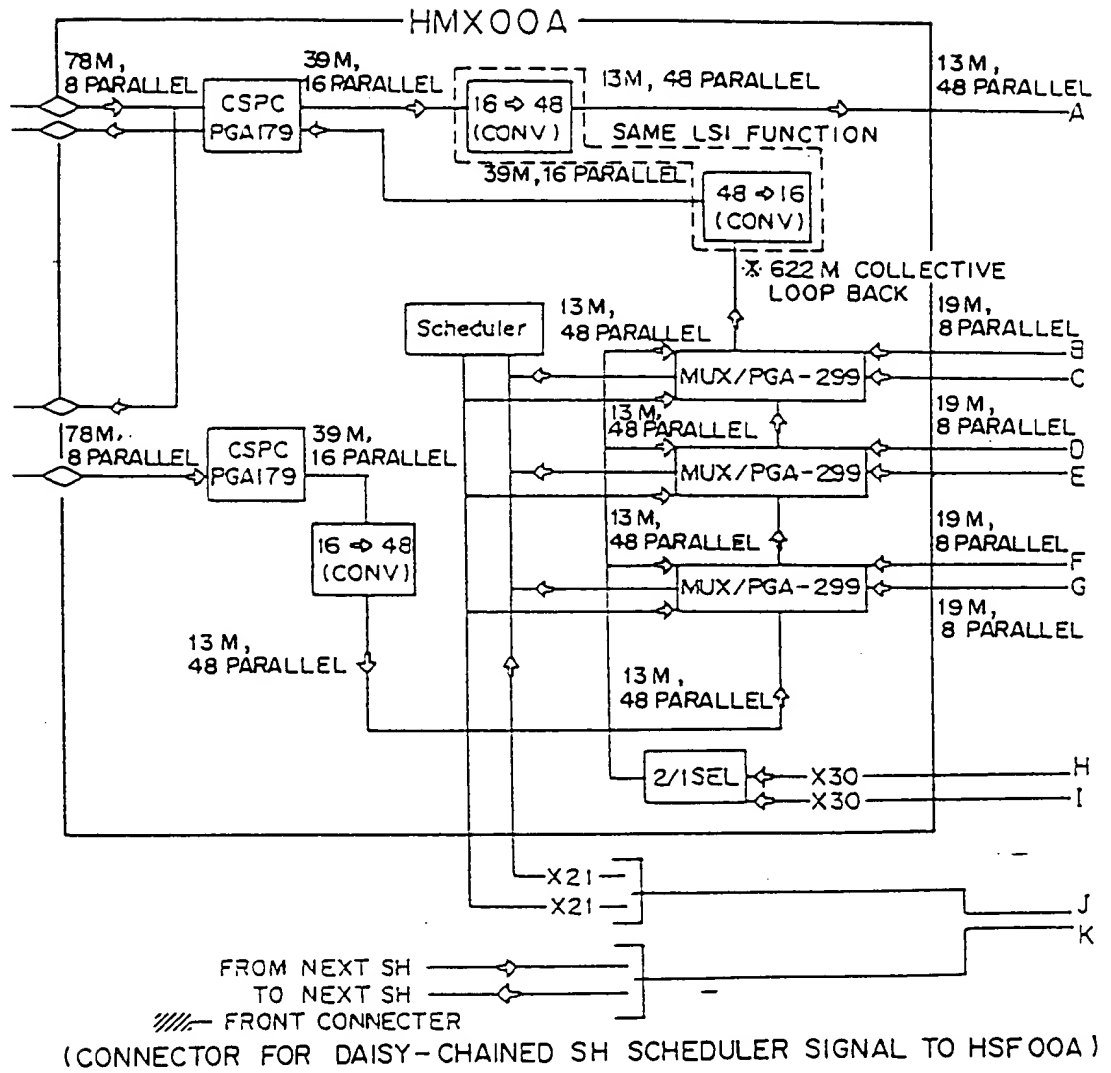


FIG. 753

[illegible]

FIG. 754

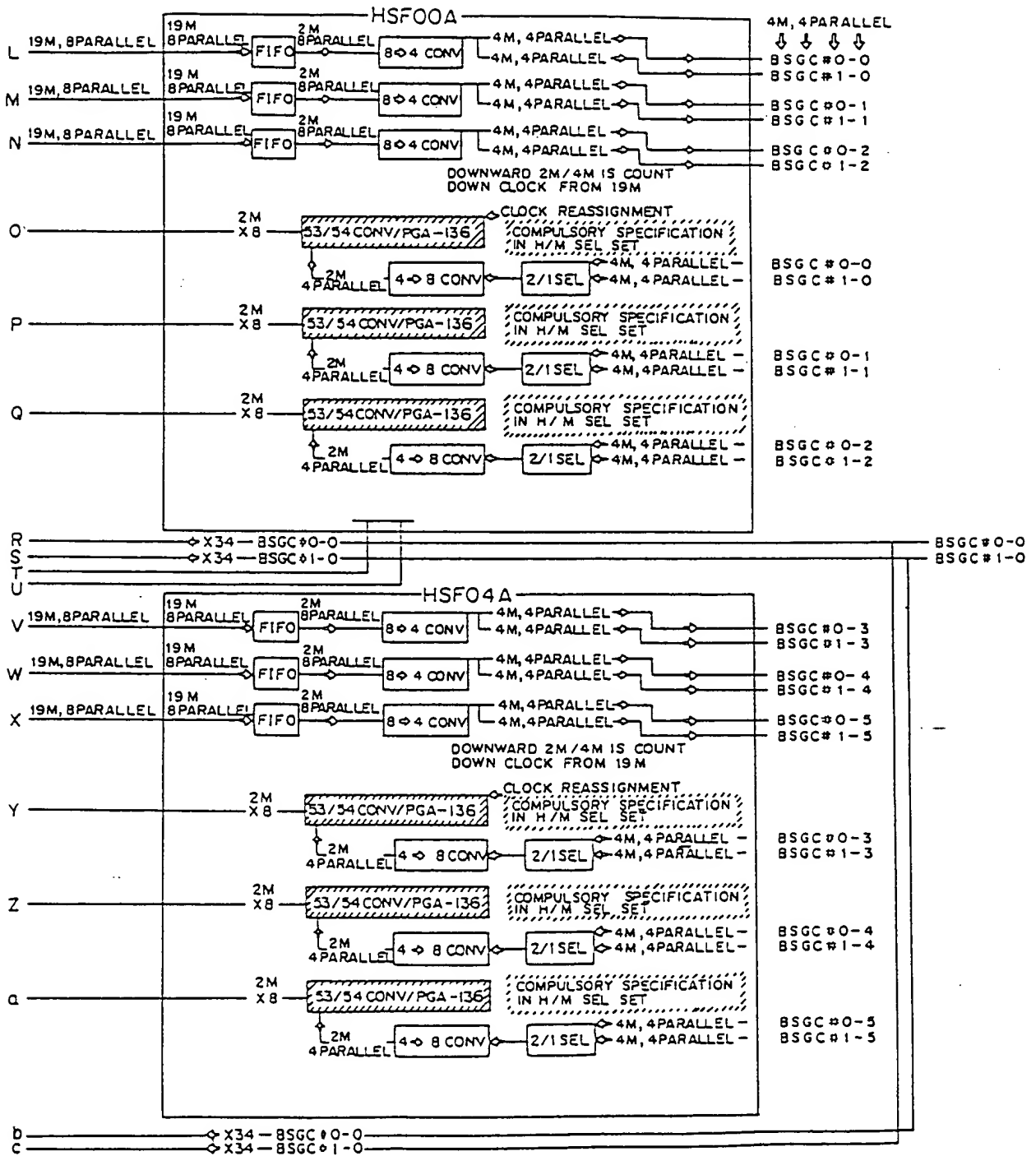


FIG. 755

HM000A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	CSPC	LEVEL IS CONVERTED BETWEEN ECL AND TTL OF 622M UP/DOWN DATA BY INTERFACING WITH ASSWSH. CONVERSION BETWEEN ECL LEVEL 8 BITS, 78M AND LEVEL 16 BITS, 39M.	MB222M607-CR-G
2	16 ⇄ 48 16 ⇄ 48 CONV (CSPCAD)	AMENDMENT IS MADE FROM 39M, 16 BITS TO 13M, 48 BITS OR FROM 13M, 48 BITS TO 39M, 16 BITS.	MBCG10572-607CR-G
3	SCHEDULER	MAIN FUNCTION OF SCHEDULER CAPABLE OF CELL MULTIPLEXING CONTROL FOR HOME SH 6BSGC AND LOWER SH 6BSGC IS REALIZED BY LCA.	64K EPROM LCA E76C-0024-0740 #6470G132
4	MUX	156M CELL 2 SYSTEM AND 622M HIGH SPEED CELL 1 SYSTEM CAN BE MULTIPLEXED. MULTIPLEXER.	MBCG31204-639CR-G
5	2/1 SEL	DATA, ADD. SELECTOR OF CONTROL LINE, AND ACT-BSGC ARE SELECTED FROM HOME/MATE SYSTEM STARTING NUMBER BSGC.	—

HMx01A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	DMUX	TAG IS DETECTED FROM CELL OF 622M. MATCHED WITH PREDETERMINED TAG INFORMATION, AND OUTPUT AS 156M CELL IF THEY MATCH. INPUT 13M. 48 PARALLEL \Rightarrow OUTPUT 19M. 8 PARALLEL	MBCG31204-638CR-G
2	SEL-N1 (a)	FOR CELL BY CELL LOOPBACK TO BSGC SPECIFYING LOOPBACK CELL FROM 0-BIT IN TAG.	MBCG21104-616ZFV
3	SEL-N1 (b)	FOR CELL BY CELL LOOPBACK TO ASSWSH SPECIFYING LOOPBACK CELL FROM 0-BIT IN TAG. VCI OF TEST CELL IS SPECIFIED BY SPECIFIC VRLUE. VCI=03FE, 03FF	MBCG21104-616ZFV
4	VCIP	REALIZING VCC FUNCTION. EXTERNALLY PROVIDING MEMORY AND CONVERTING CELL1-6 OCT DATA TO A VALUE WRITTEN TO MEMORY. AS SRAM, 64K \times 16BIT CMOS SRAM (TC551664J-20 : FROM TOSHIBA)	MBCG21503-609ZFV E76L-0025-0269## 5164-20
5	2/1 SEL	DATA, ADD, SELECTOR OF CONTROL LINE, AND ACT-BSGC ARE SELECTED FROM HOME/MATE SYSTEM STARTING NUMBER BSGC.	_____

FIG. 757

HSF00A/HSF04A

NO	FUNCTION BLOCK NAME	OUTLINE OF FUNCTIONS	MAIN LSI
1	FIFO	MEMORY FOR USE IN CONVERTING FROM 19M, 8 PARALLEL TO 1M, 8 PARALLEL	IDT 7206-20
2	8 \Rightarrow 4 CONV	CONVERTING PARALLEL WIDTH FROM 8 TO 4 TO INTERFACE WITH BSGC 2M, 8BIT \Rightarrow 4M, 4BIT	—
3	2/1 SEL (a)	BSGC-DIRECTION LOOPBACK SELECTOR	—
4	2/1 SEL (b)	HOME/MATE SYSTEM SELECTOR IN BSGC DIRECTION SELECTING ACT-BSGC	—
5	4 \Rightarrow 8 CONV	CONVERTING PARALLEL WIDTH FROM 4 TO 8 TO INTERFACE WITH BSGC 4M, 4BIT \Rightarrow 2M, 8BIT	—
6	53/54 CONV	CONVERTING CELL VALID OCT LENGTH 53OCT (CARP LSI SPECIFICATION) CONVERSION FOR 54OCT IN SW	MB632607-G (CELL FIFO)

FIG. 758

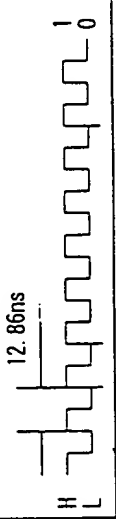
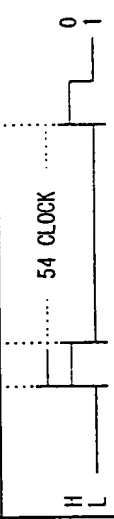
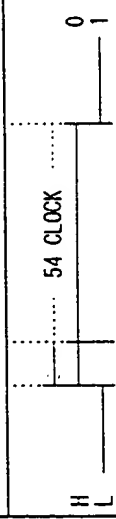
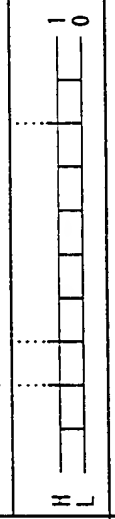
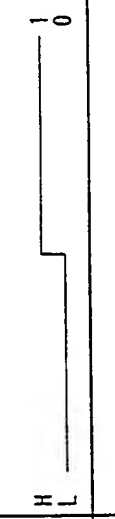
SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
IMX00A (A)	SWMDX (IMX03A)	OSICKX, Y	77.76MHz CLOCK	1	ECL BALANCED		50-CORE COAXIAL CABLE	
		OSICFX, Y	CELL FRAME SIGNAL	1				I CELL SLOT LEADING BIT "H"
		OSICEX, Y	CELL ENABLE SIGNAL	1				L: INVALID CELL SLOT H: VALID CELL SLOT
		OS100 ~7X, Y	CELL DATA OS107:MSB OS100:LSB	8				
		JSOU	IMPLEMEN- TATION SIGNAL	1	TTL UNBALANCED			L: IMPLEMENTED H: NON-IM- PLEMENTED
		OSIPTX, Y	CELL DATA PARITY	1	ECL BALANCED			

FIG. 759

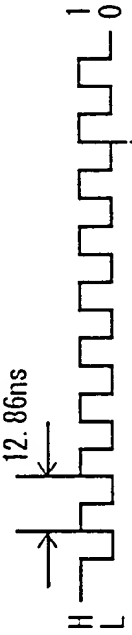
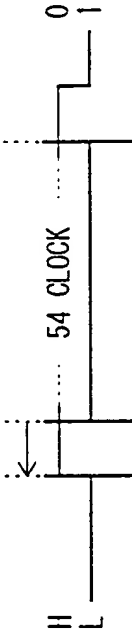
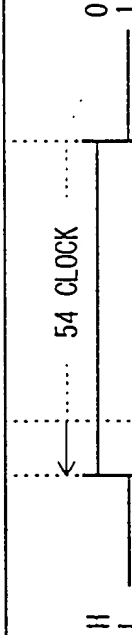
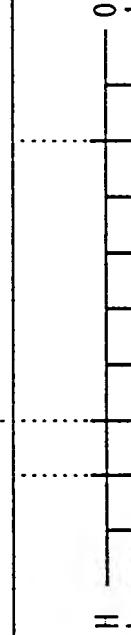


SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
SWMDX (IMX03A)	HMX00A (A)	ISICKX, Y	77.76MHz CLOCK	1	ECL BALANCED		50-CORE COAXIAL CABLE	
		ISICFX, Y	CELL FRAME SIGNAL	1				CELL SLOT LEADING BIT 'H'
		ISICEX, Y	CELL ENABLE SIGNAL	1				L: INVALID CELL SLOT H: VALID CELL SLOT
		ISI00-7X, Y	SELF DATA IMDX7 : MSB IMDX0 : LSB	8				
		ISIPTX, Y	CELL DATA PARITY 1	1				

FIG. 760

(a)

SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
HSF04A	SWTIF (HNC00A)		LOWER ORDER μ P FAULT SIGNAL	2	PSEUDO ECL BALANCED		12-PAIR AC BUS CABLE	L: VALID H: INVALID
			LOWER ORDER DEVICE IM-PLEMENTATION SIGNAL	2				L: IMPLEMENTED H: NON-IMPLEMENTED

(b)

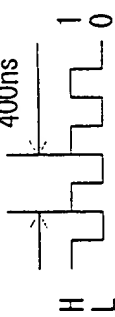

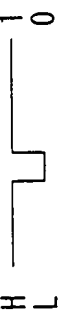
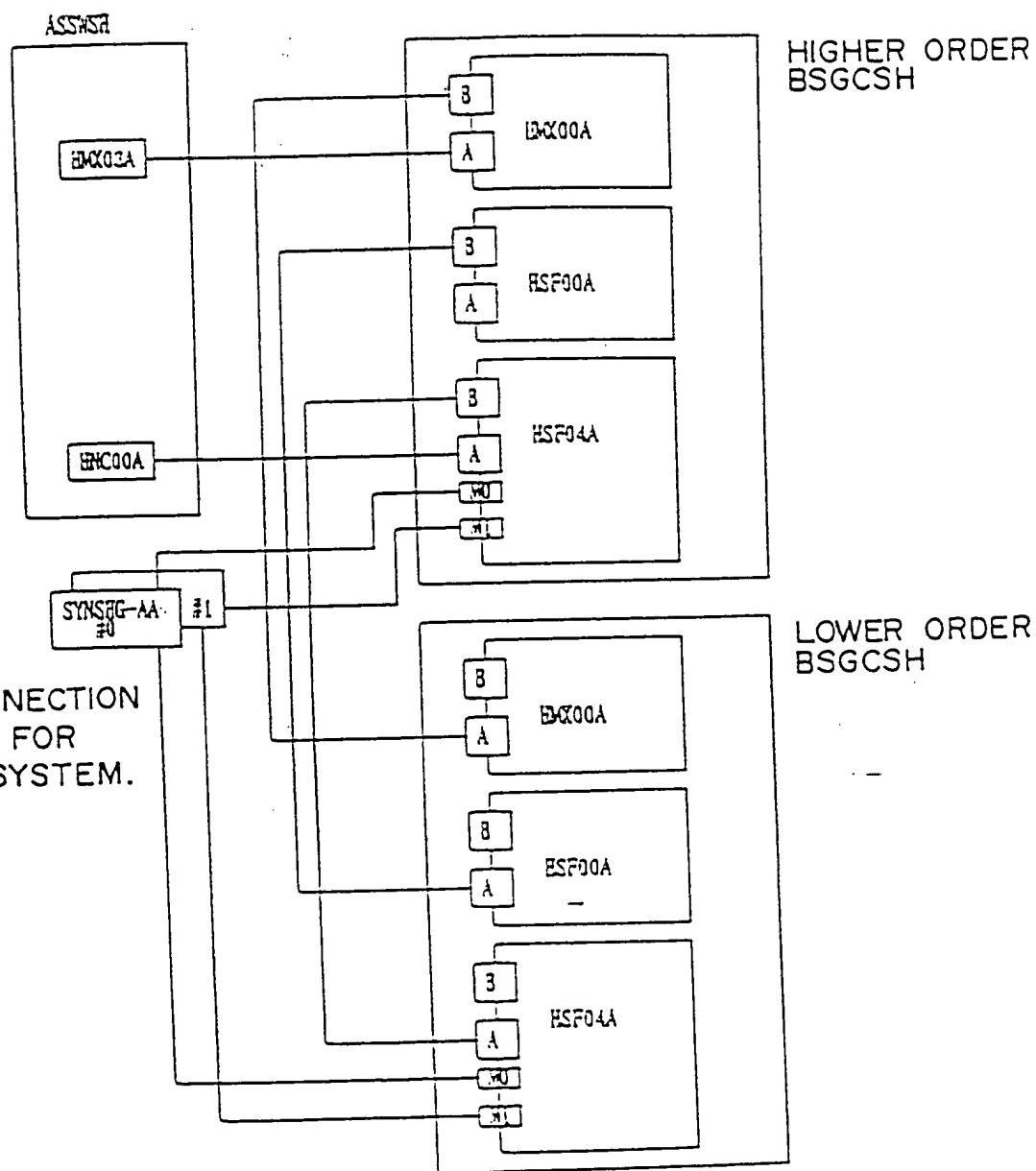
SENDING	RECEIVING	SIGNAL NAME	OUTLINE OF FUNCTION	NUMBER	TRANSMISSION FORMAT	SIGNAL FORMAT	CONNECTING METHOD	REMARKS
SWTIF (HNC00A)	HSF04A		SENDING/RECEIVING CLOCK	2	PSEUDO ECL BALANCED		12-PAIR AC BUS CABLE	
			LU SYSTEM SELECTION SIGNAL	2				L: 0 SYSTEM SELECT INSTRUCTION H: 1 SYSTEM SELECT INSTRUCTION
			LU SYSTEM SELECTION STROBE SIGNAL	2				L: VALID H: INVALID

FIG. 761

* THIS CONNECTION
IS MODE FOR
SINGLE SYSTEM.



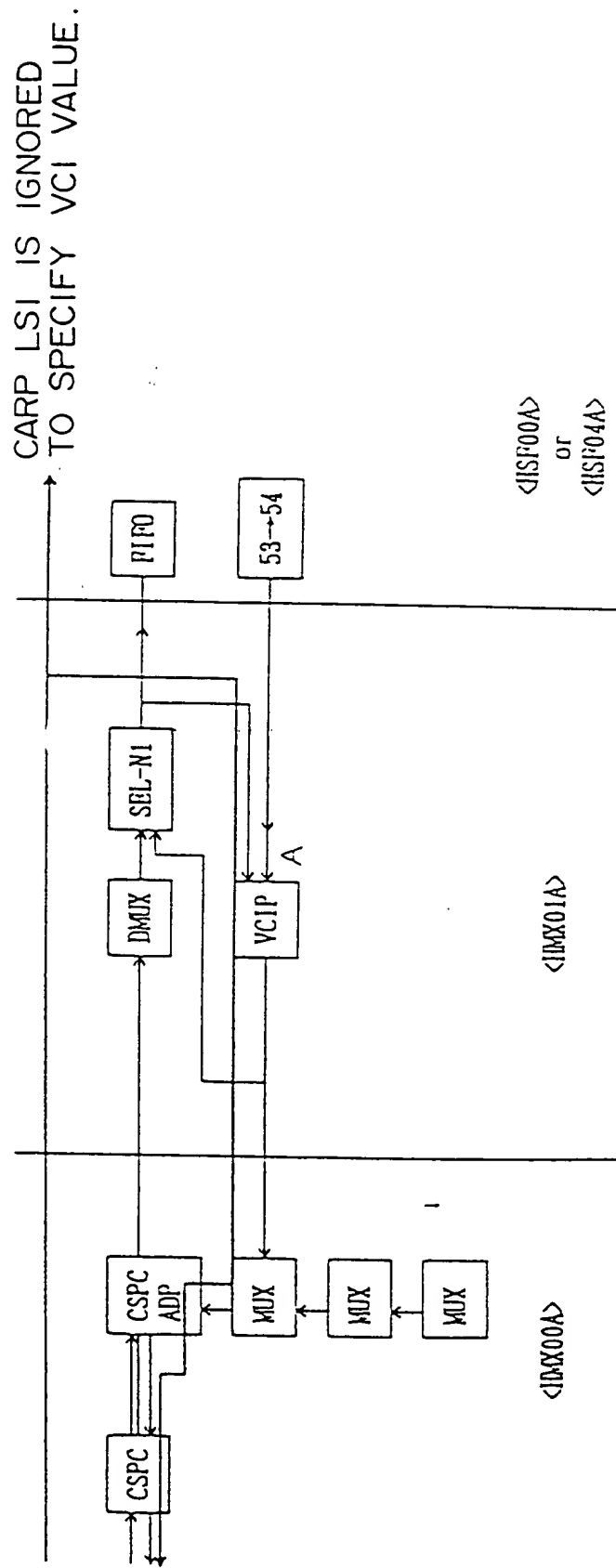


FIG. 763

SECRET

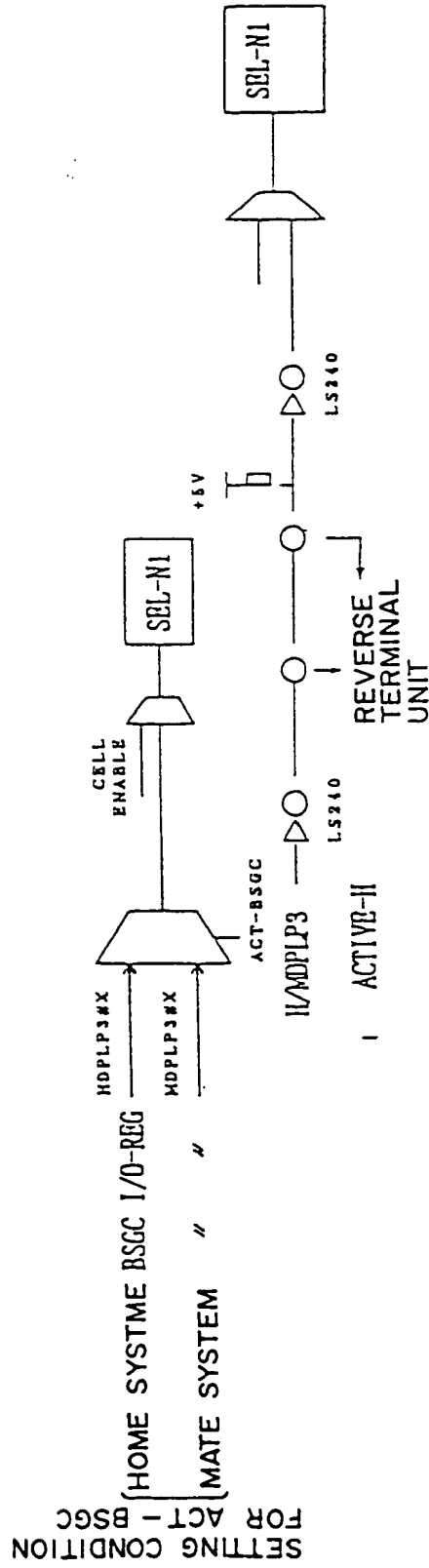


FIG. 764

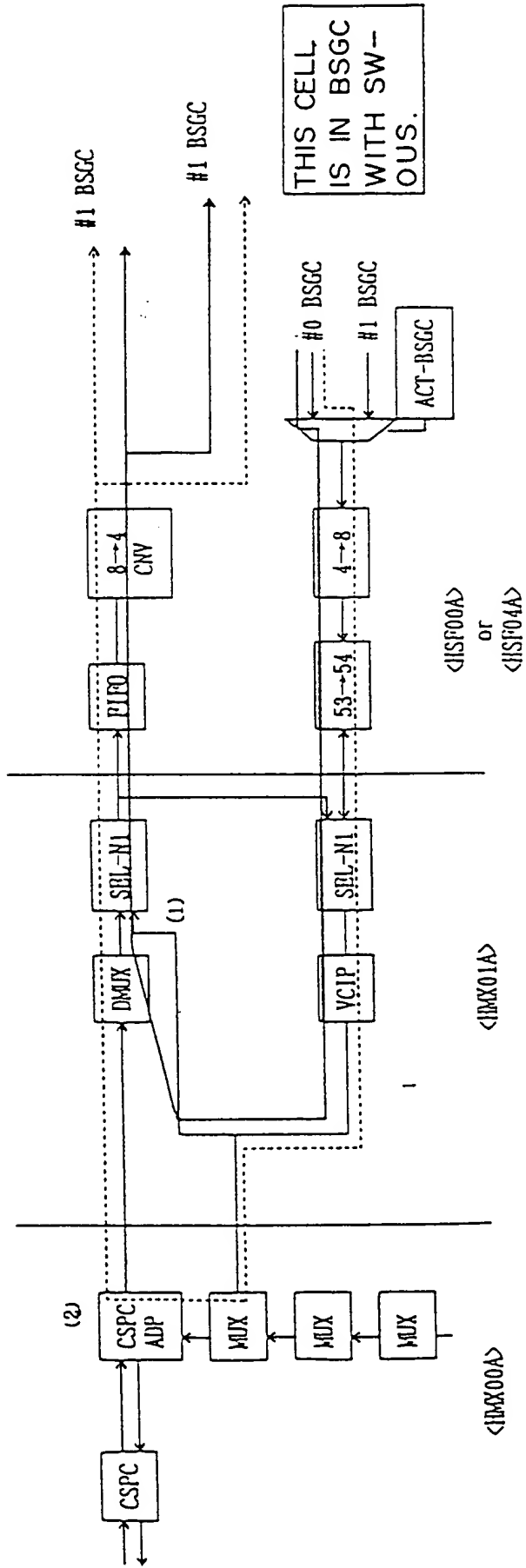


FIG. 765

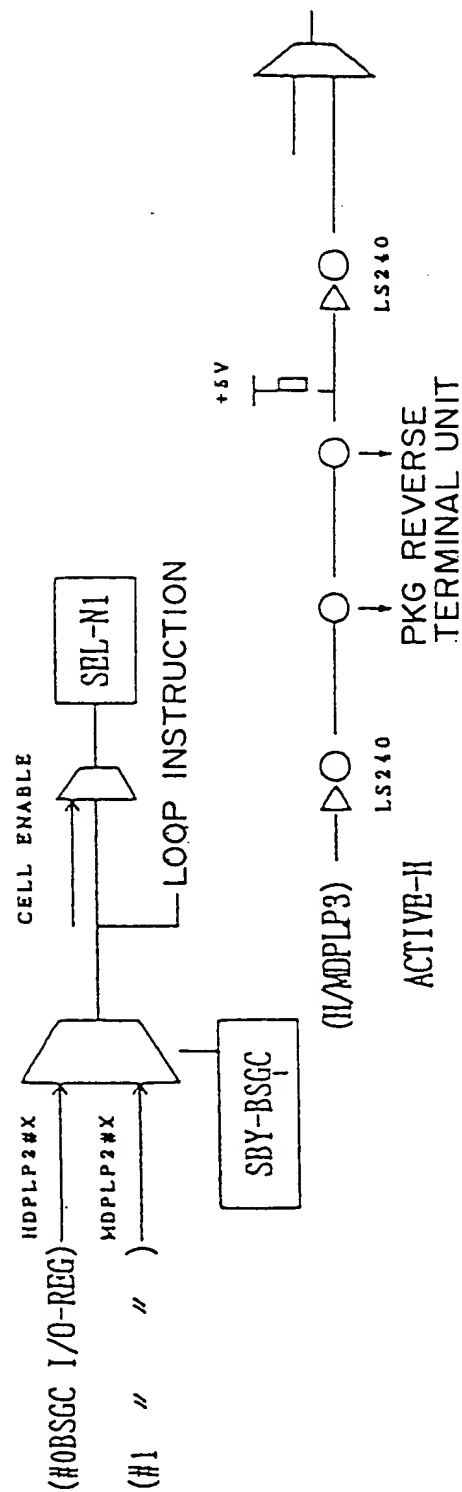


FIG. 766

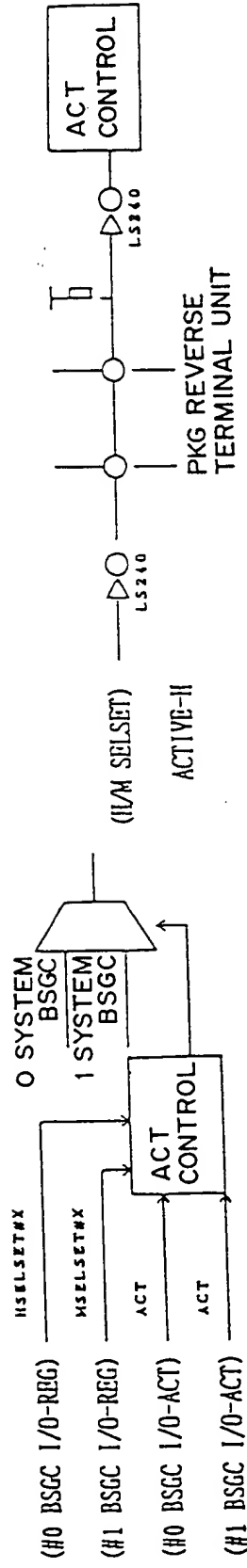


FIG. 767

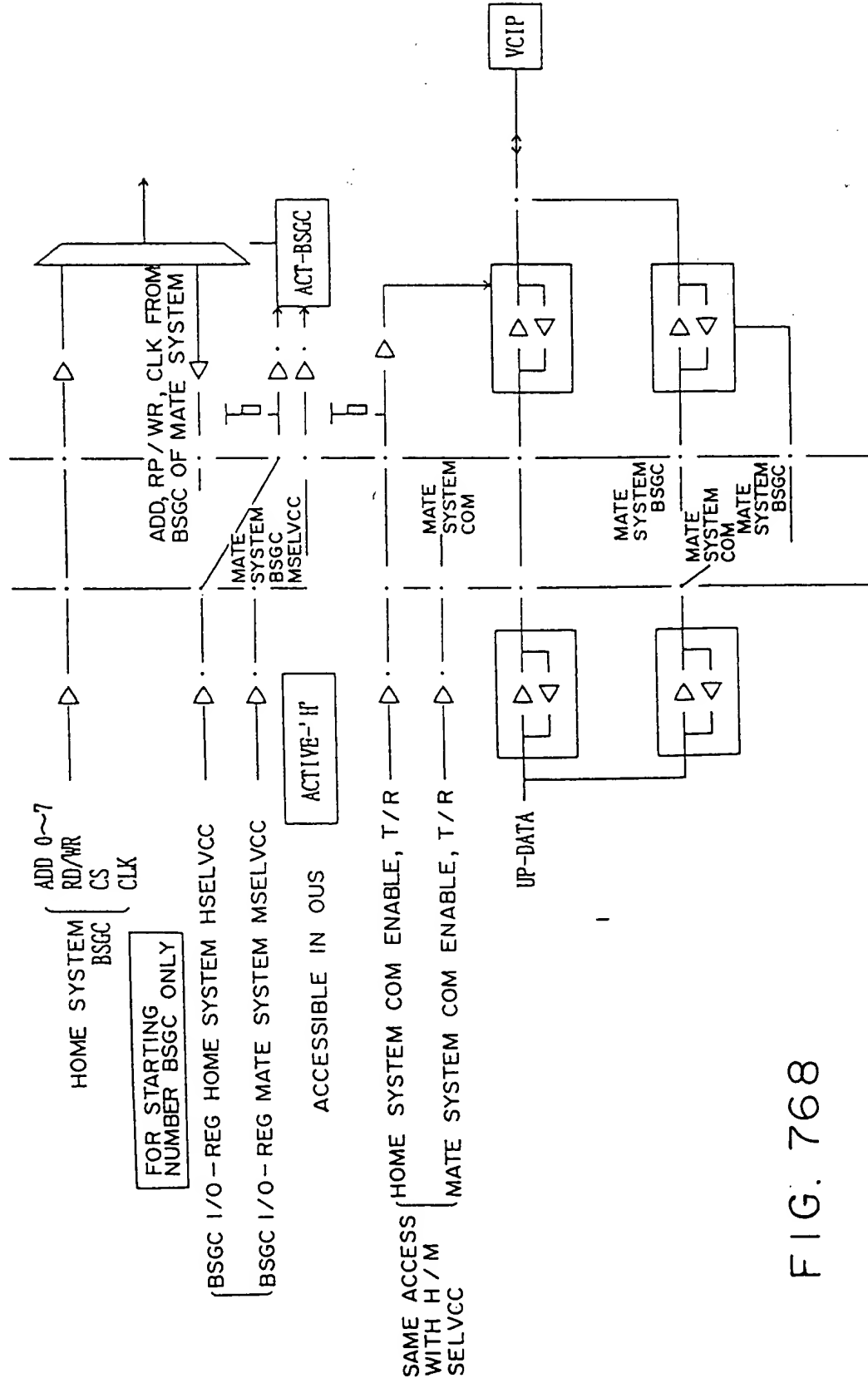


FIG. 768

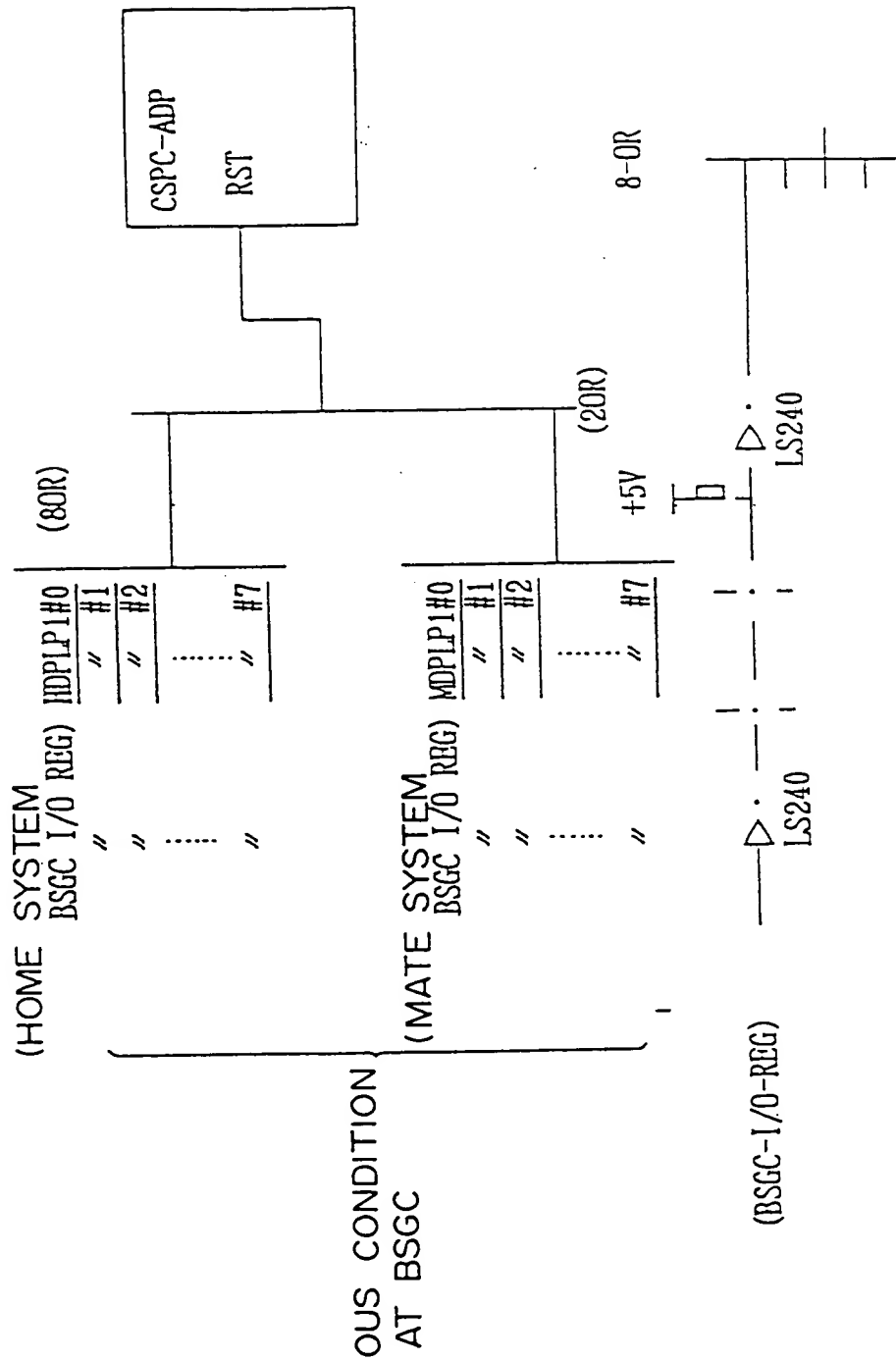


FIG. 769

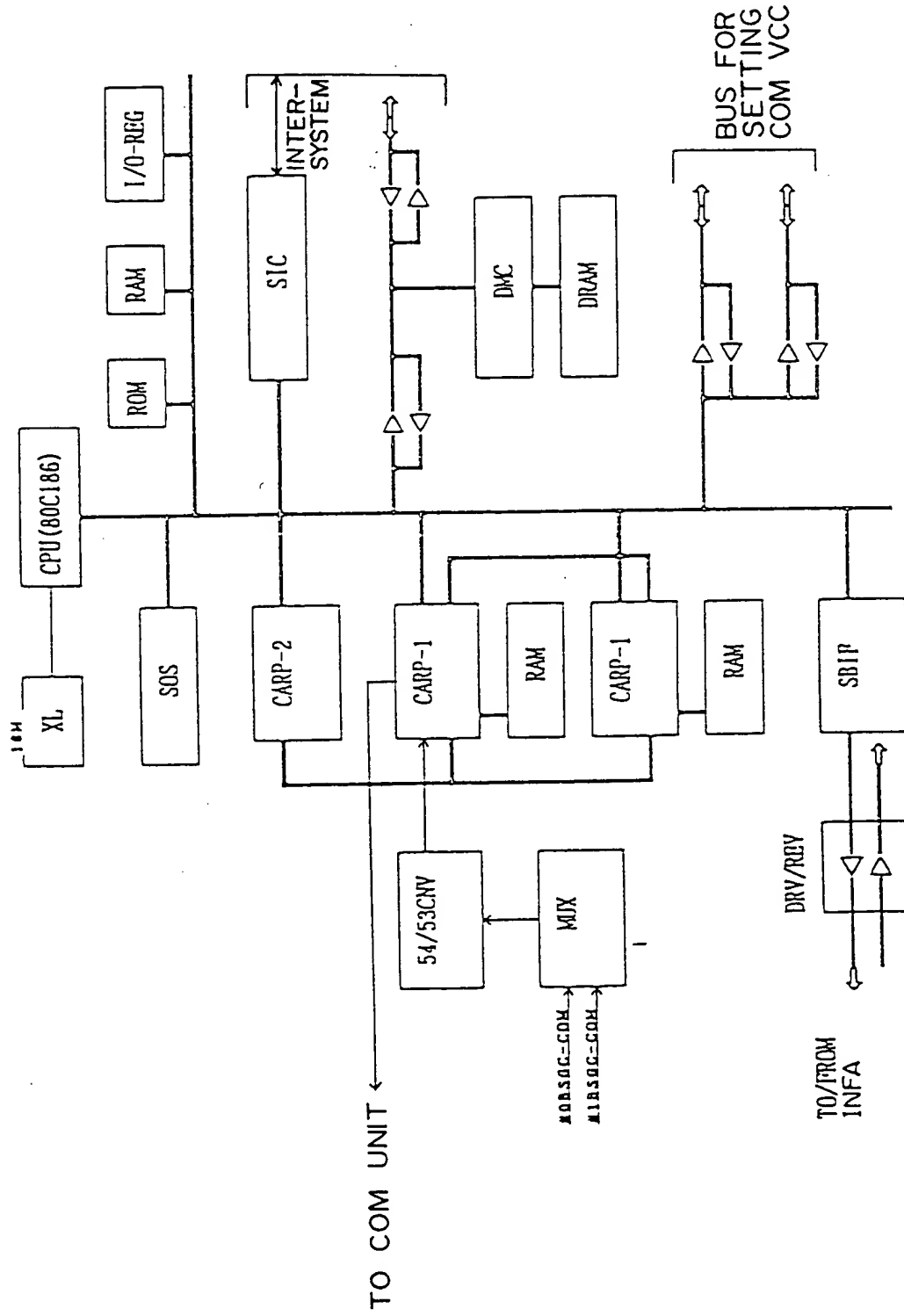


FIG. 770

FUNCTION BLOCK NAME	OUTLINE OF FUNCTION	MAIN LSI
MPU	MAIN CONTROL PROCESSOR 8MHz OPERATION. INF INTERFACE/SUBSCRIBER, INTER-DEVICE LAP CONTROL	INTEL80C186
ROM	64 KBYTE X 4 PHASE BAND CONFIGURATION	HN27C4096G-10
RAM	SRAM - 32 KBYTE	MB84256A
	DRAM - 896 KBYTE	MB81256 X 4 81C4256 X 8
DMC	DETECTING DRAM CONTROL, MEMORY WRITE PROTECT, AND MATE SYSTEM CLOCK DISCONNECTION. DETECTING MATE SYSTEM POWER SOURCE DISCONNECTION	MB670639
CARP-1	MULTIPLEXING LSI CAPABLE OF SIMULTANEOUSLY OPERATING UP TO 16 CH CELL DISASSEMBLY AND ASSEMBLY BY SUPPORTING TYPE-3 OF ATM LAYER OF B-ISDN PROTOCOL AND CELL DISASSEMBLY/ASSEMBLY SUBLAYER (SAR)	MBCG31134-602
CARP-2	CARP-2 IS CONNECTED TO CARP-1 AND TRANSFERS TRANSMISSION DATA IN MEMORY TO SW IN DMA OPERATION AS TRANSMISSION PROCESS	MB630615
SIC	FOR SYSTEM CROSS-CONNECTION, PARALLEL DATA FROM CPU IS CONVERTED INTO SERIAL DATA FOR COMMUNICATIONS	MB674602
SOS	LSI FOR PERFORMING 80186 CPU REALTIME COMPASS III PROCESS AT HIGH SPEED	MB602773
SBIF	DATA TRANSFER PROCESS BETWEEN INF INTERFACE AND CPU BUS. COMMAND ACTIVATION IS REALIZED AND REPORTED THROUGH INTERRUPTION TO CPU. DATA TRANSMISSION DMA IS SPECIFIED FOR REG IN SBIF	MB651623
DRV/REV	ELECTRICAL CHANGE IS MADE IN INF INTERFACE (V.11)	MB412/MB413

FIG. 771

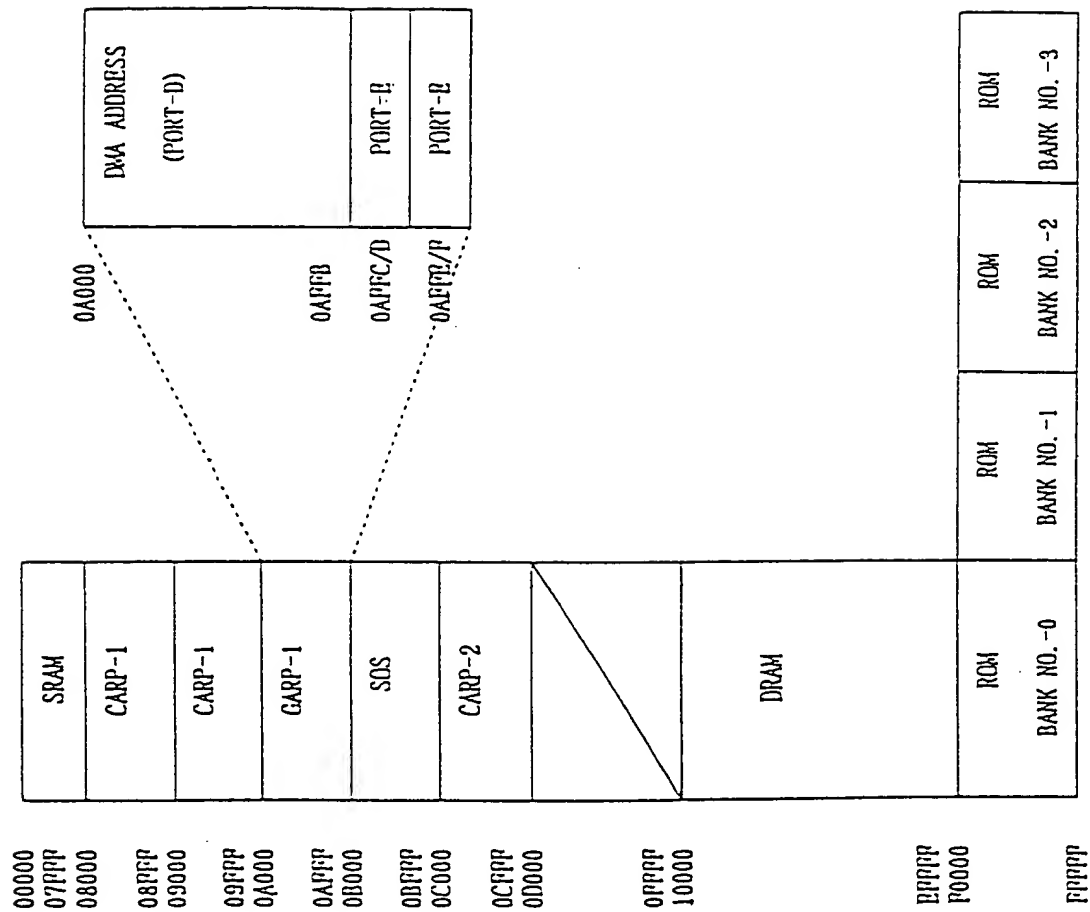


FIG. 772

0000000000000000

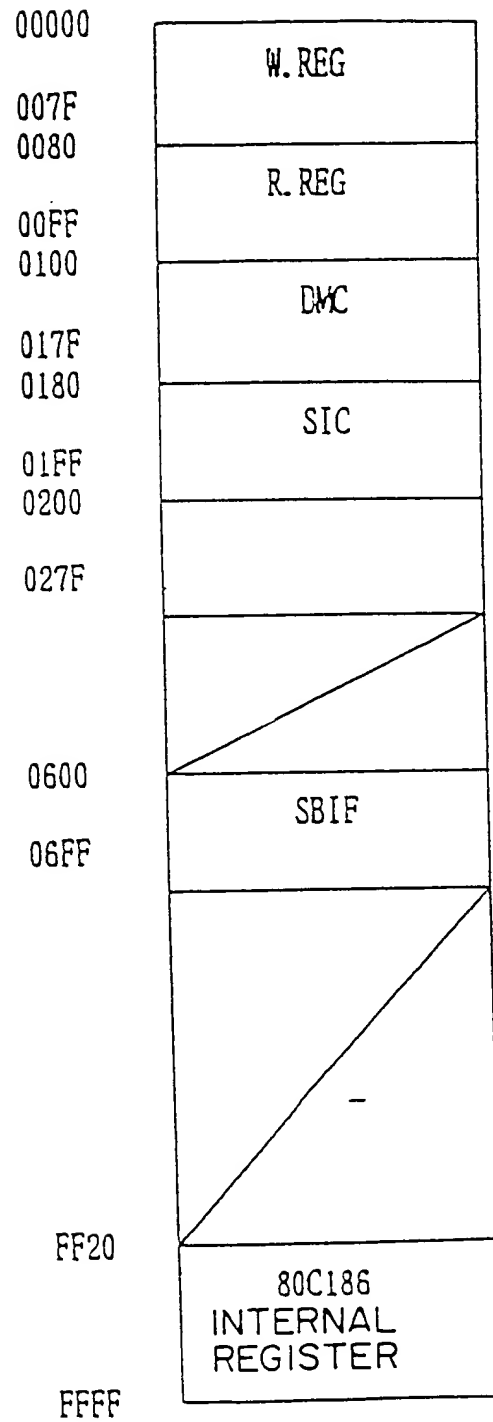


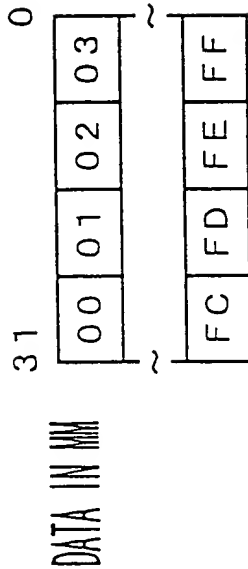
FIG. 773

No.	INSTRUCTION TYPE	IN/OUT	READ/WRITE	REMARKS
1	COMMAND ACTIVATION	OUT	WRITE	
2	RETRY INSTRUCTION	OUT	WRITE	
3	MSCN READ	IN	READ	
4	TEST LOOPBACK DATA WRITE	OUT	WRITE	
5	TEST LOOPBACK DATA READ	IN	READ	

FIG. 774

PATTERN1

CONSECUTIVE DATA PATTERN WITHOUT USING CD



PATTERN2

CONSECUTIVE DATA PATTERN USING CD

FIG. 775

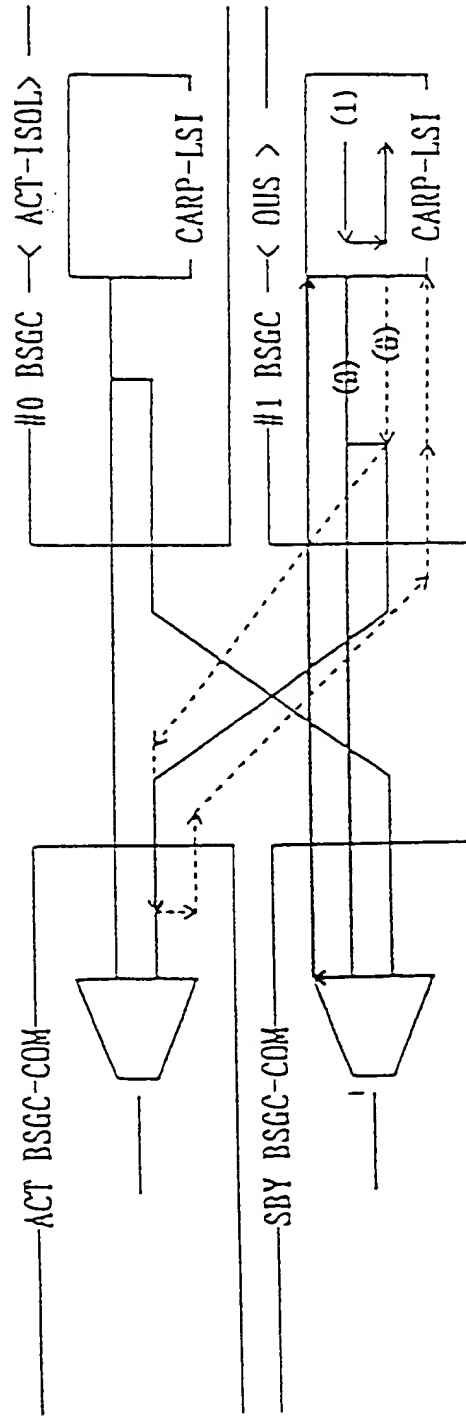
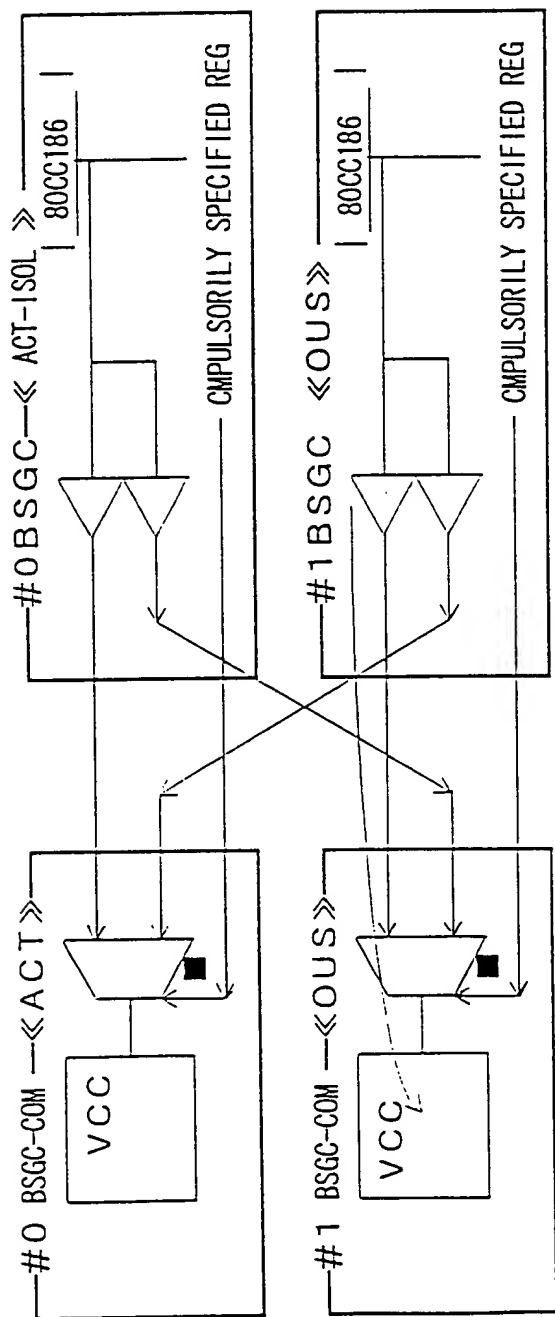


FIG. 776



■ INDICATES 2-1 SEL SELECT LOGIC CIRCUIT. NORMALLY ACT-BSGE IS SELECTED.

FIG. 777

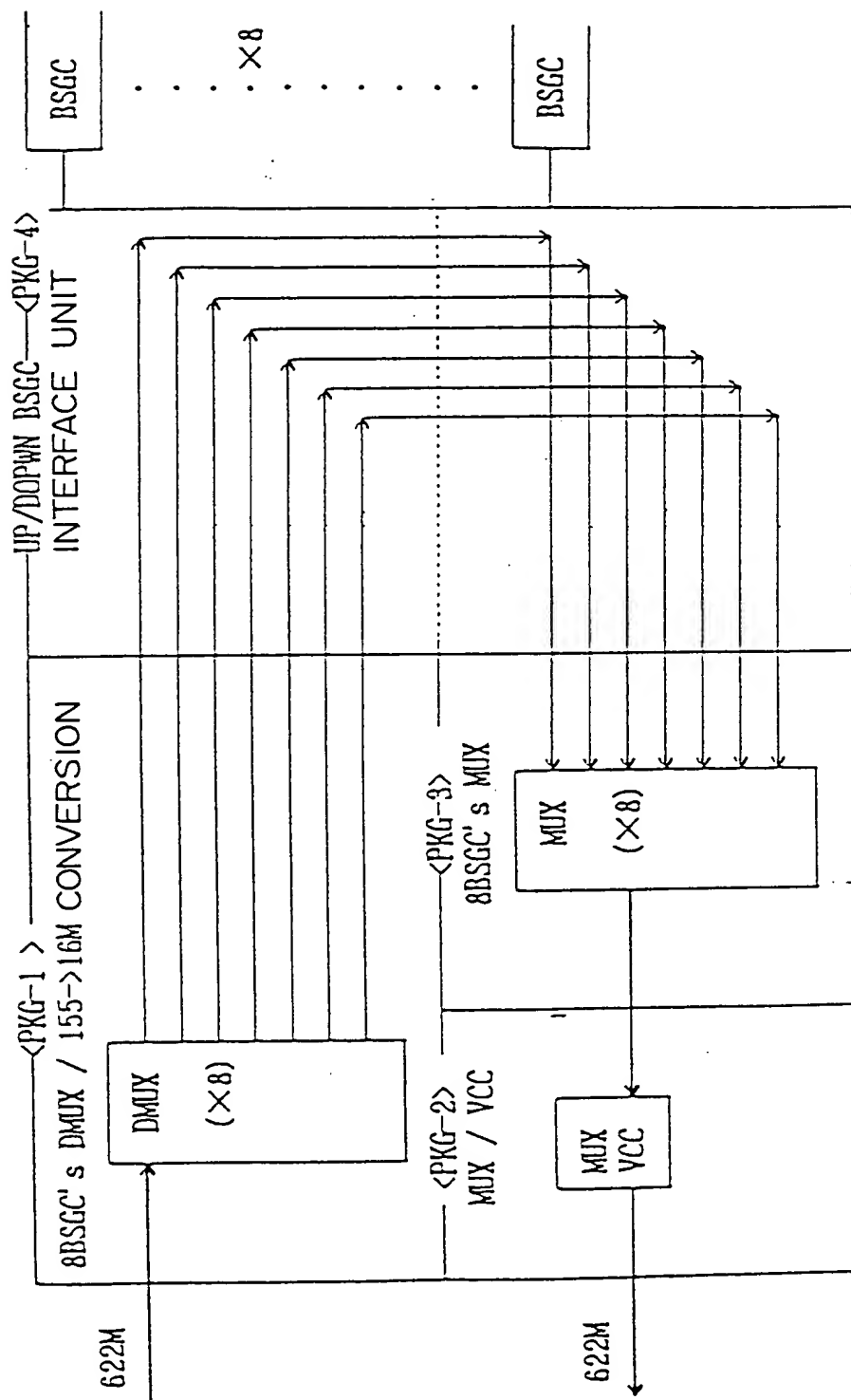


FIG. 779

6656260 672260

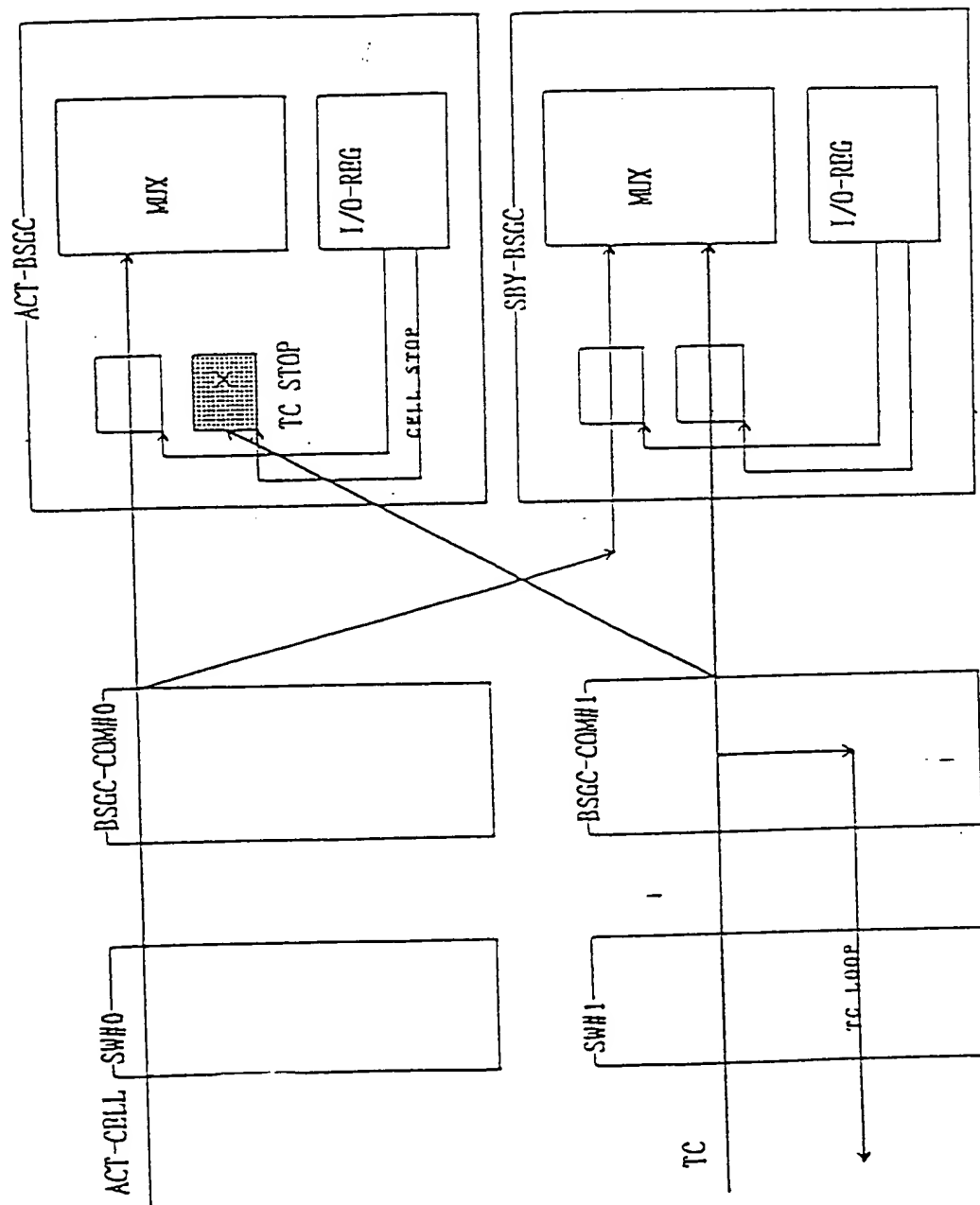


FIG. 780

66360 612260

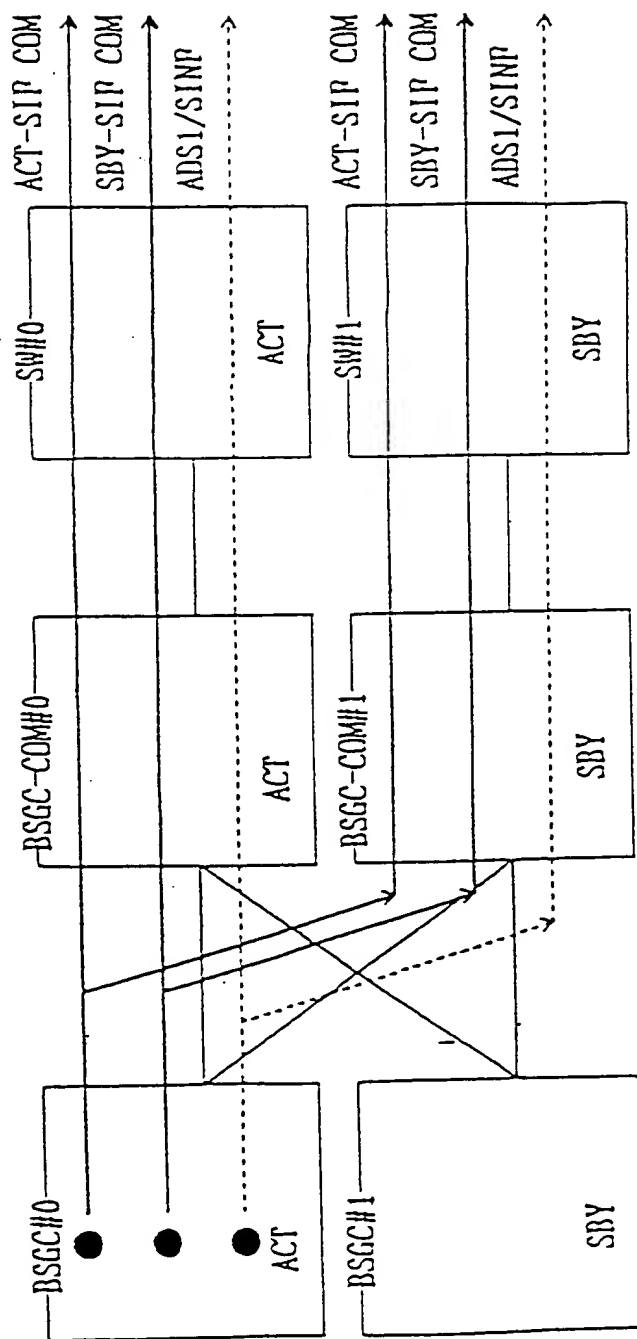


FIG. 781

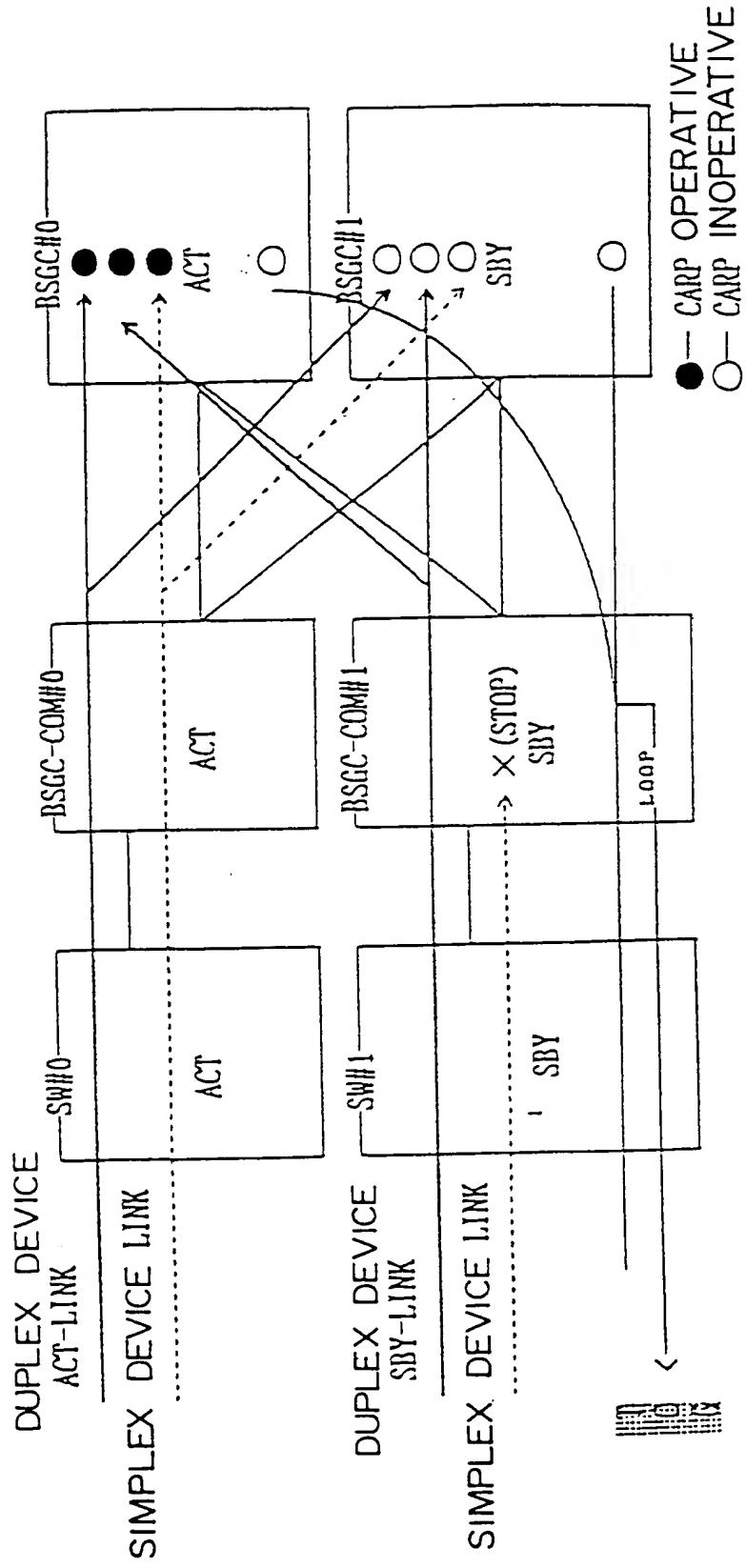


FIG. 782

66360762600

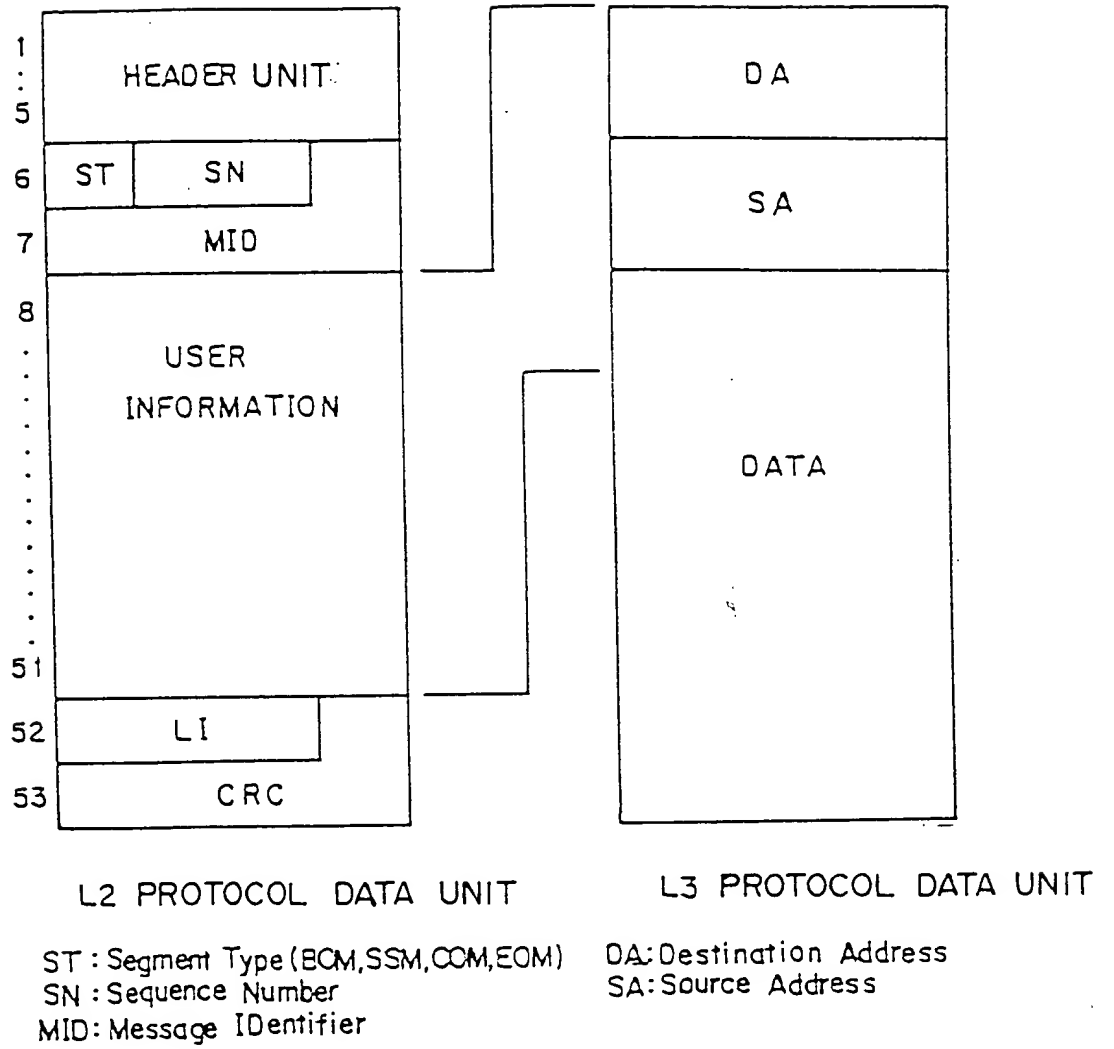


FIG. 783

669660 672260

INPUT MID

TAG	OUTPUT MID
⋮	⋮

FIG. 784

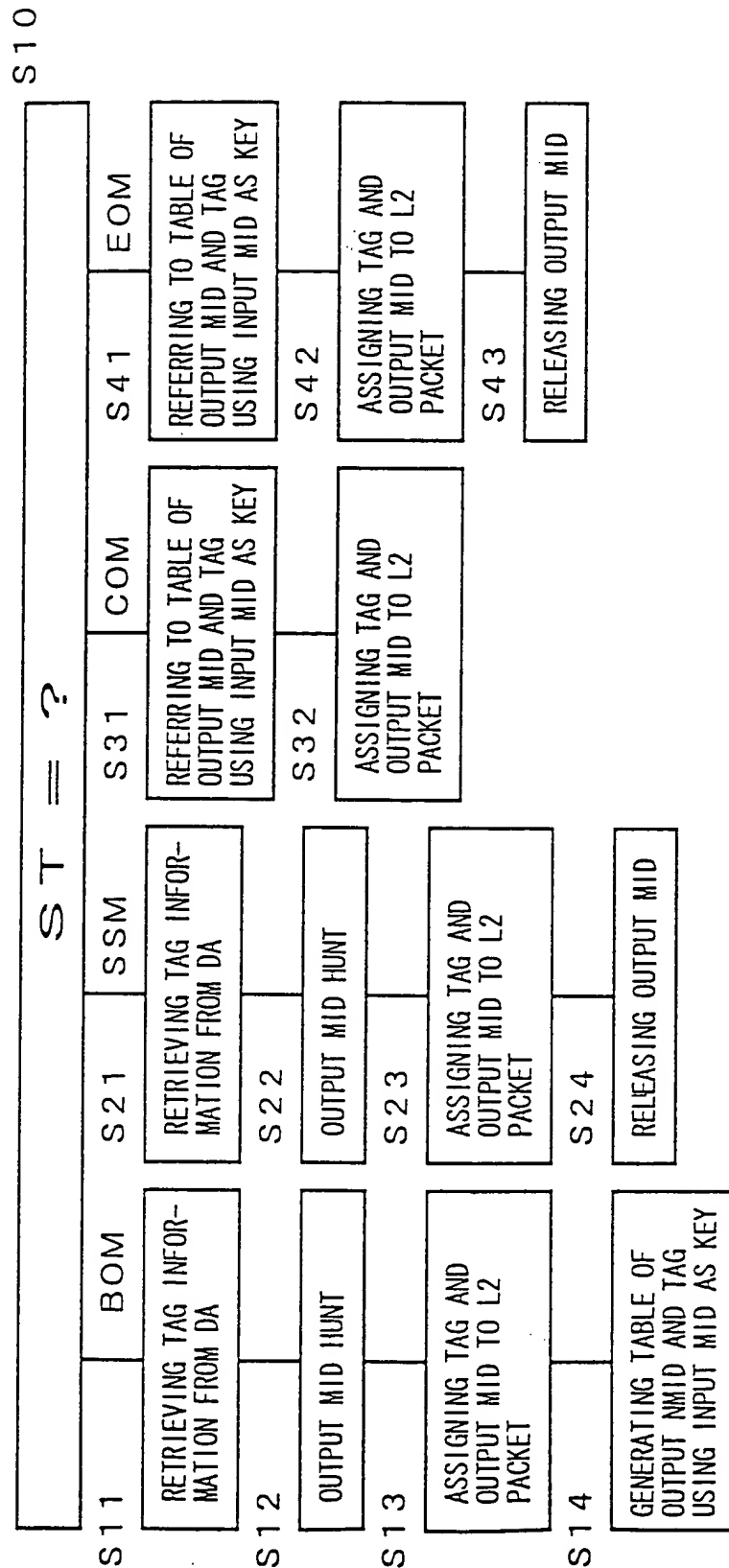


FIG. 785

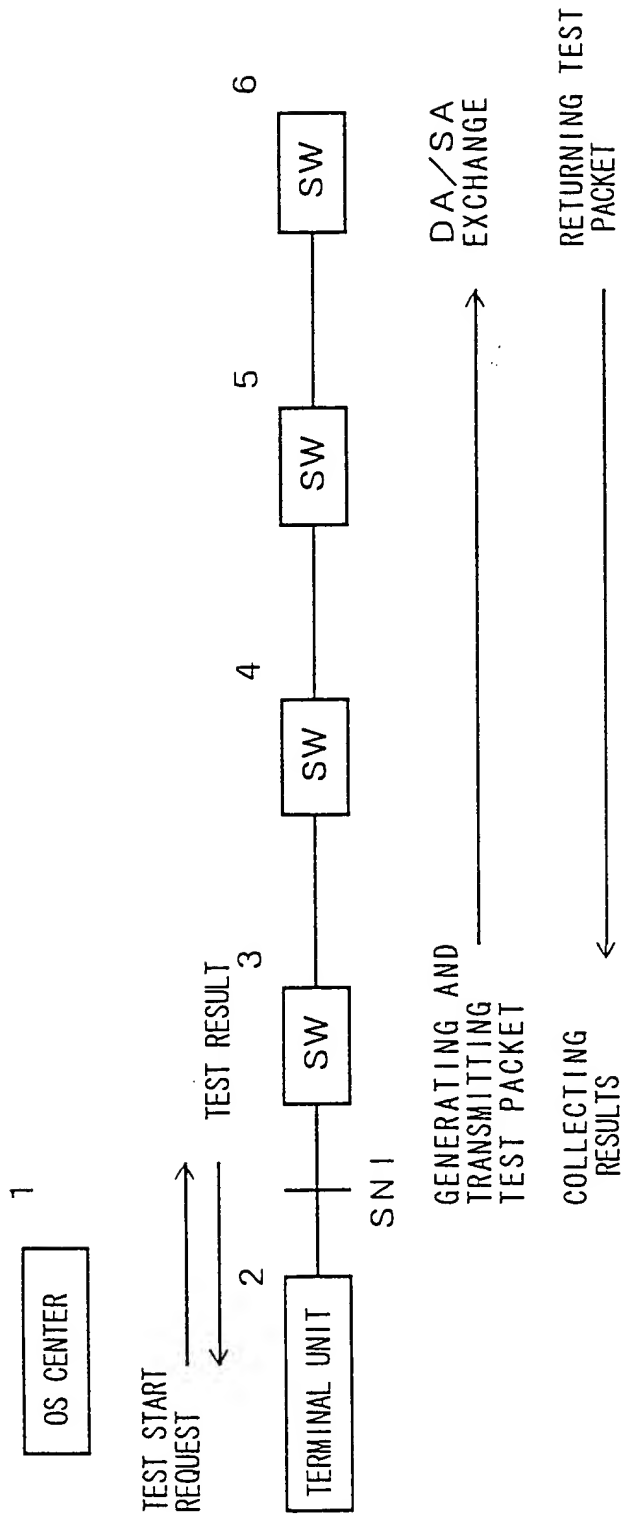


FIG. 786

669660 6122260

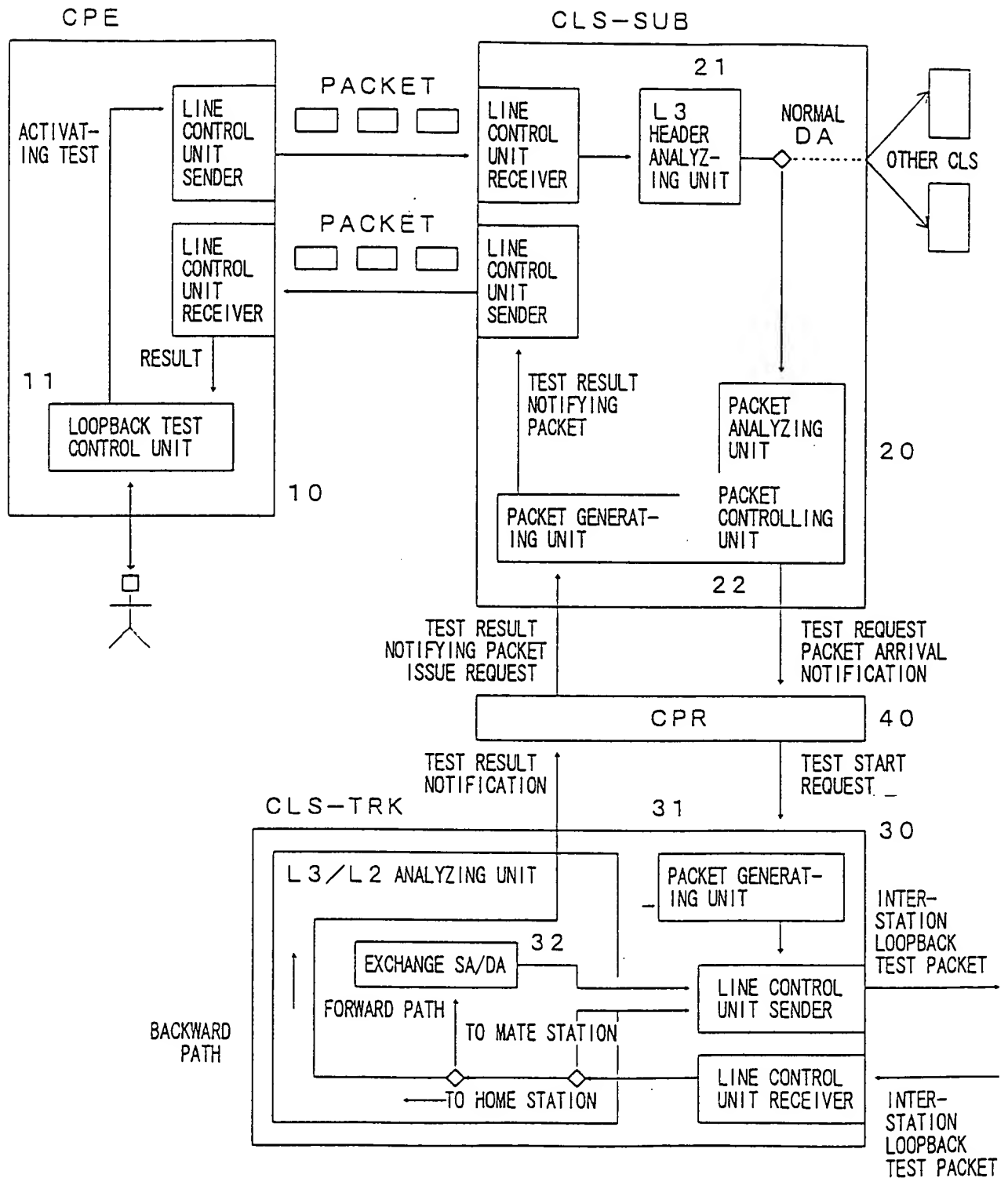


FIG. 787

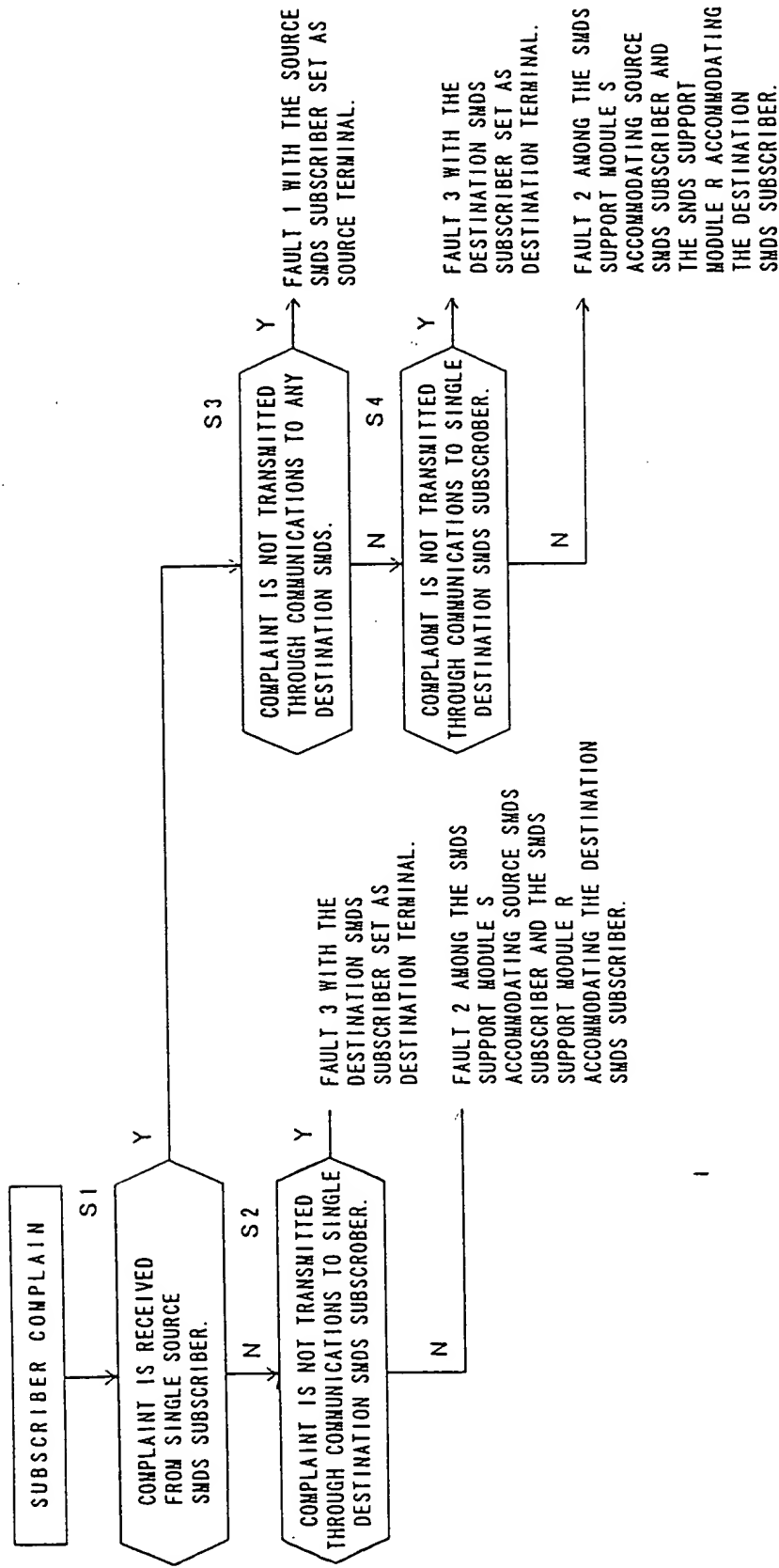


FIG. 788

SMDS SUBSCRIBER

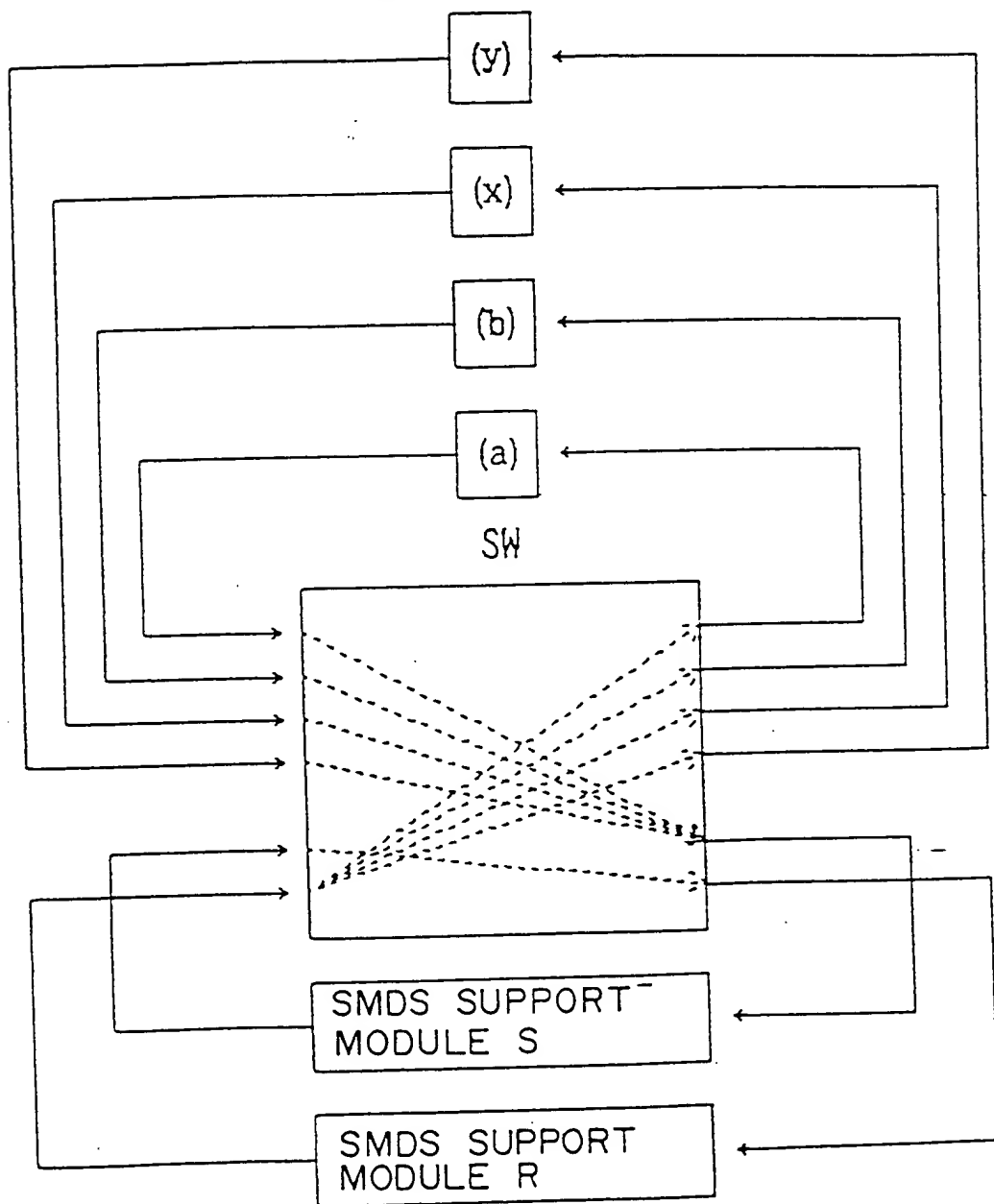


FIG. 789

SMDS SUBSCRIBER

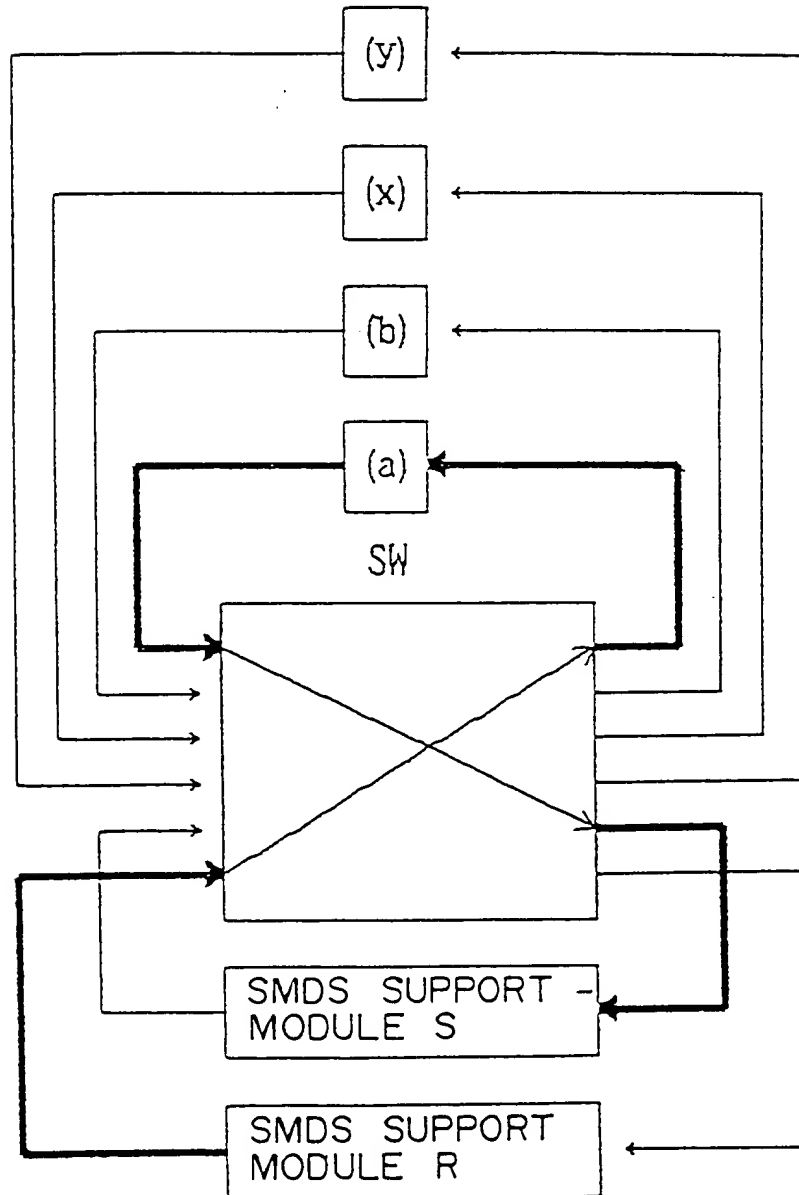


FIG. 790

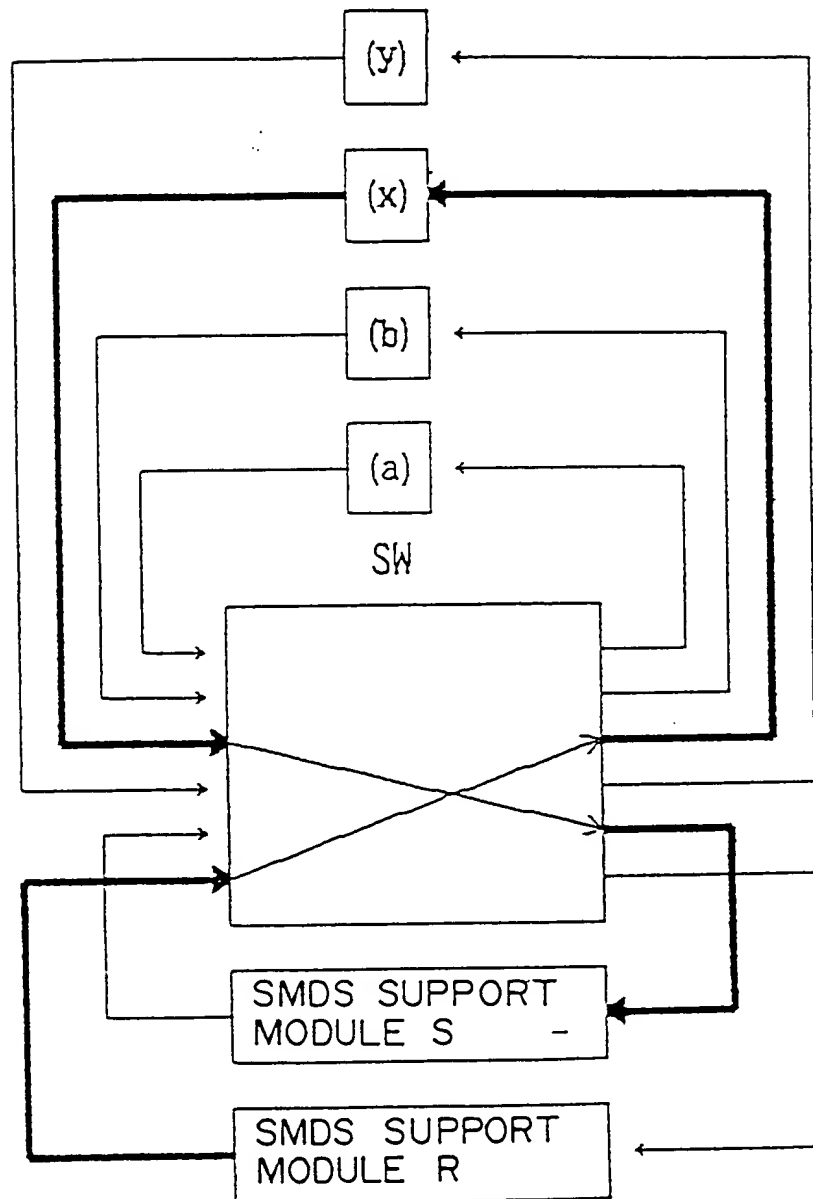
[illegible]

FIG. 791

SECRET

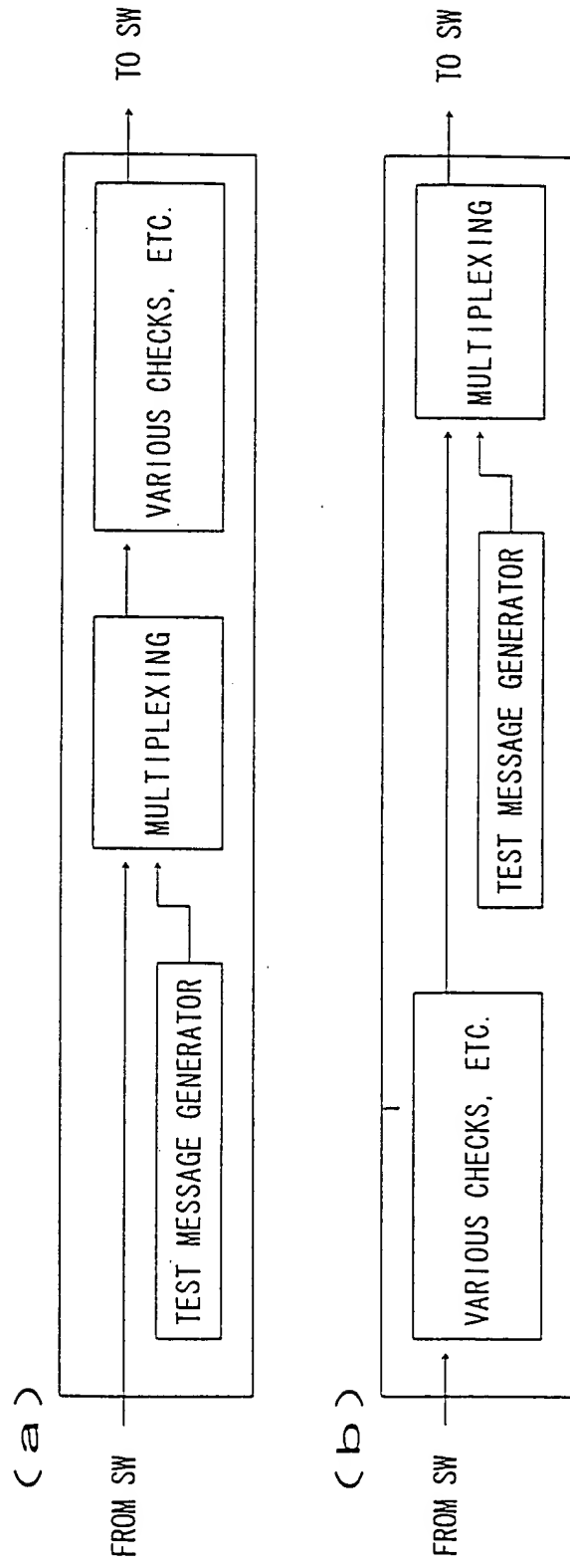


FIG. 792

SECRET

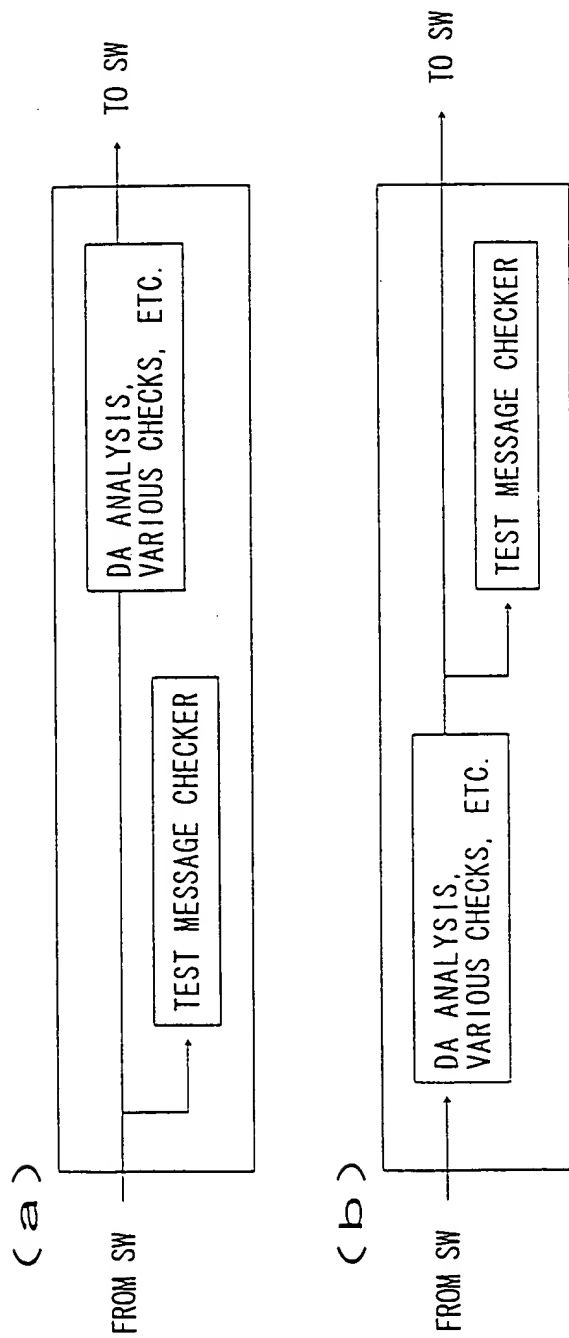


FIG. 793

66920-162260

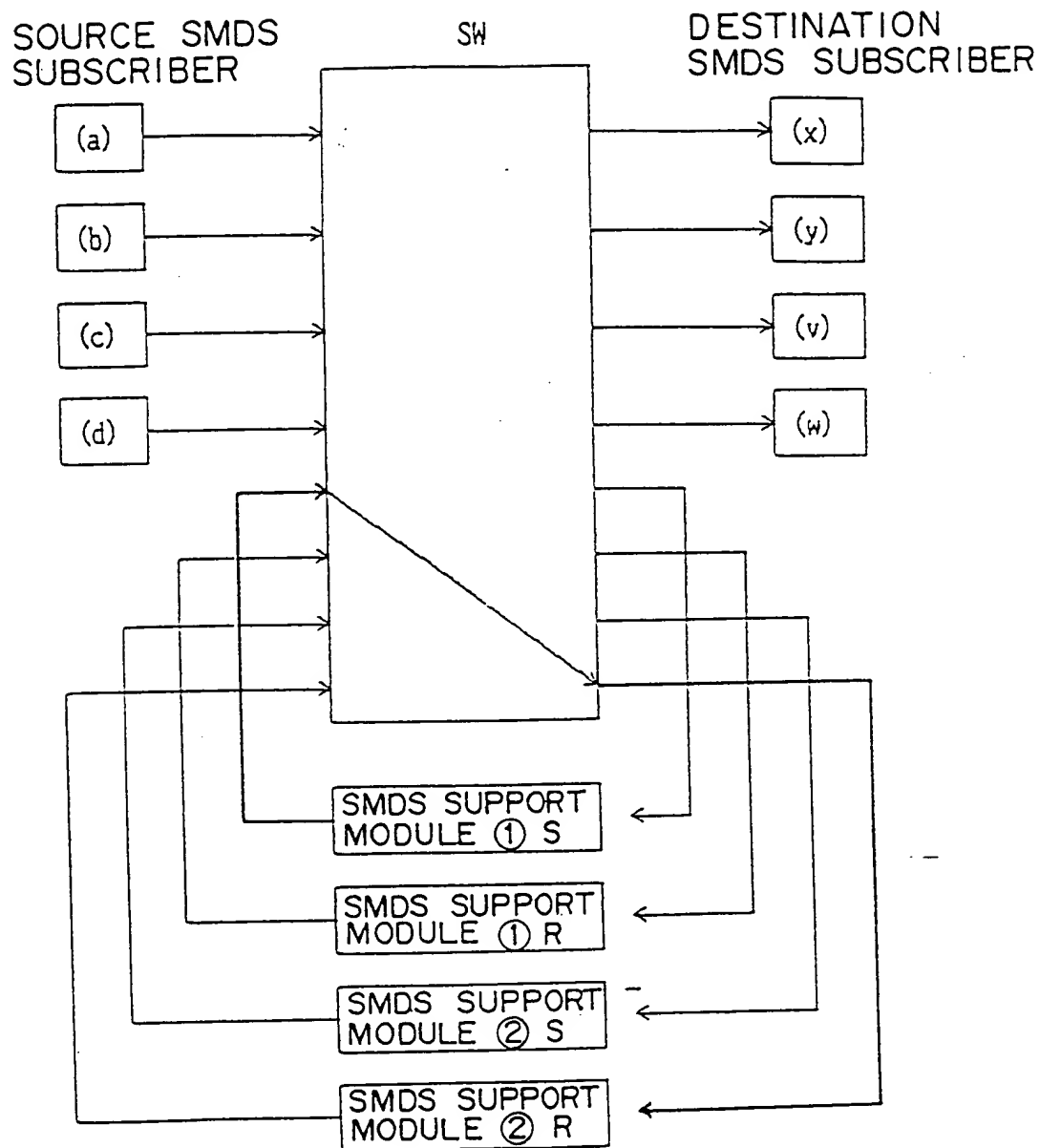


FIG. 794

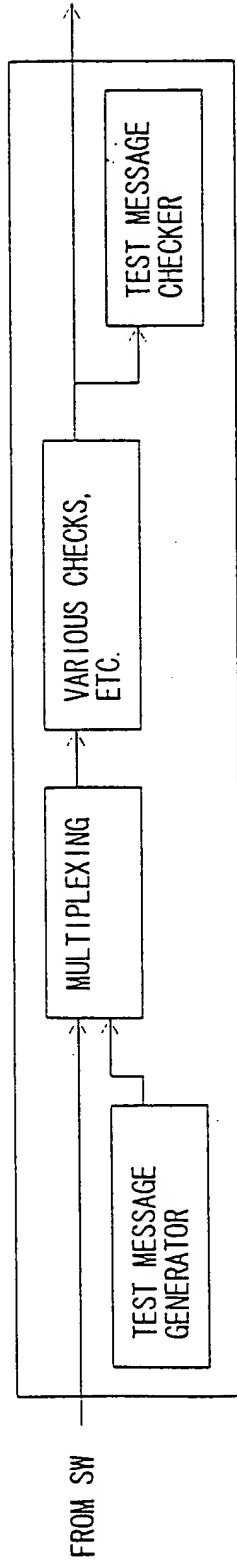
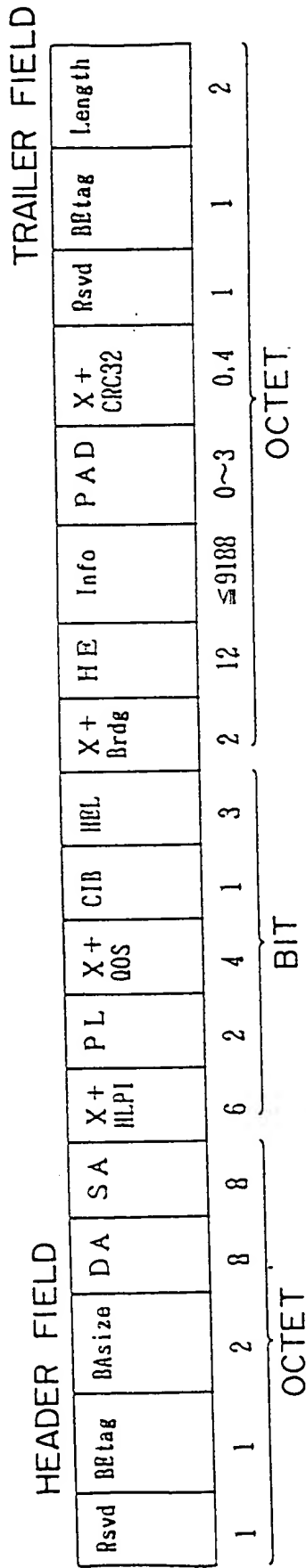


FIG. 795



Rsvd = Reserved
BEtag = Beginning-End Tag
BAsize = Buffer Allocation Size = Length
DA = Destination Address
SA = Source Address
X+ = Not processed by the network
HLPI = Higher Layer Protocol Identifier
PL = PAD Length

QOS = Quality of Service
CIB = CRC32 Indication Bit
HEL = Header Extension Length
Brdg = Bridging
HE = Header Extension
Info = Information
CRC32 = 32-bit Cyclic Redundancy Check

FIG. 796

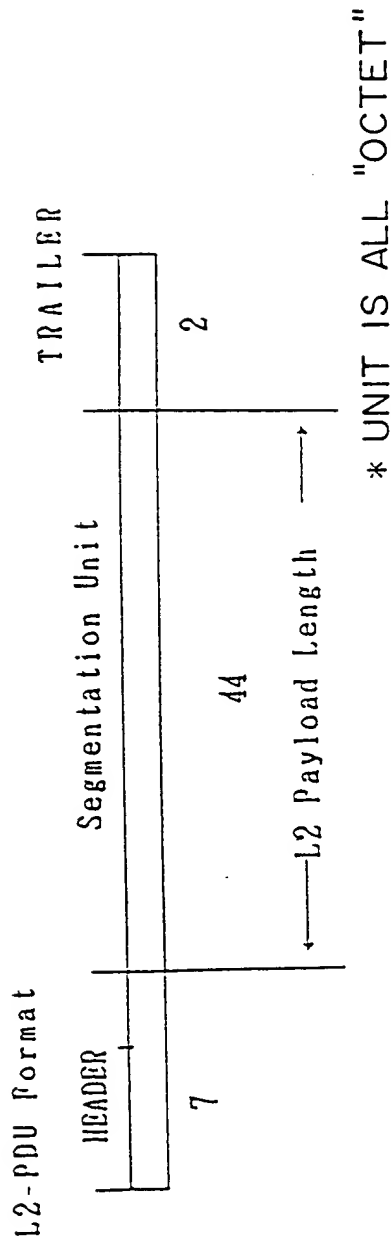
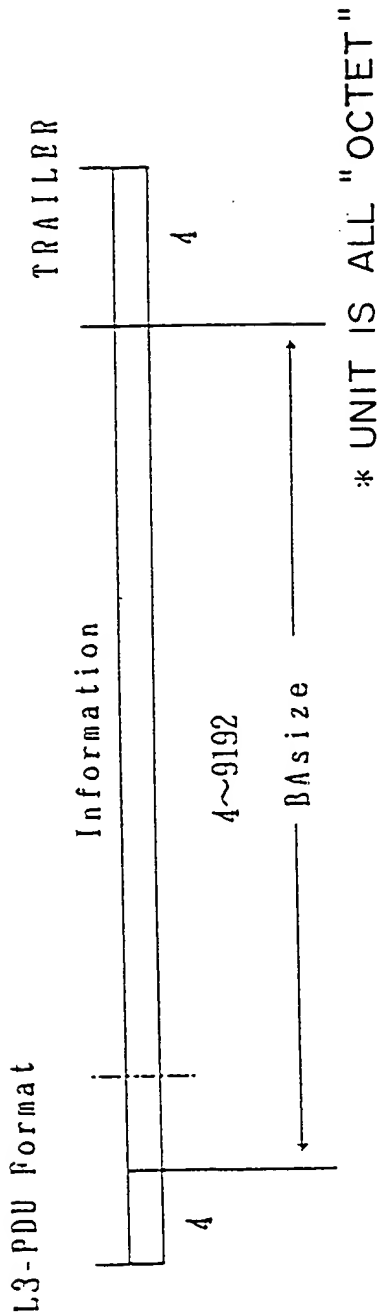


FIG. 797

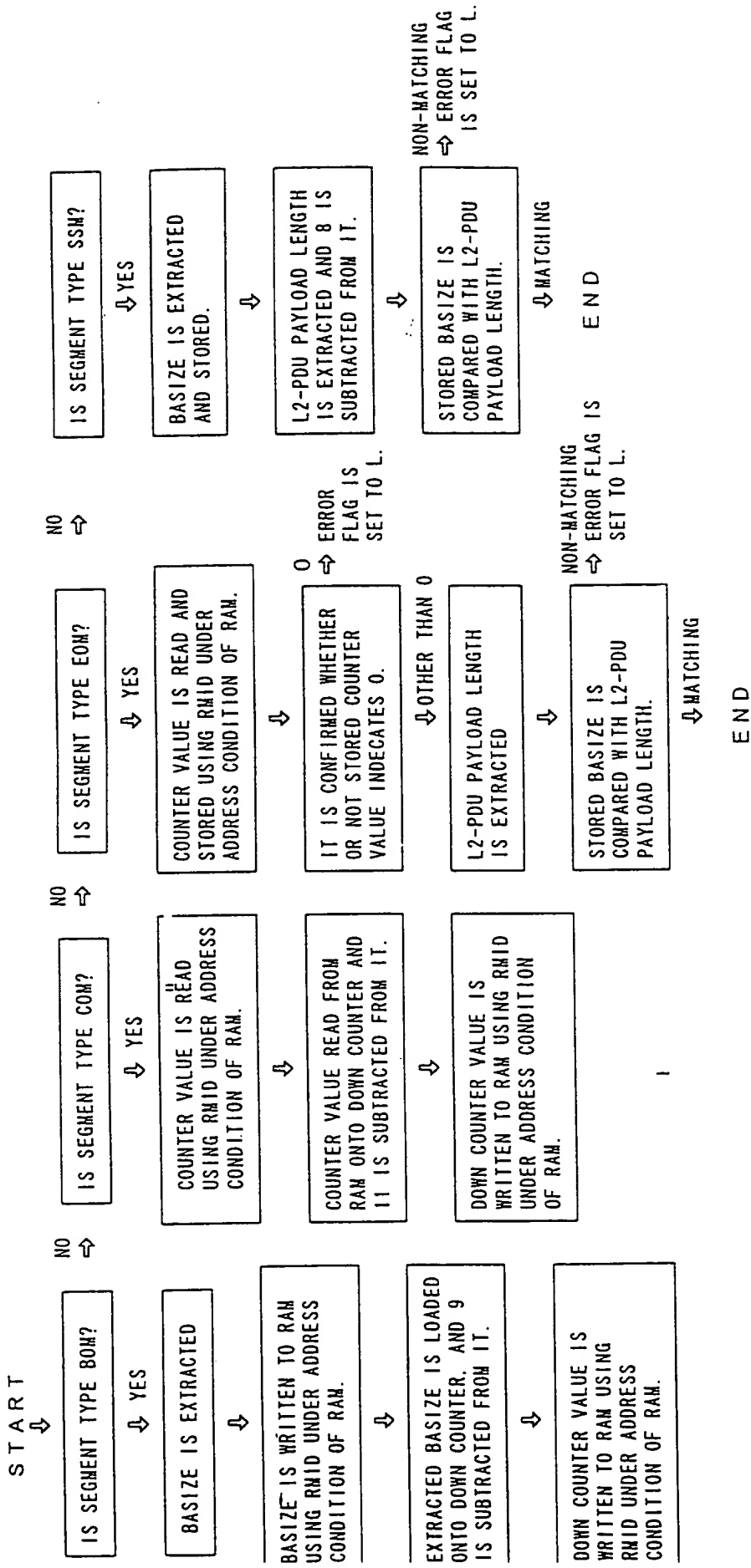


FIG. 798

669207E122200

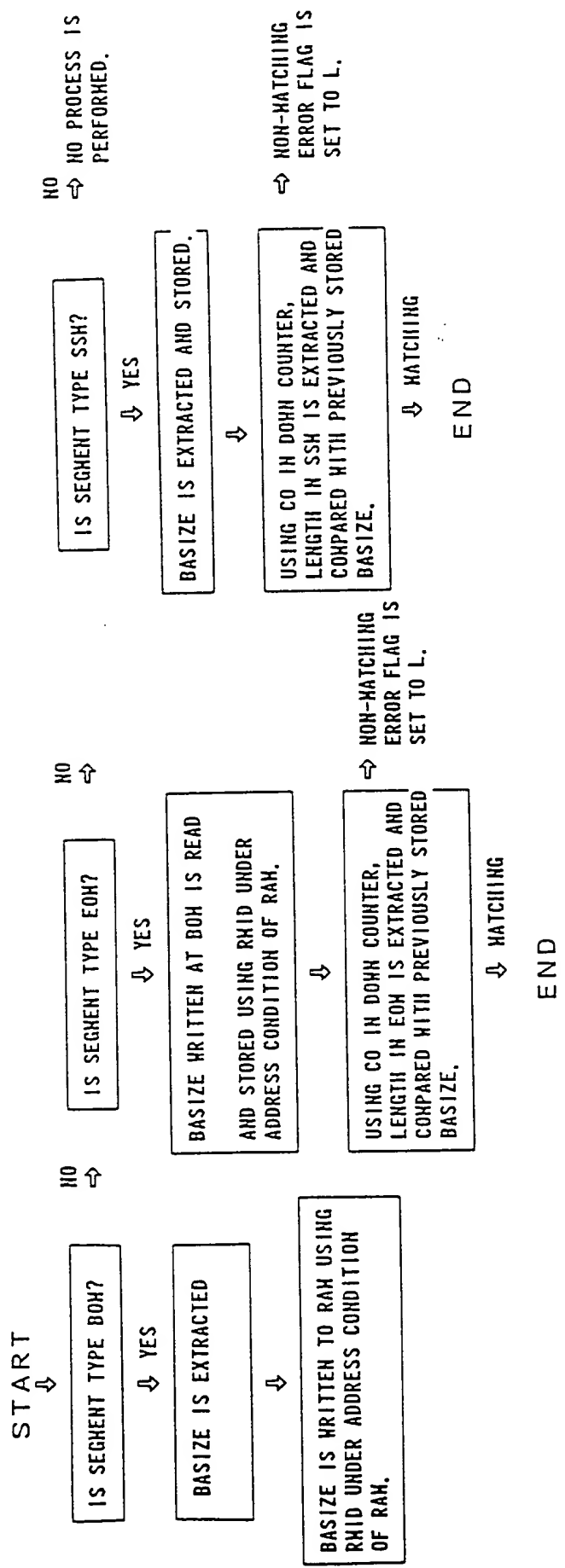


FIG. 800

00000000000000000000

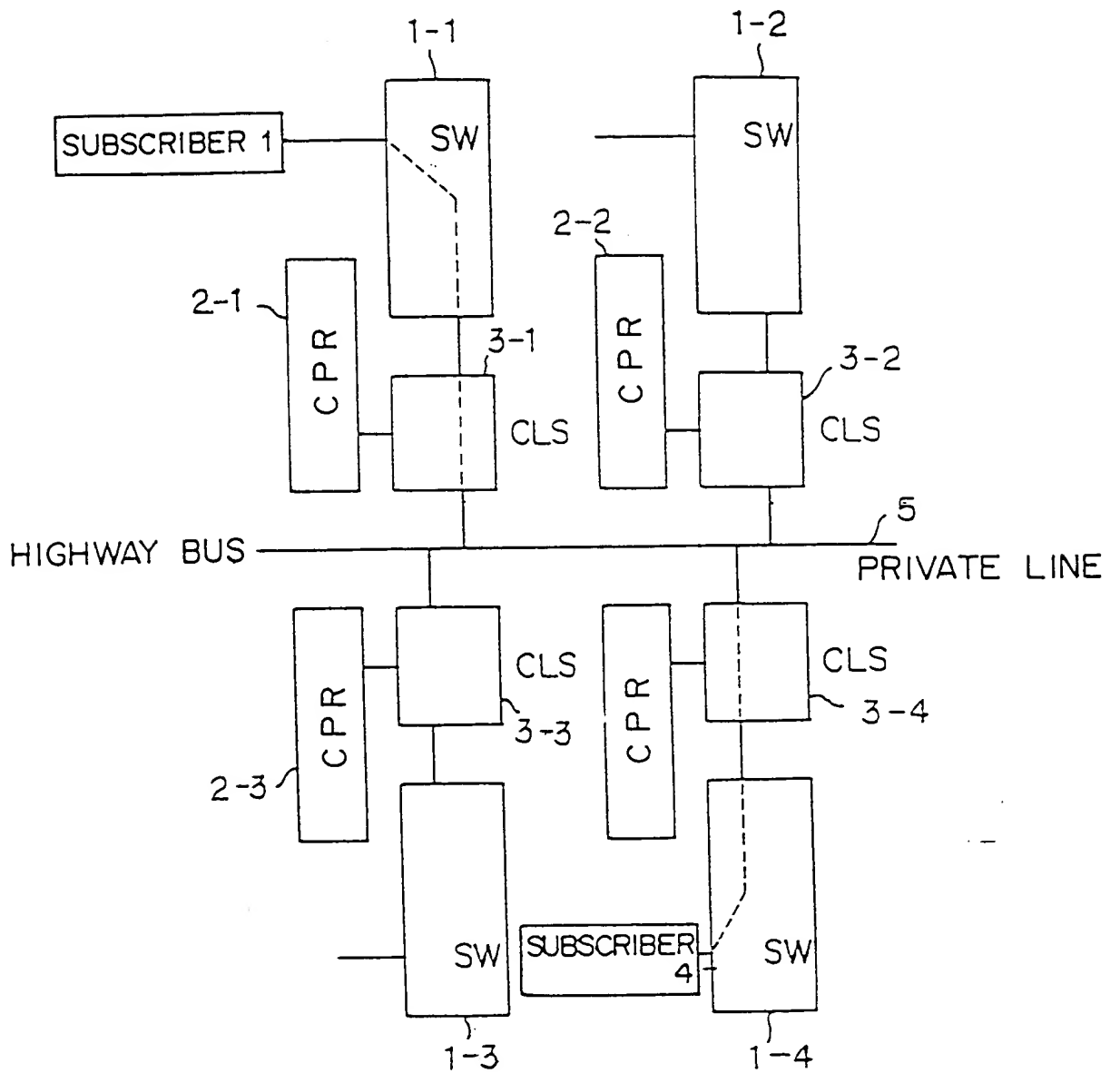


FIG. 802

(a) MANAGEMENT DATA ADDRESSED TO HOME CLS

TELEPHONE NUMBER	CONNECTION ID.
0 0 0 1	V C I = 112, V P I = 100
0 0 0 2	V C I = 113, V P I = 100
0 0 0 3	V C I = 114, V P I = 100
0 0 0 4	V C I = 115, V P I = 100
.	.
.	.
.	.
.	.

(b) MANAGEMENT DATA ADDRESSED TO MATE CLS

TELEPHONE NUMBER	CLS IDENTIFICATION NUMBER
1 0 0 1	0 0 0 2
1 0 0 2	0 0 0 2
1 0 0 3	0 0 0 3
1 0 0 4	0 0 0 3
.	.
.	.
.	.
.	.

F I G. 8 0 4

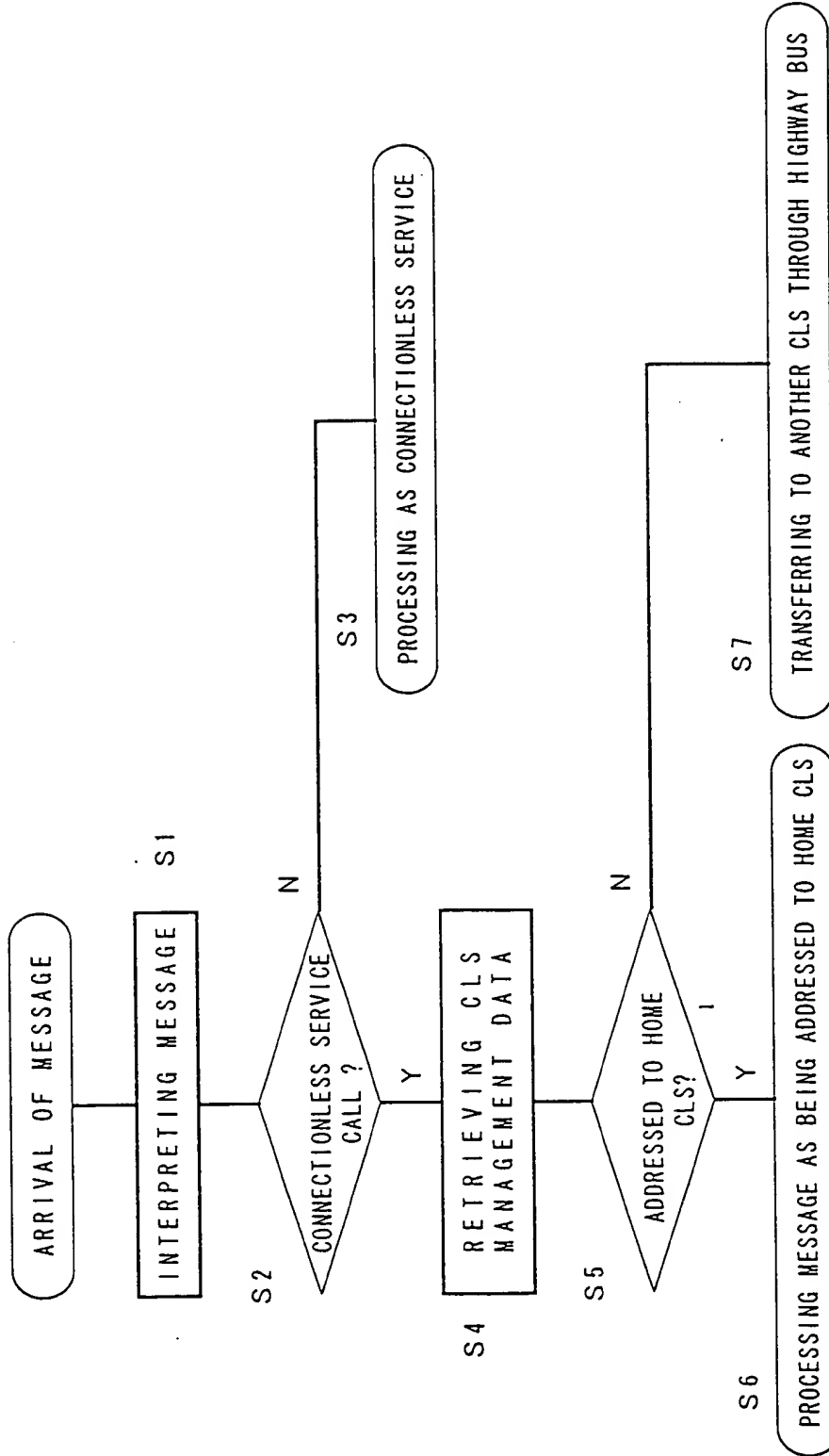


FIG. 805

669660 6122260

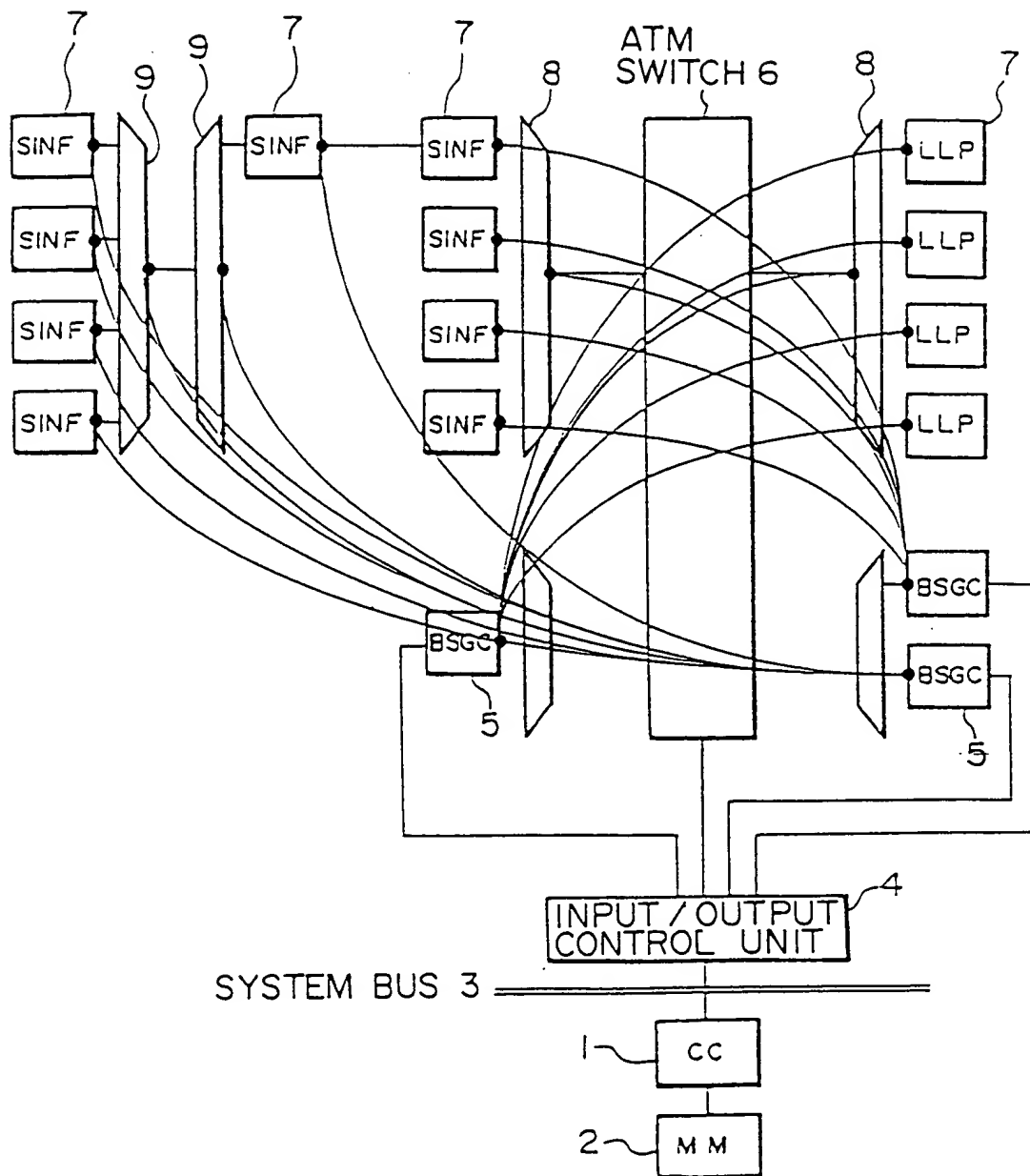


FIG. 806

669220-122200

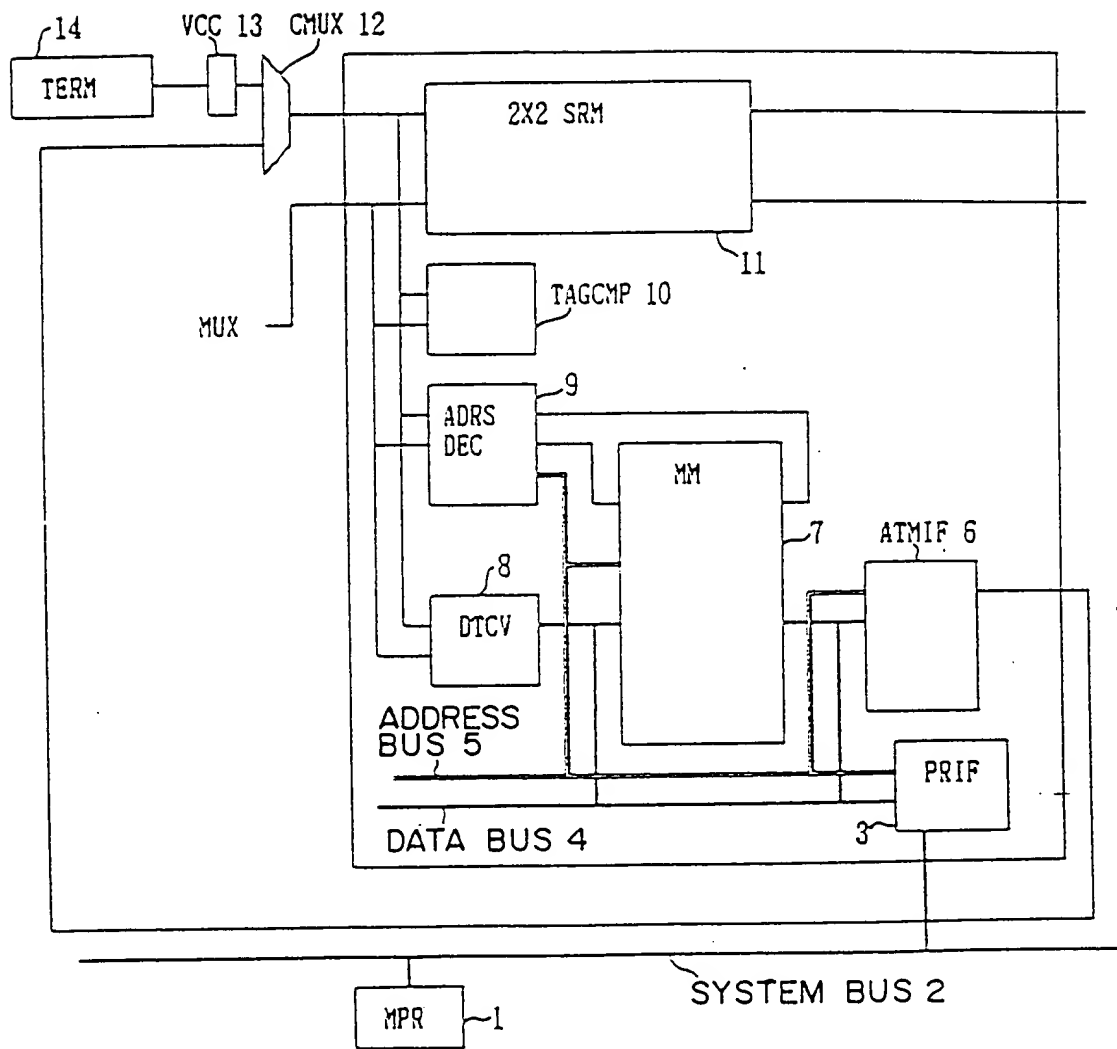


FIG. 807

00920-ET2200

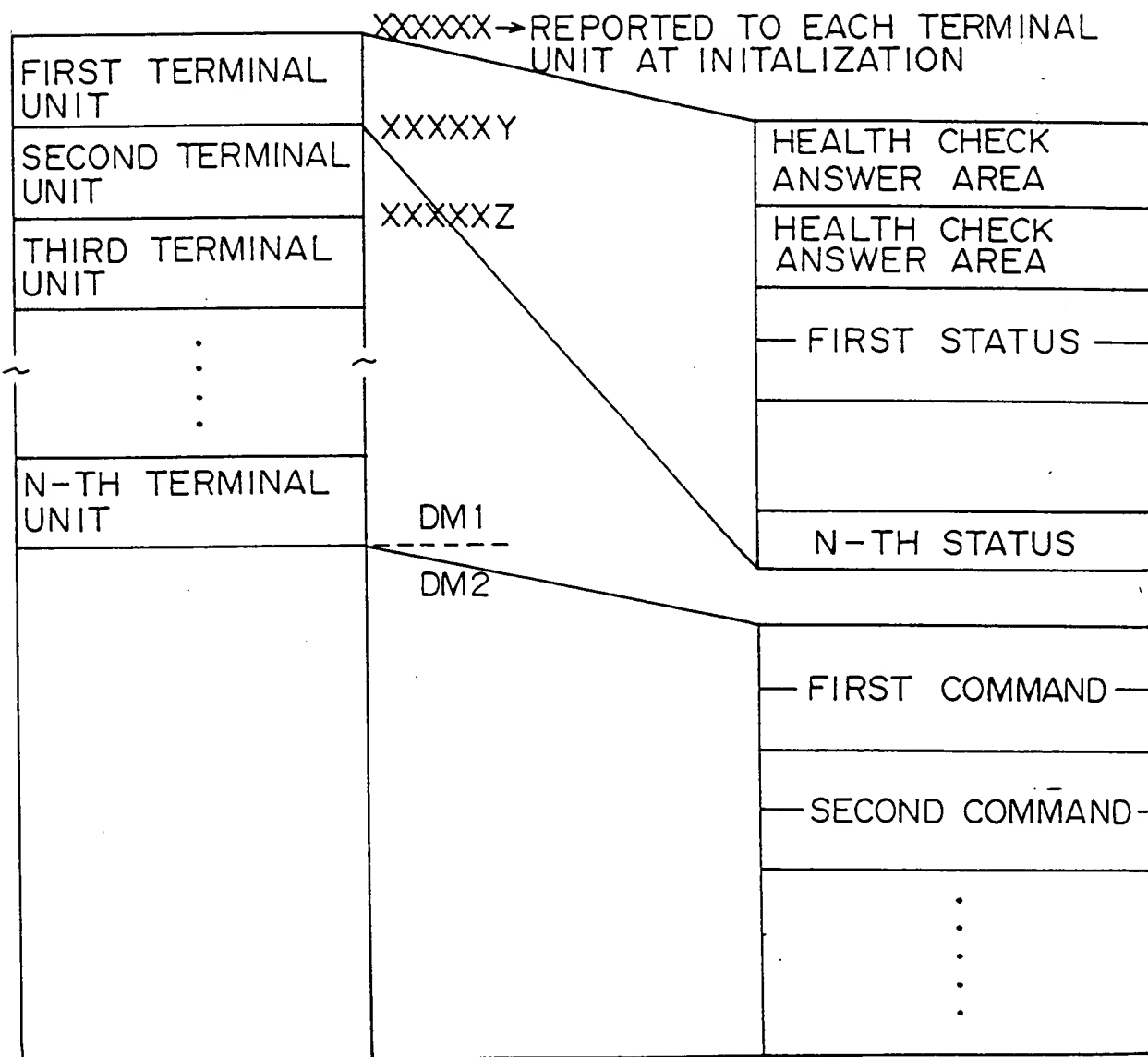
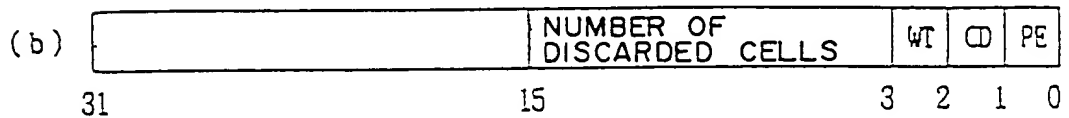
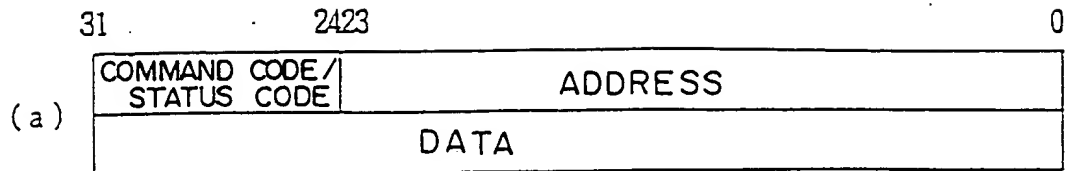


FIG. 808

00000000000000000000000000000000



PE: PARITY ERROR
CD: CLOCK DISCONNECTION
WT: PROCESSOR FAULT

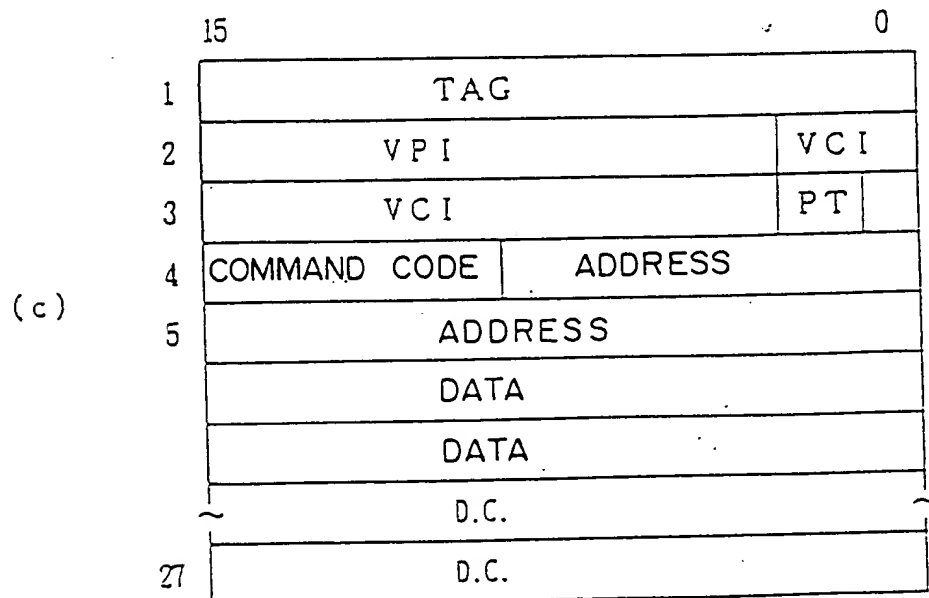


FIG. 809

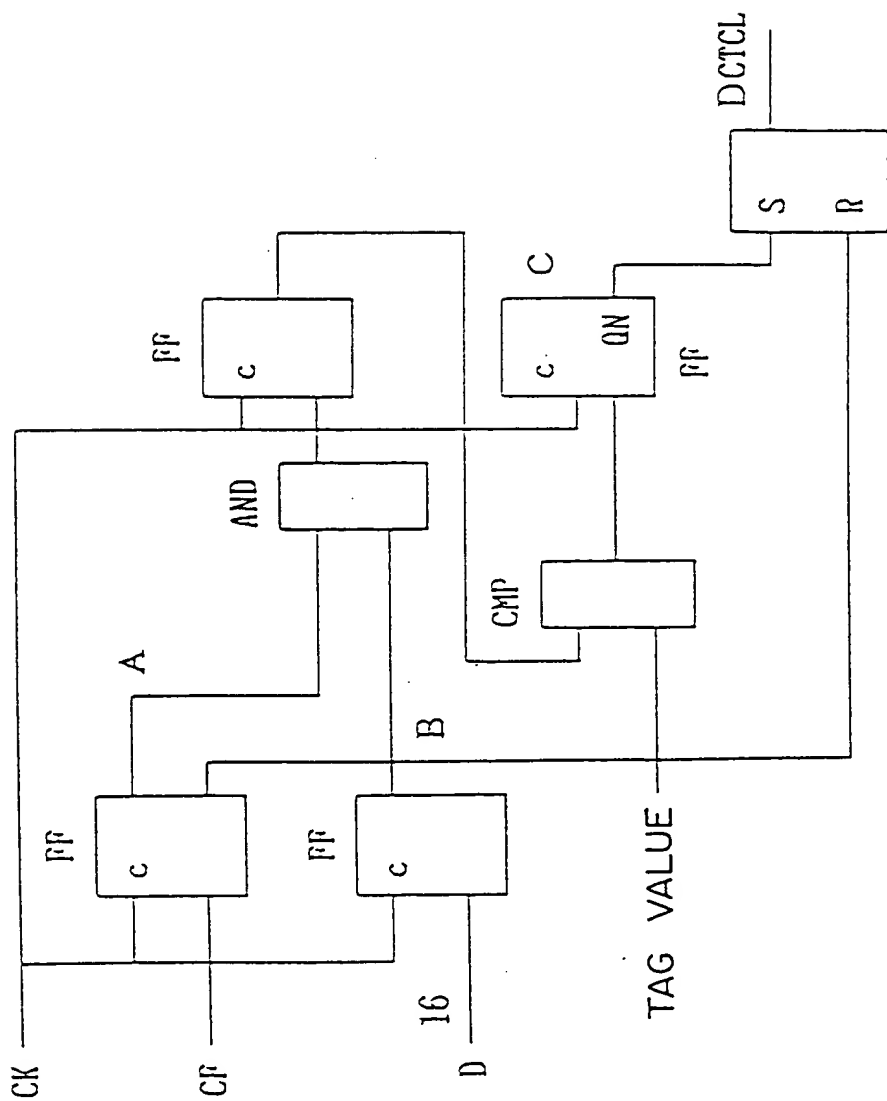


FIG. 810

669260-ET2260

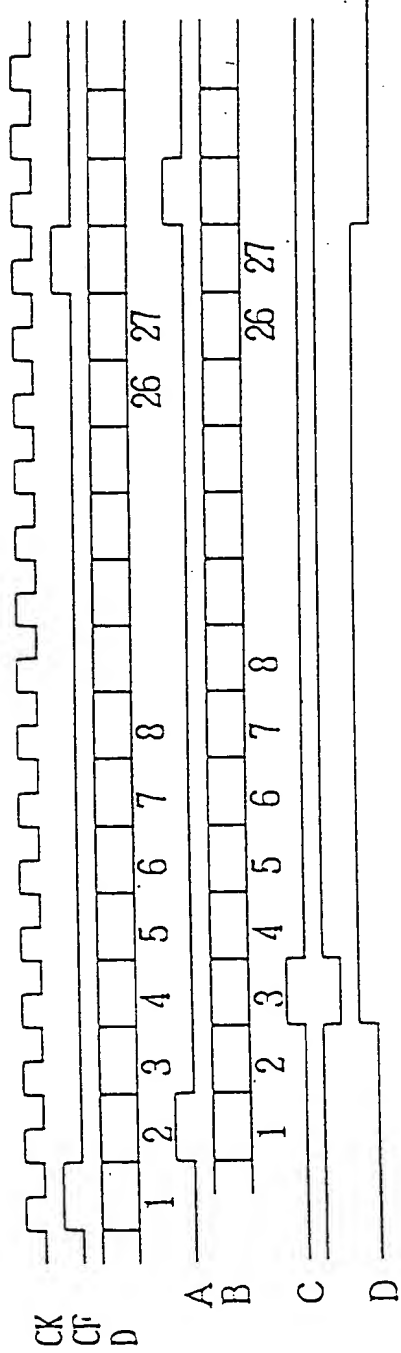


FIG. 811

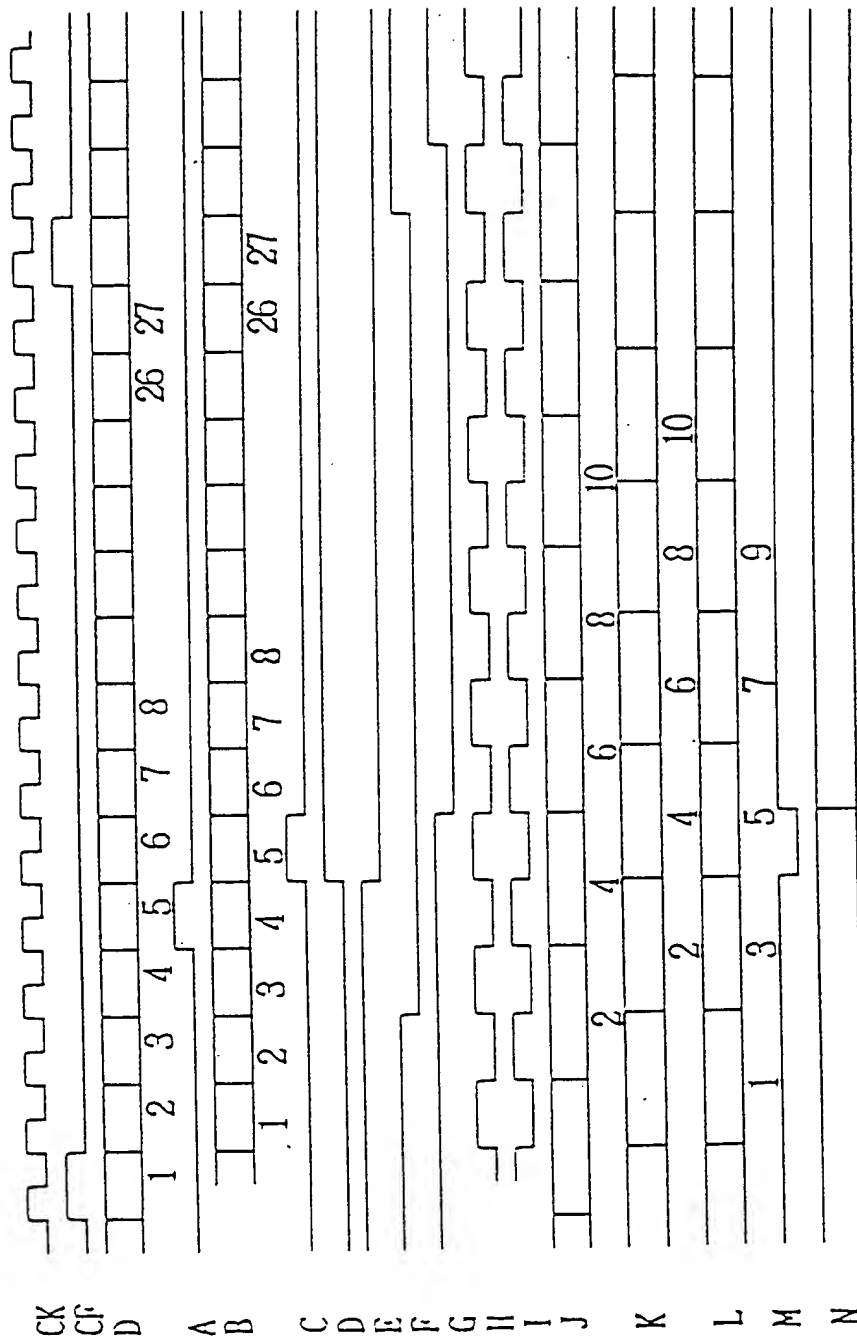


FIG. 813

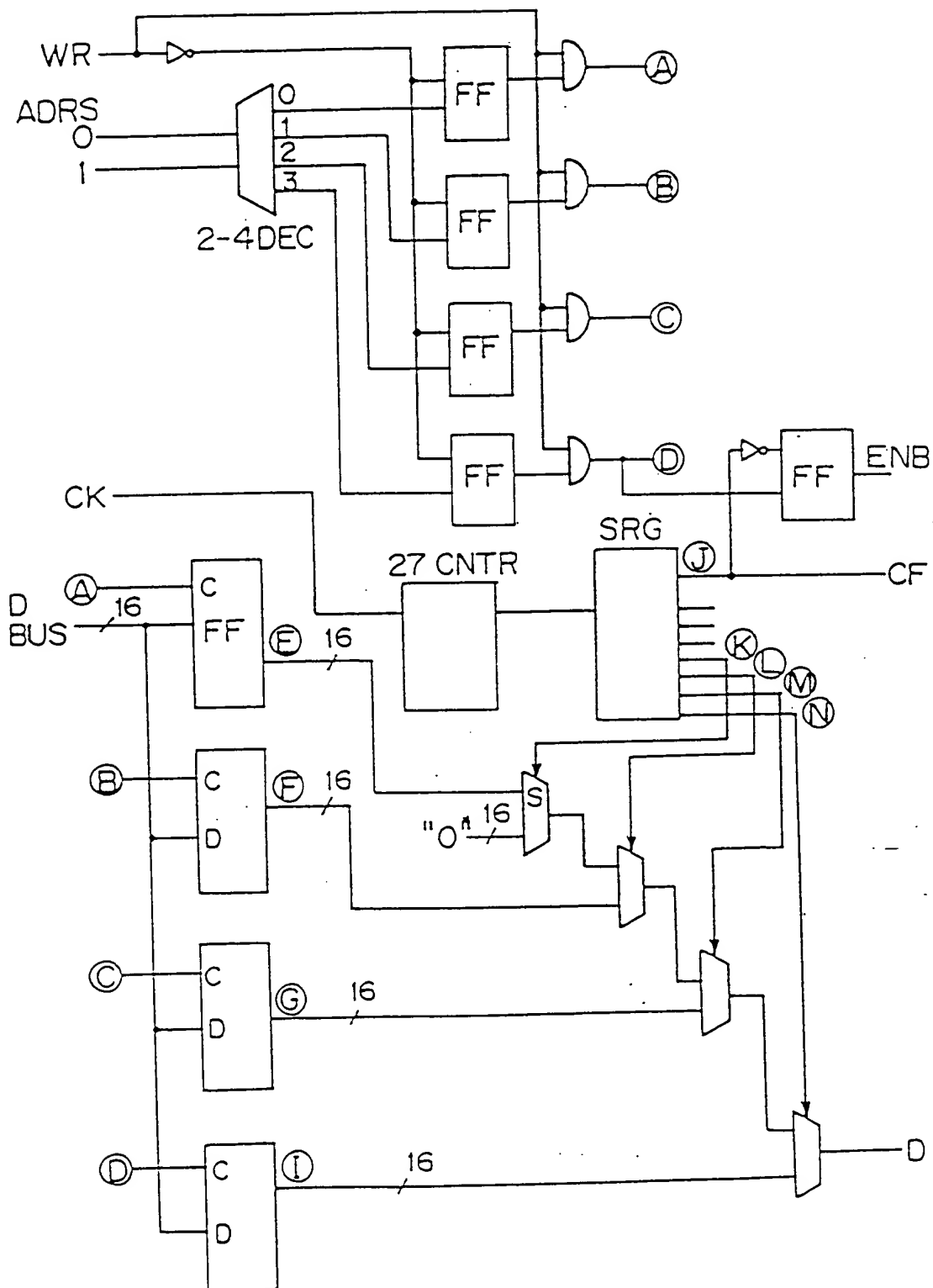
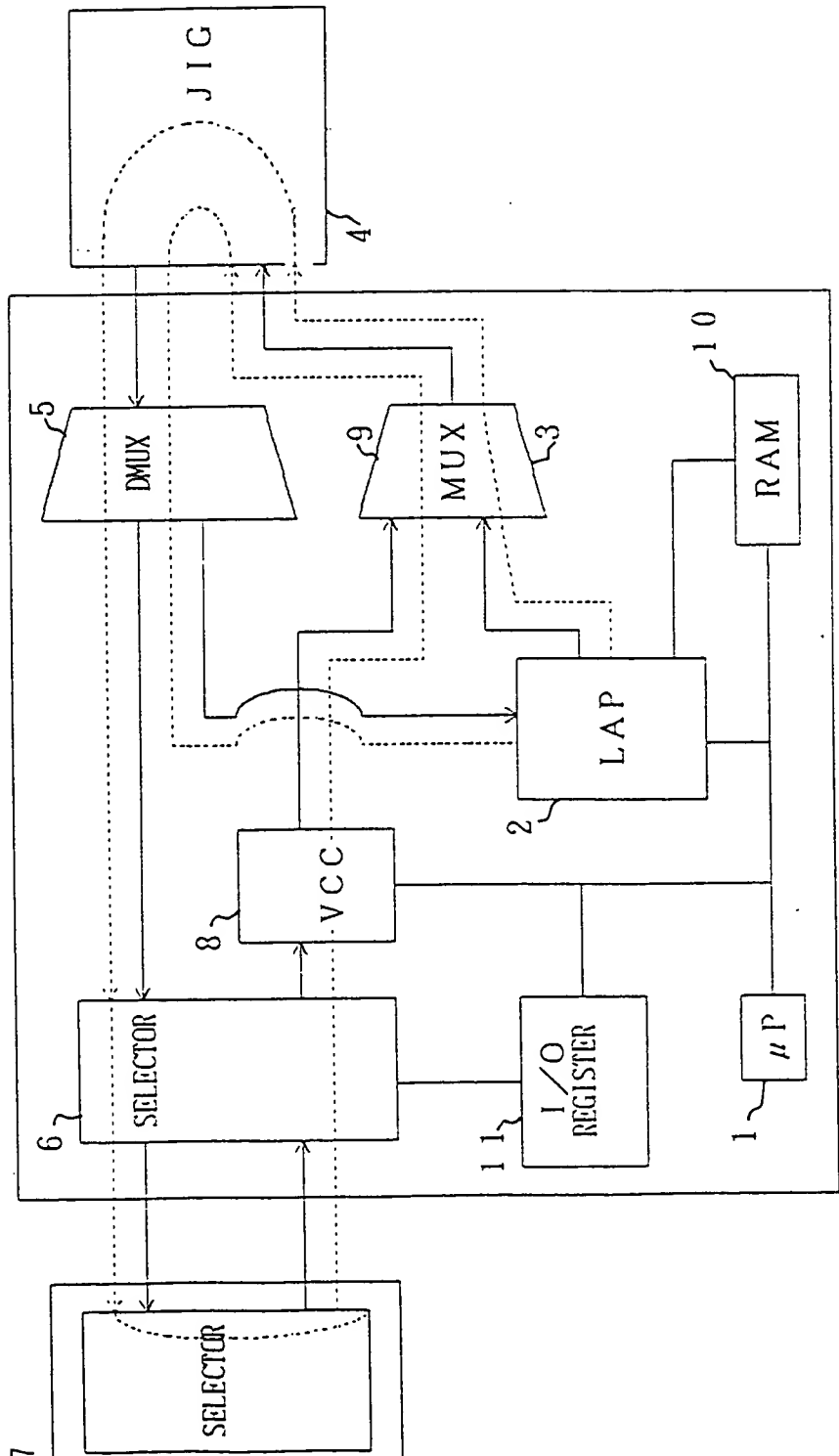


FIG. 814

FIG. 815



VCC : ROUTING SYMBOL ASSIGNING UNIT CELL DATA FLOW
 LAP : LAP COMMUNICATING UNIT
 μP : MICROPROCESSOR
 MUX : MULTIPLEXING
 DMUX : DEMULTIPLEXING

FIG. 816

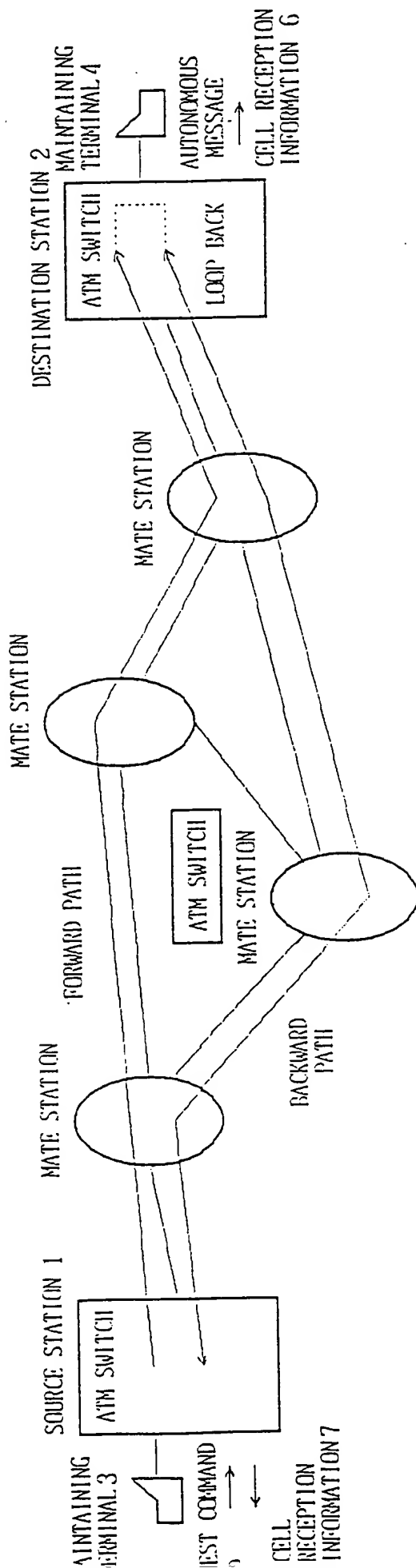


FIG. 817

669220-242220

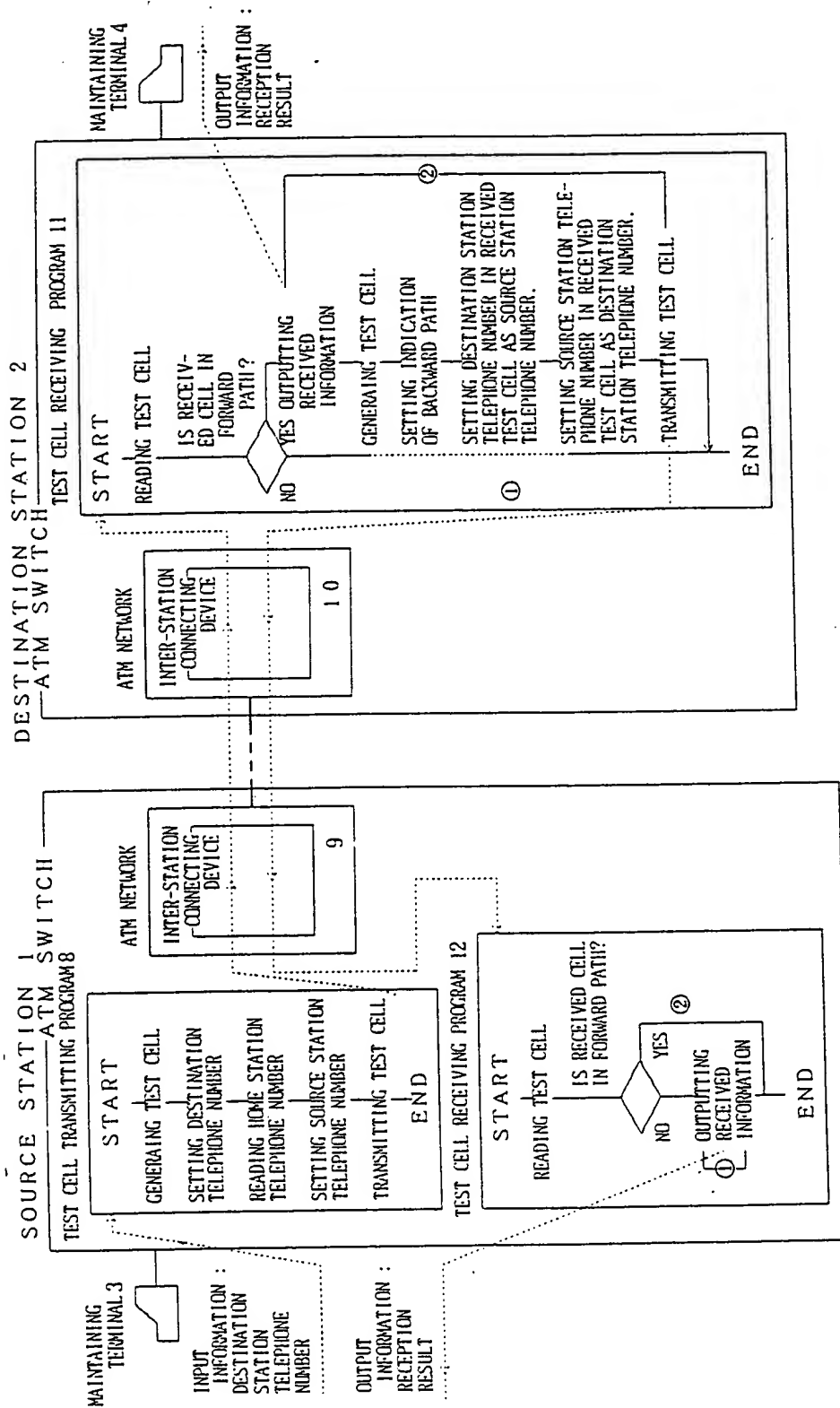
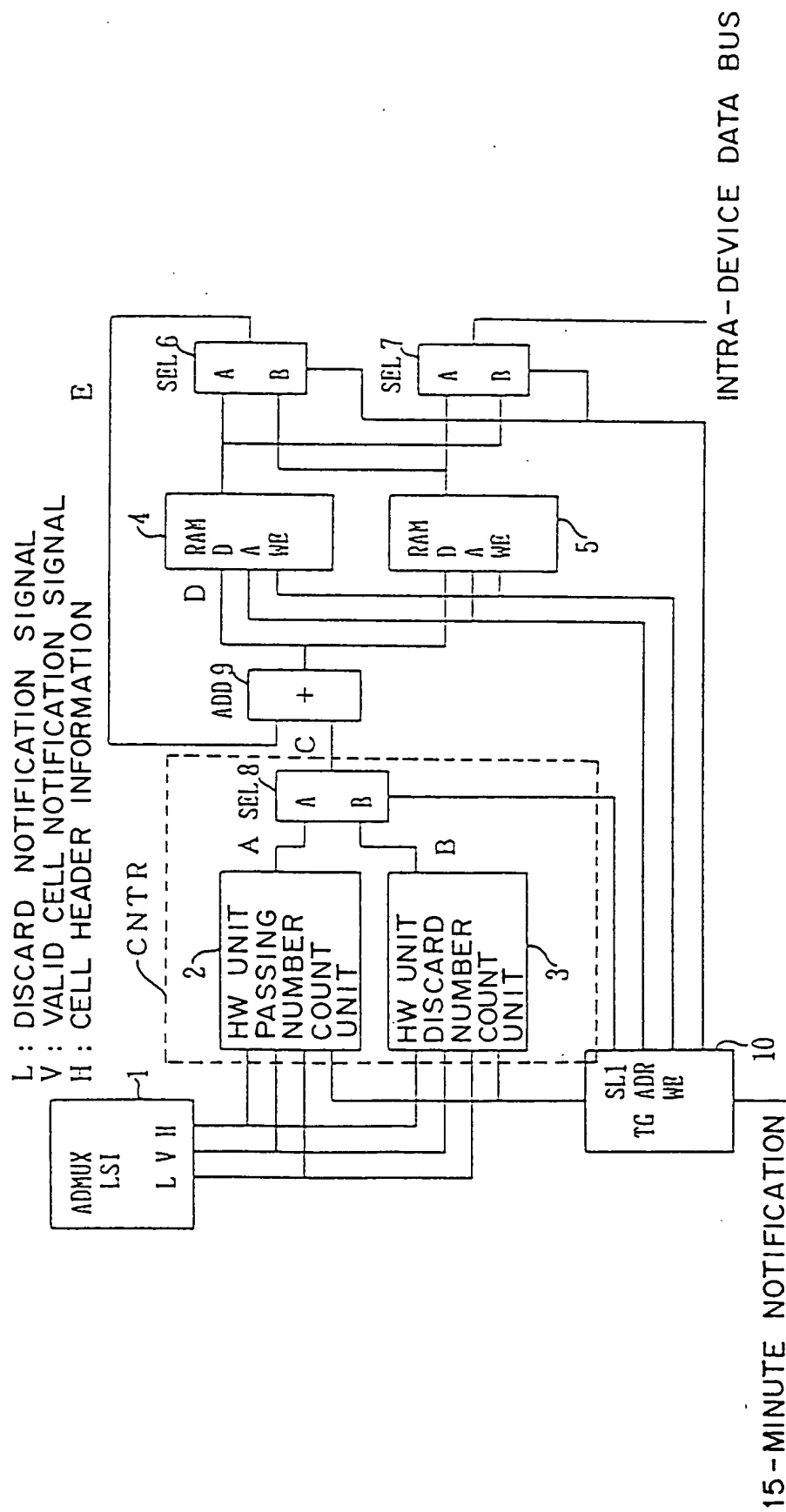


FIG. 818

[illegible]

00H	DISCARD CELL NUMBER	LOWER	8 bit
01H	DISCARD CELL NUMBER		8 bit
02H	DISCARD CELL NUMBER		8 bit
03H	DISCARD CELL NUMBER	HIGHER	8 bit
04H	PASSING CELL NUMBER	LOWER	8 bit
05H	PASSING CELL NUMBER		8 bit
06H	PASSING CELL NUMBER		8 bit
07H	PASSING CELL NUMBER	HIGHER	8 bit

FIG. 820

00000000000000000000000000000000

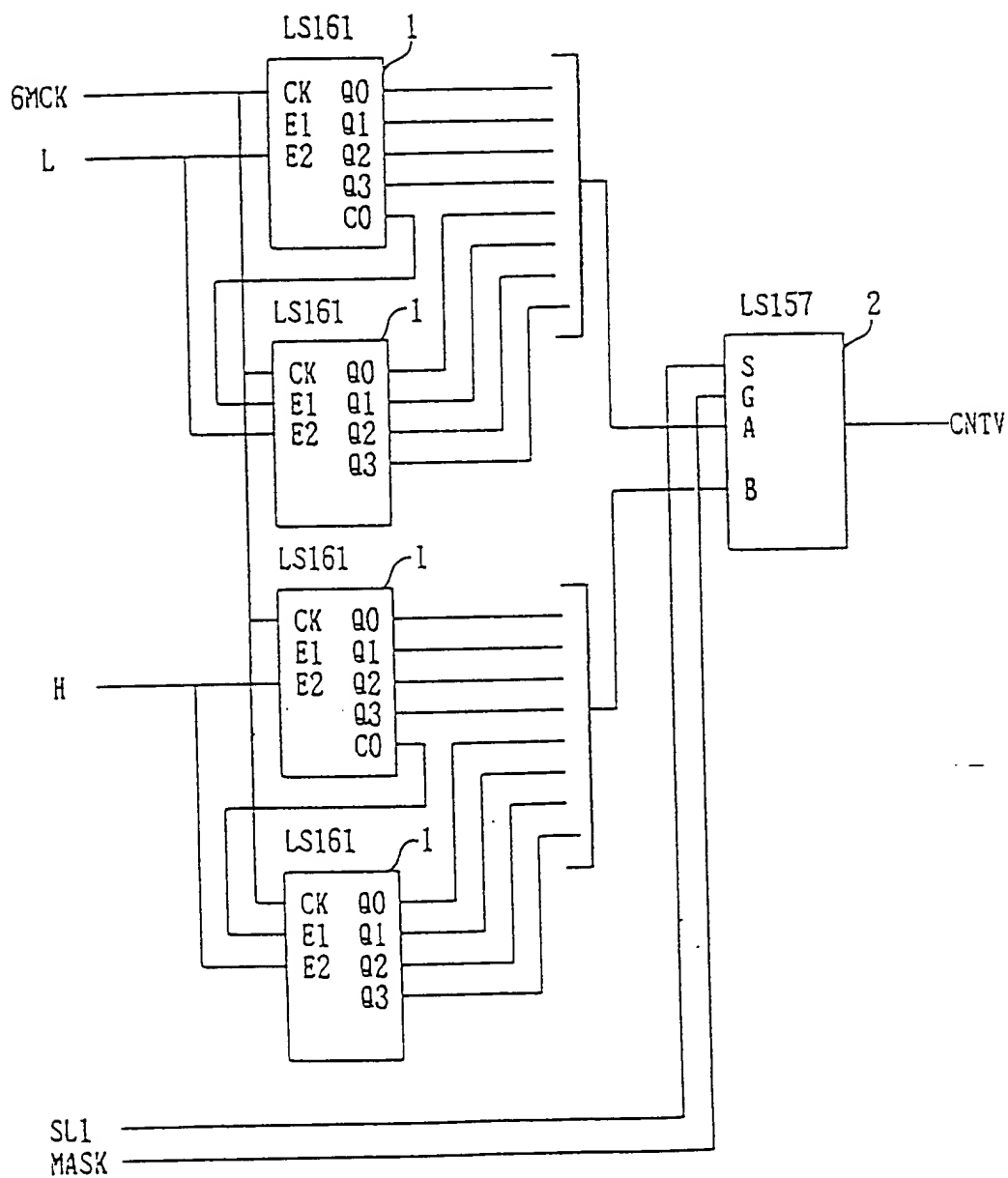


FIG. 821

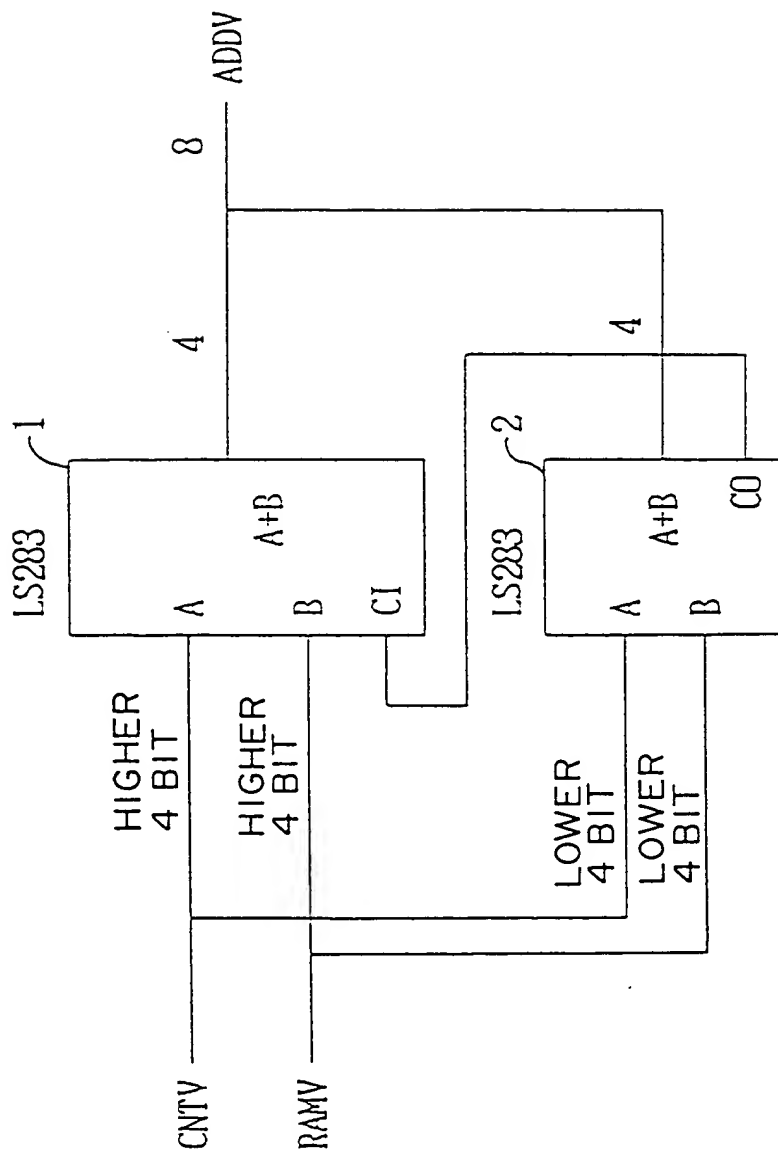


FIG. 822

The logic diagram illustrates the internal architecture of the C2568CR microcontroller. Key components include:

- C2568CR:** The central microcontroller unit with pins for DATA 0-7, RCLPL, TC, CE, and R.
- RDB (Read Data Buffer):** A 256-word buffer connected to the data bus and the C2568CR.
- Registers and Counters:**
 - FDC (First Data Counter):** Connected to the C2568CR and the RDB.
 - FRS (First Register Set):** Connected to the C2568CR and the FDC.
 - FQ (First Queue):** Connected to the C2568CR and the FRS.
 - TC (Timer Counter):** Connected to the C2568CR and the FQ.
- Control Logic:**
 - CLK_68:** The main clock signal for the C2568CR.
 - RAMW, RAMWD, RAMW:** Signals for RAM write and read operations.
 - RAWO, RAWI:** Signals for RAM output and input.
 - BSELT:** A signal for selecting between different data paths.
 - TBCLR:** A signal for clearing the timer counter.
 - INTOUT, PRTOUT:** Signals for interrupt output and printer output.
- External Connections:**
 - TBLRCO, DCLRO, CLCO, C_CLR:** Control signals for the C2568CR.
 - RAWO, RAWI:** Data signals for the RAM.
 - BSELT:** A signal for selecting between different data paths.
 - TBCLR:** A signal for clearing the timer counter.
 - INTOUT, PRTOUT:** Signals for interrupt output and printer output.

FIG. 823

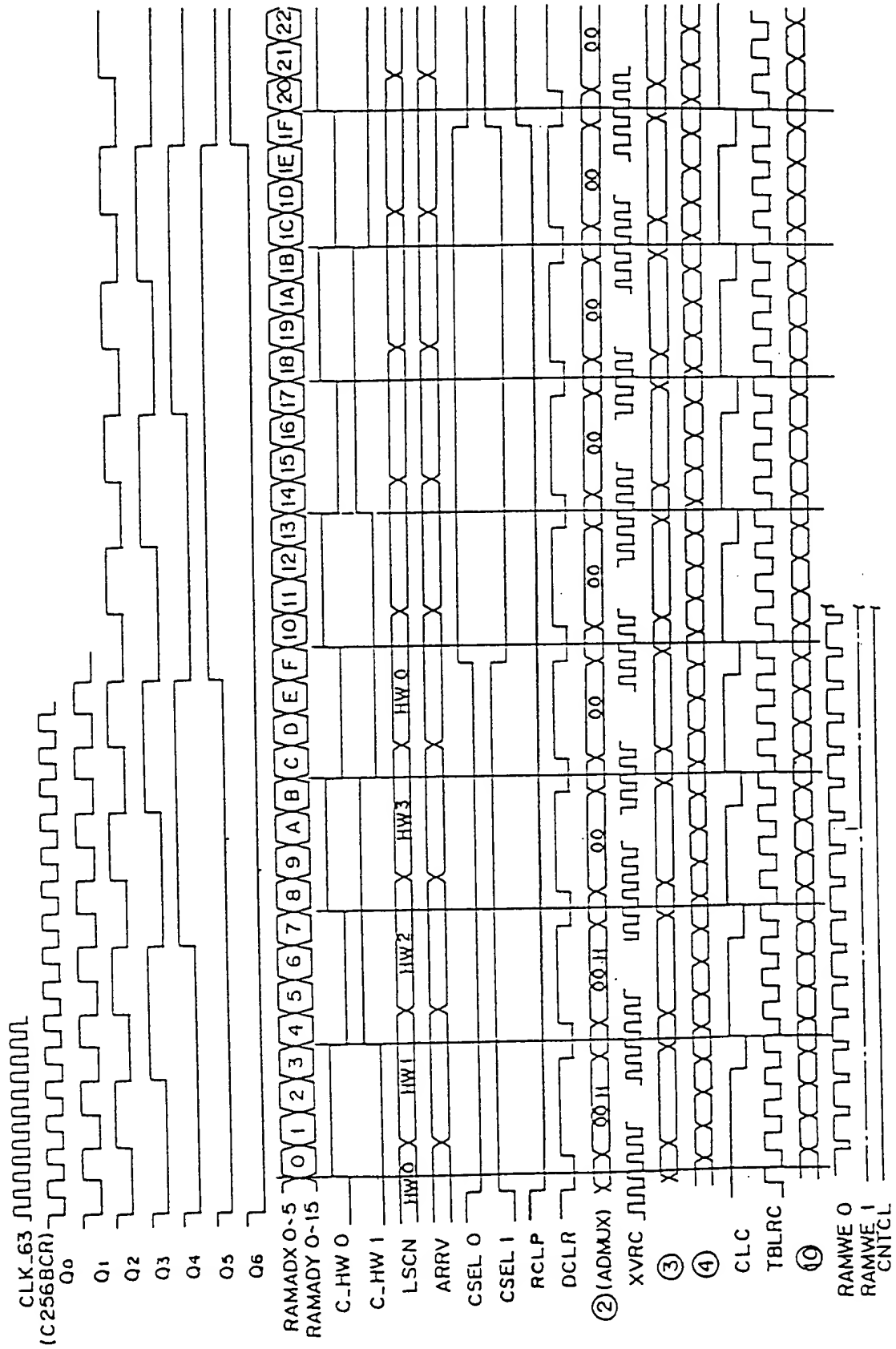


FIG. 824

00920-0122000

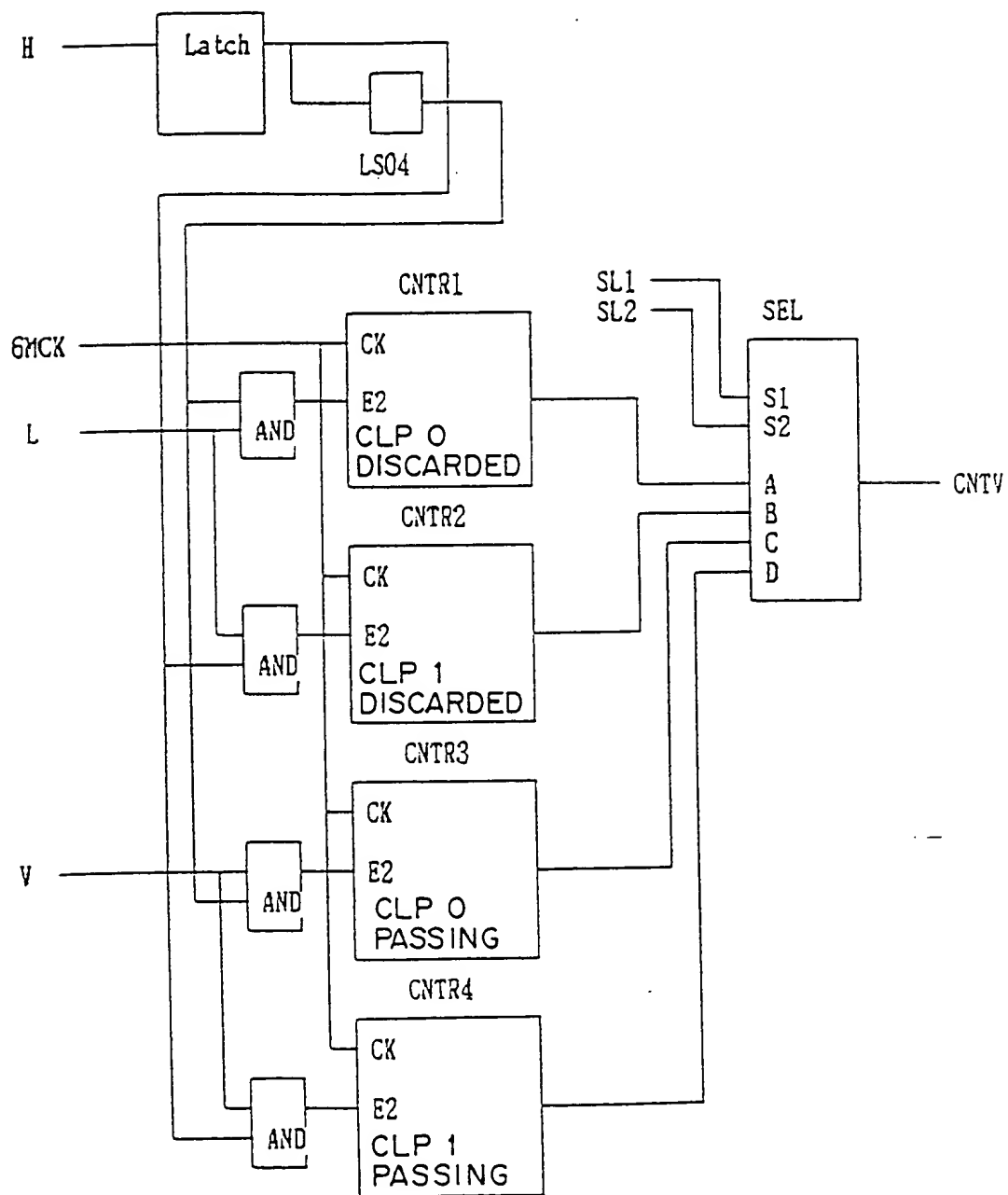


FIG. 825

66360-01-000

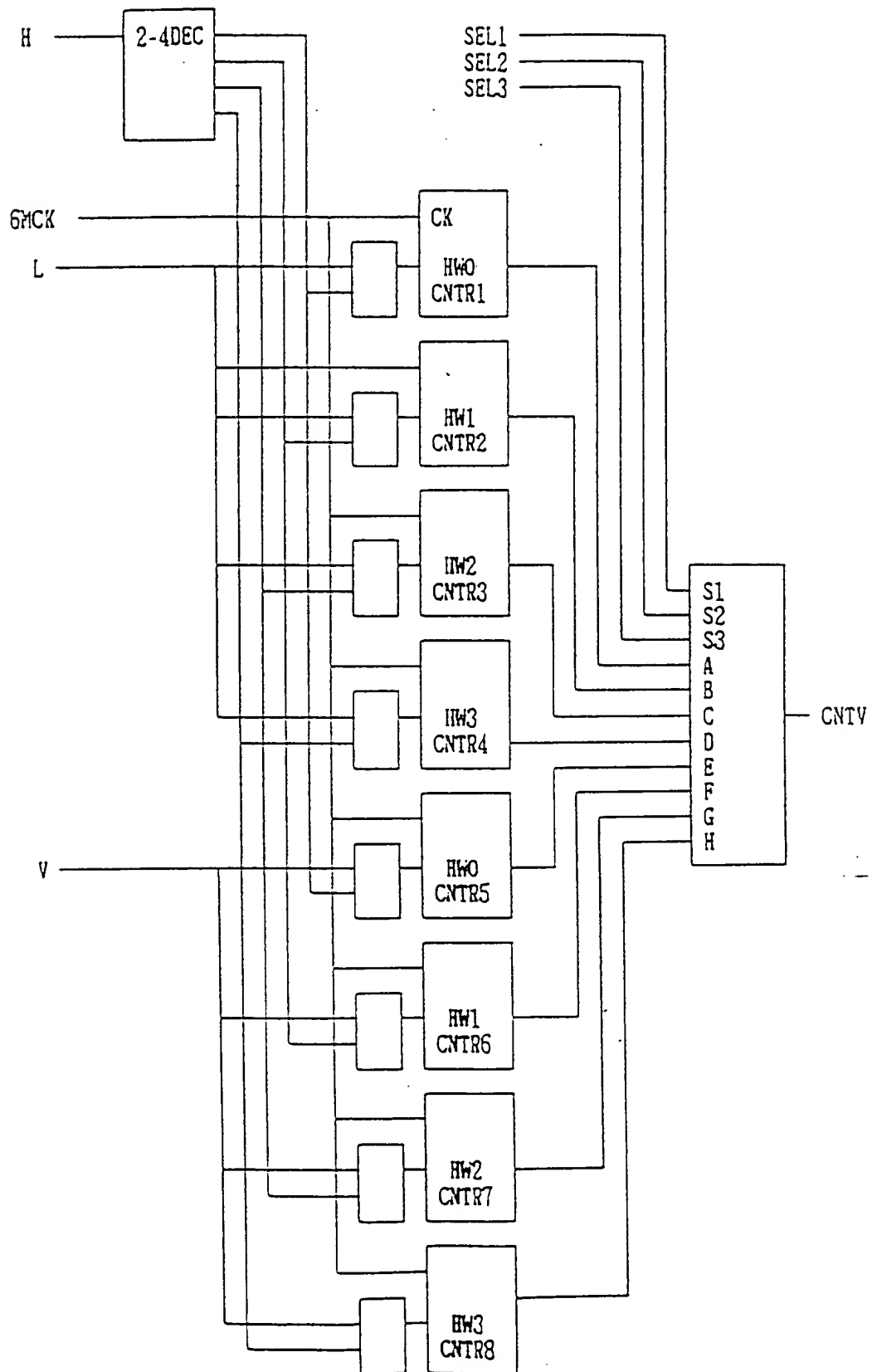


FIG. 826

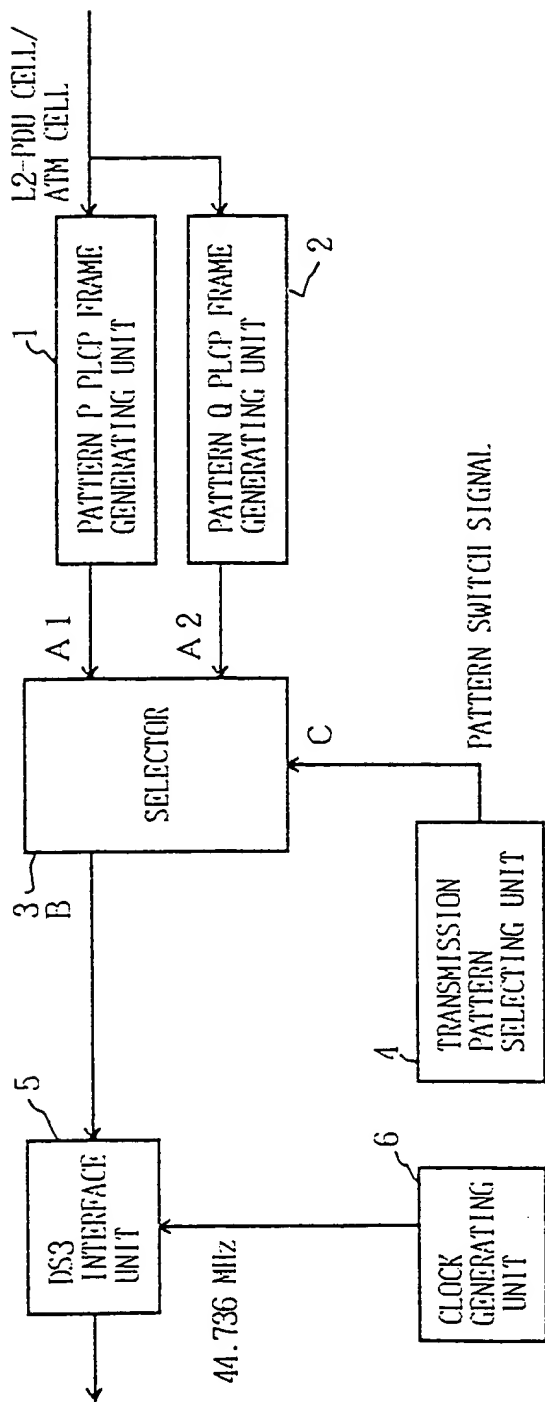


FIG. 827

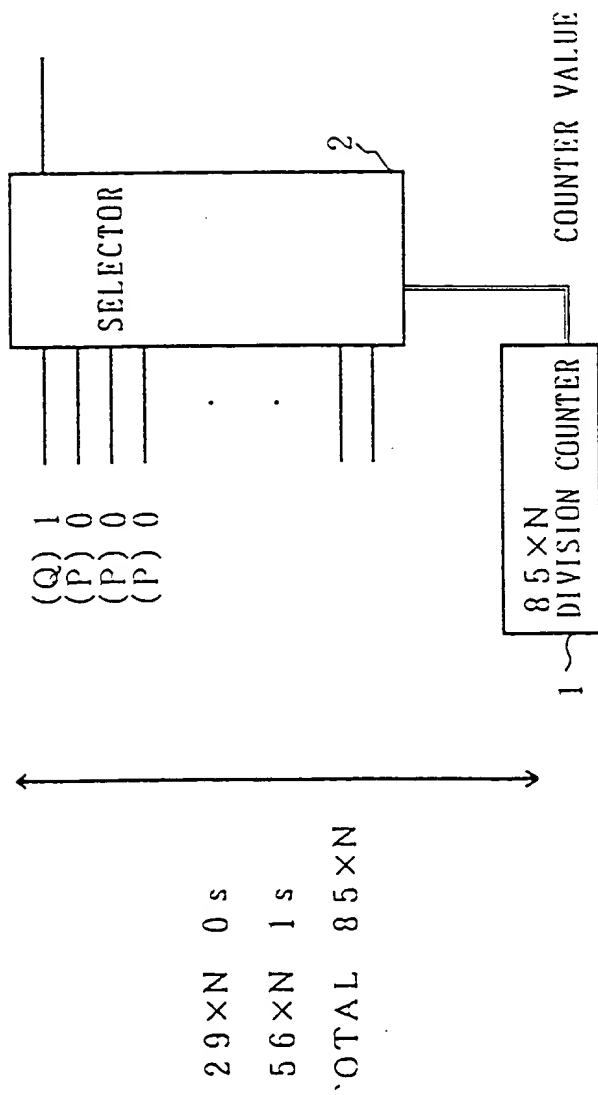


FIG. 828

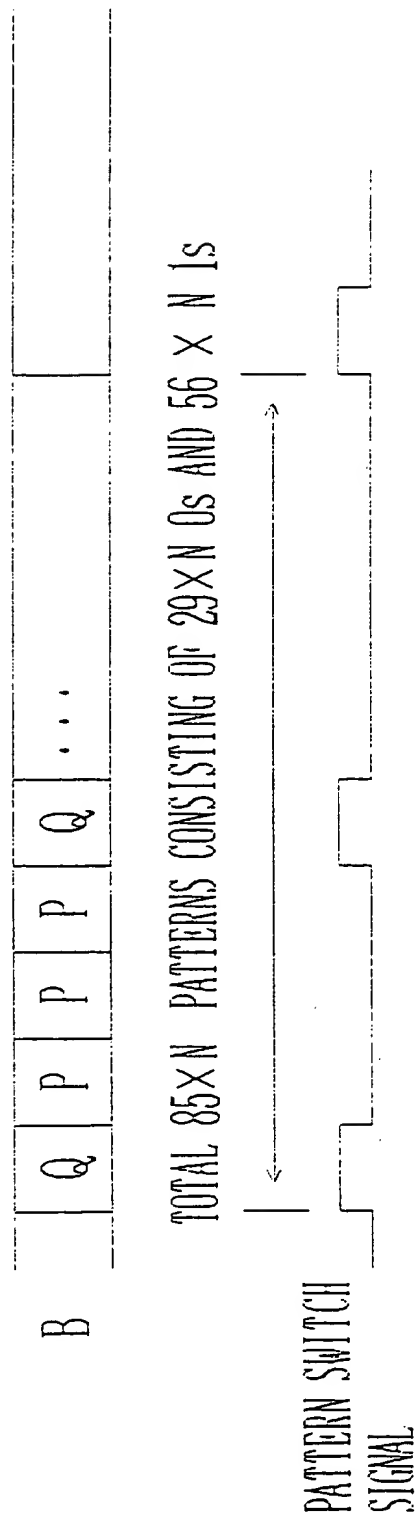


FIG. 829

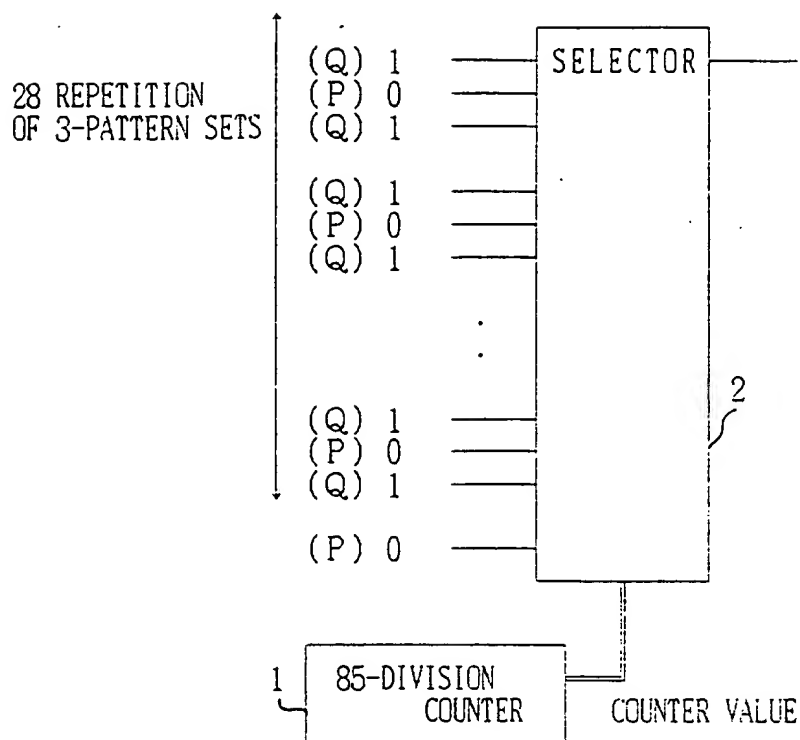


FIG. 830

093724-0369
66920-12260

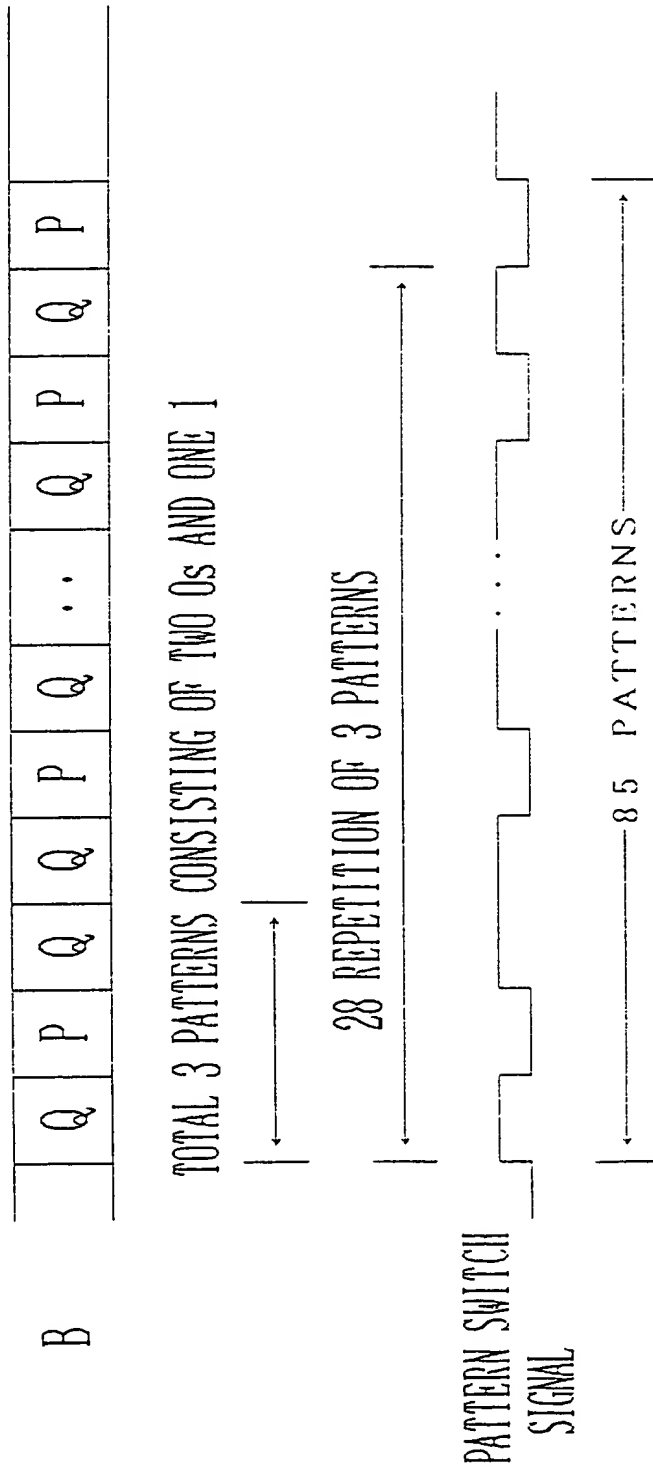
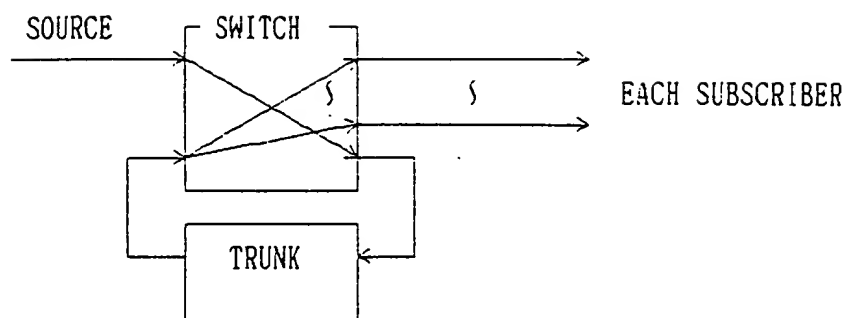


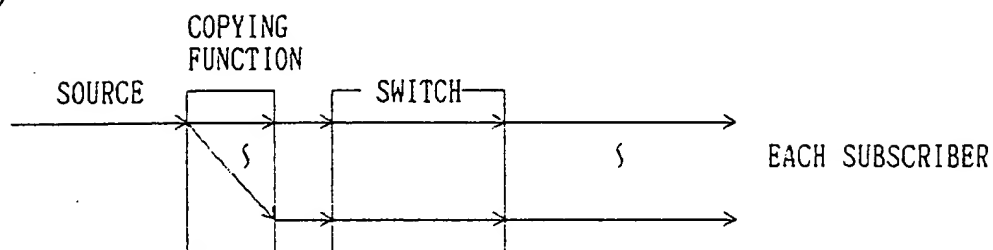
FIG. 831

092724-03699
669220-22250

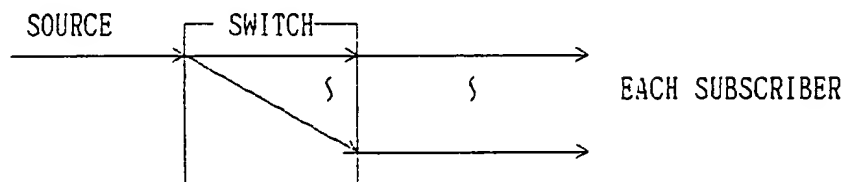
(a)



(b)



(c)



F I G. 8 3 2

SYSTEM	MERITS	DEMERITS
TRUNK SYSTEM	<ul style="list-style-type: none"> • EASY TO CONTROL SWITCHES ONLY POINT-TO-POINT CONNECTION • REASSIGNMENT OF VPI/VCI IS NOT REQUIRED 	<ul style="list-style-type: none"> • TRUNK IS REQUIRED • NUMBER OF PATHS DEPENDS ON CAPACITY OF TRUNK • BAND OF PATH SUPPORTED BY SYSTEM DECREASES FOR TRUNKS • DOUBLE DELAY OVER POINT-TO-POINT CONNECTION BECAUSE OF TEMPORARY ACCOMMODATION IN TRUNK
INPUT COPY SYSTEM	<ul style="list-style-type: none"> • EASY TO CONTROL SWITCHES ONLY POINT-TO-POINT CONNECTION 	<ul style="list-style-type: none"> • REASSIGNMENT OF VPI/VCI IS REQUIRED • COPYING FUNCTION SHOULD BE ADDED • BAND OF PATH SUPPORTED BY SYSTEM DECREASES FOR COPY IN PREVIOUS STEP
INTERNAL COPY SYSTEM	<ul style="list-style-type: none"> • BAND OF PATH SUPPORTED BY SYSTEM IS ALLOWED FOR MAXIMUM CAPACITY OF SYSTEM 	<ul style="list-style-type: none"> • REASSIGNMENT OF VPI/VCI IS REQUIRED • COPYING FUNCTION SHOULD BE INCORPORATED. • COMPLICATED SWITCH CONTROL

FIG. 833

MUX

1st STAGE

2nd STAGE

3rd STAGE

DMUX

POINT-TO-MULTIPOINT CONNECTION

BIT MAP

BIT MAP

BIT MAP

GENERATING BIT MAP BY DECODING ;VPI/VCI

FIG. 834



FIG. 835

66960-0366

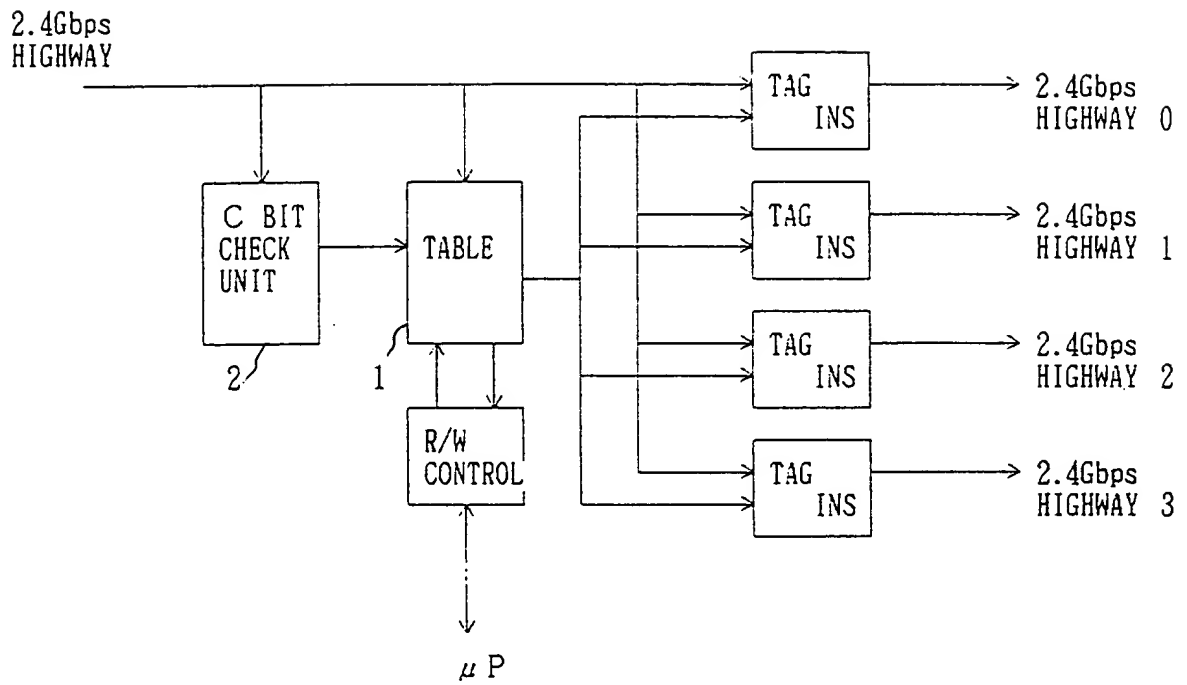


FIG. 836

009907E124250

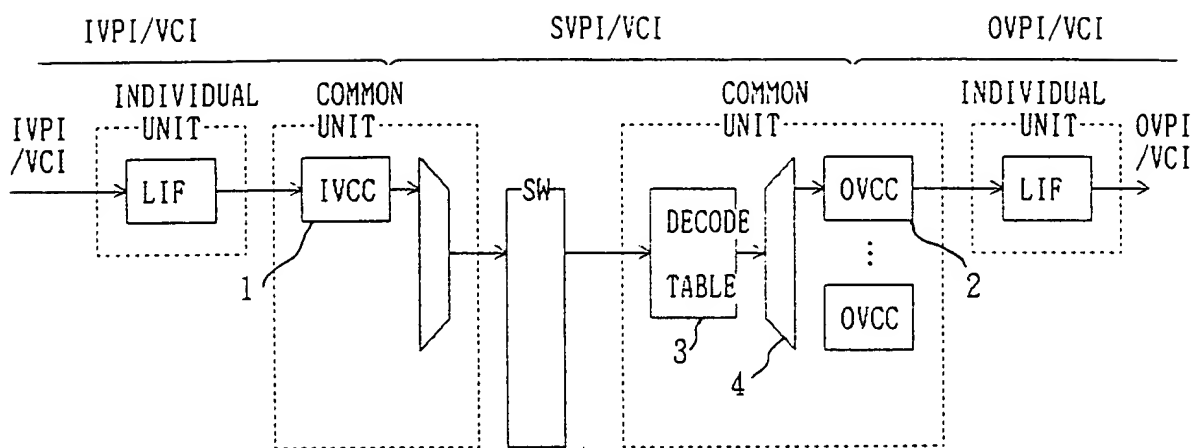


FIG. 837

66920-6122260

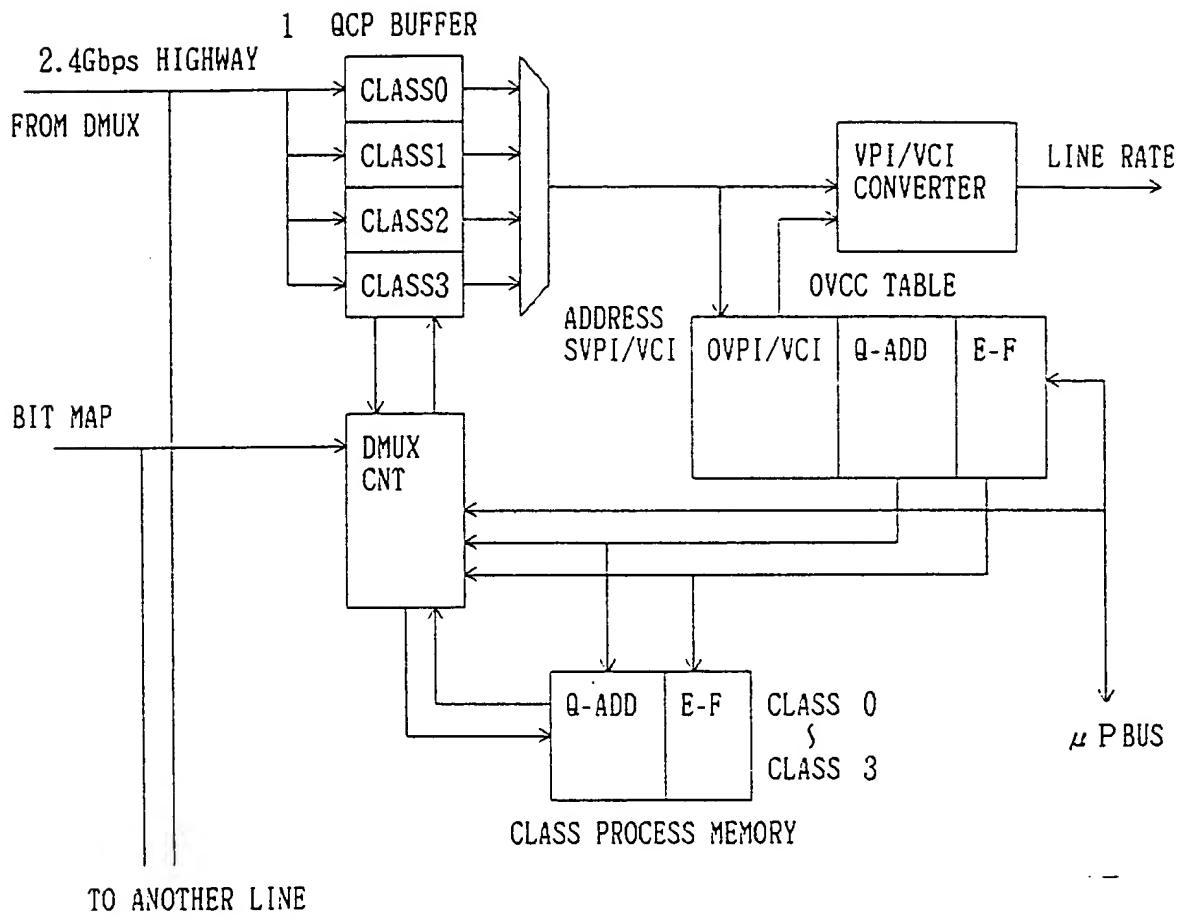


FIG. 838

00000-00000

	ADDRESS	CONTENTS OF OVCC TABLE OVPI/VCI	Q-ADD	E-F
POINT-TO POINT CONNECTION	SVPI/VCI	OVPI/VCI	D.C.	1
POINT-TO-MULTIPOINT CONNECTION	SVPI/VCI	OVPI/VCI	ADDRESS	x

FIG. 839

00000000000000000000000000000000

ADDRESS	OVPI/VC1	Q-ADD	E-F	
a	b0	c0	0	← CELL TO TRANSMISSION 1
c0	b1	c1	0	← CELL TO TRANSMISSION 2
c1	b2	c2	0	← CELL TO TRANSMISSION 3
c2	b3	D.C.	1	← CELL TO TRANSMISSION 4

FIG. 840

START

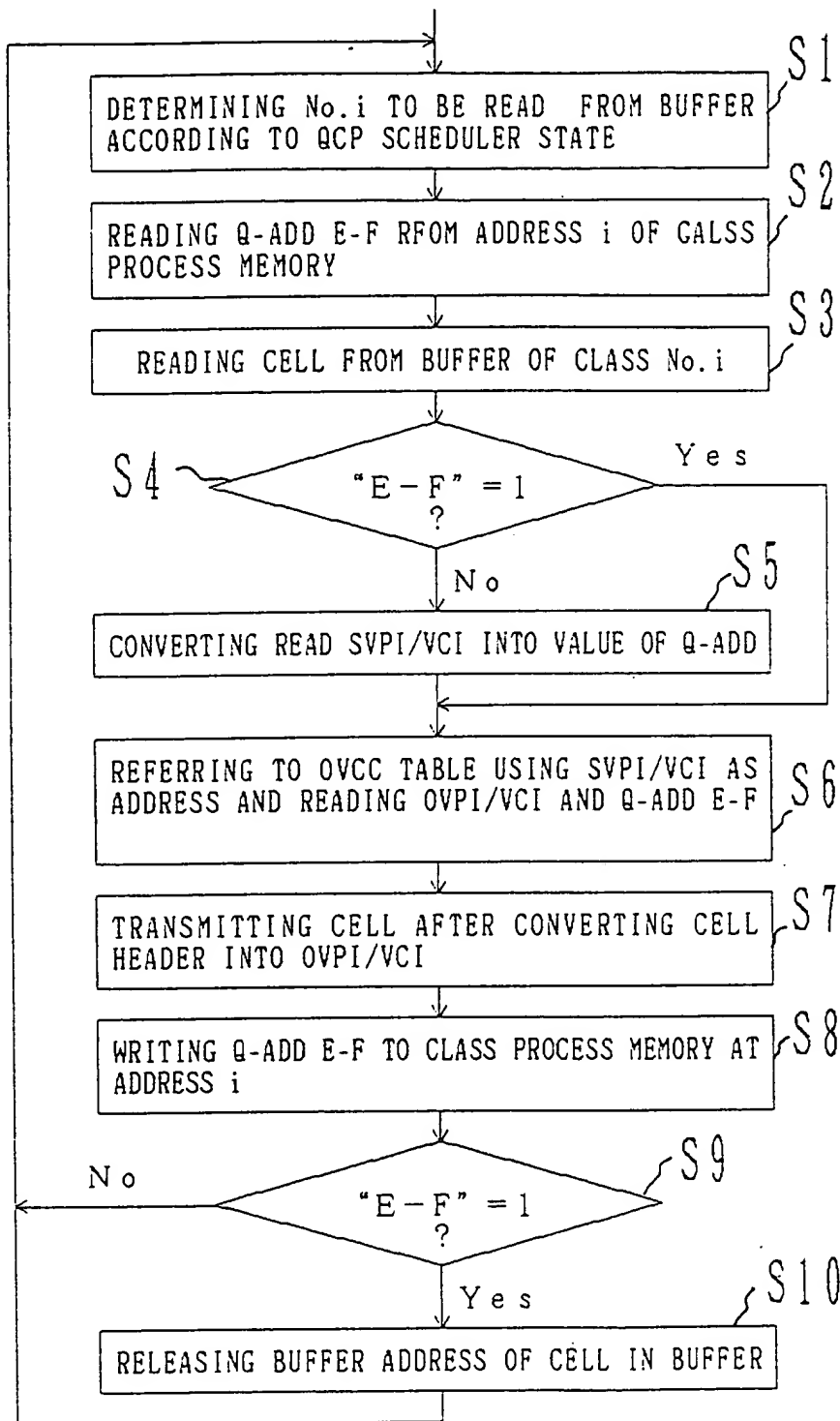
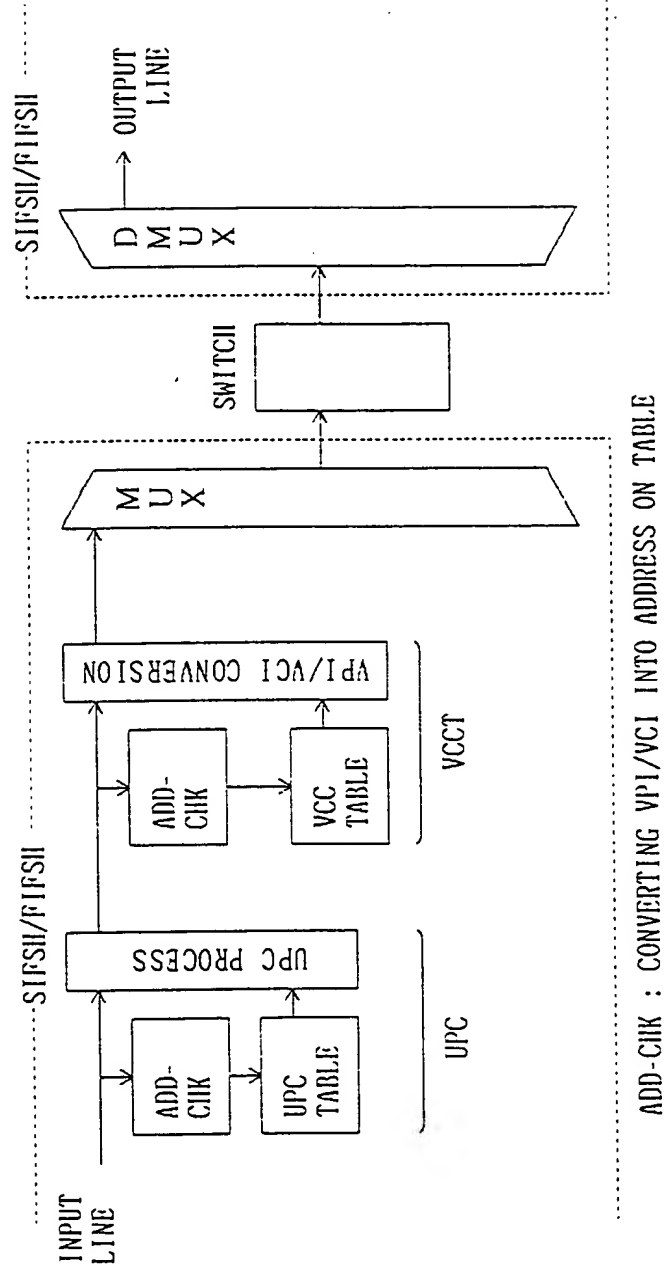
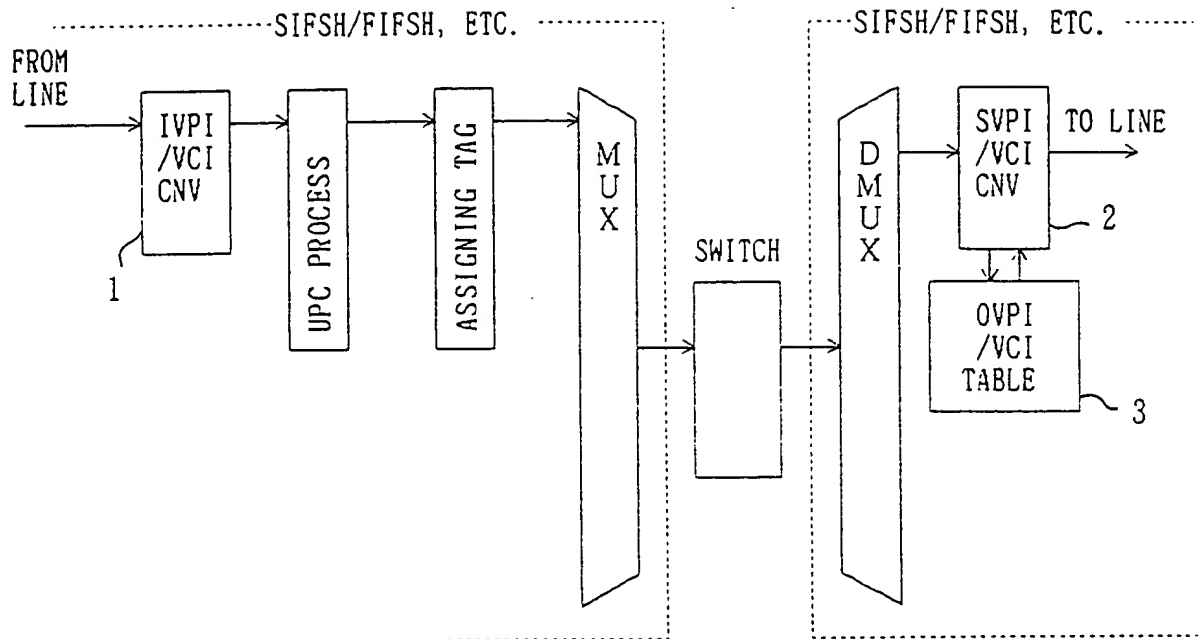


FIG. 841



ADD-CHK : CONVERTING VPI/VCI INTO ADDRESS ON TABLE

FIG. 842



IVPI/VCI CNV : CONVERSION FROM IVPI/VCI INTO SVPI/VCI
 SVPI/VCI CNV : CONVERSION FROM SVPI/VCI INTO OVPI/VCI

F I G. 8 4 3

Diagram illustrating the structure of a 53-bit data structure, divided into three main sections:

- TAG:** Occupies bits 0 through 1.
- HEADER:** Occupies bits 2 through 5.
- PAYLOAD:** Occupies bits 6 through 53.

Bit positions are marked on the left (0, 1, 2, 3, 4, 5, 6, 53) and top (B7, B6, B5, B4, B3, B2, B1, B0).

FIG. 844

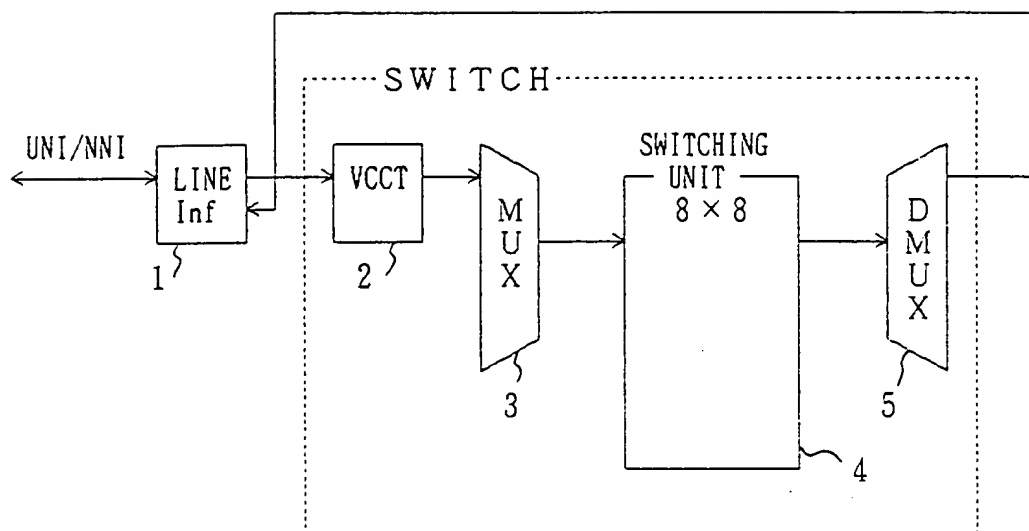


FIG. 845

669260-ET2260

66920-6162260

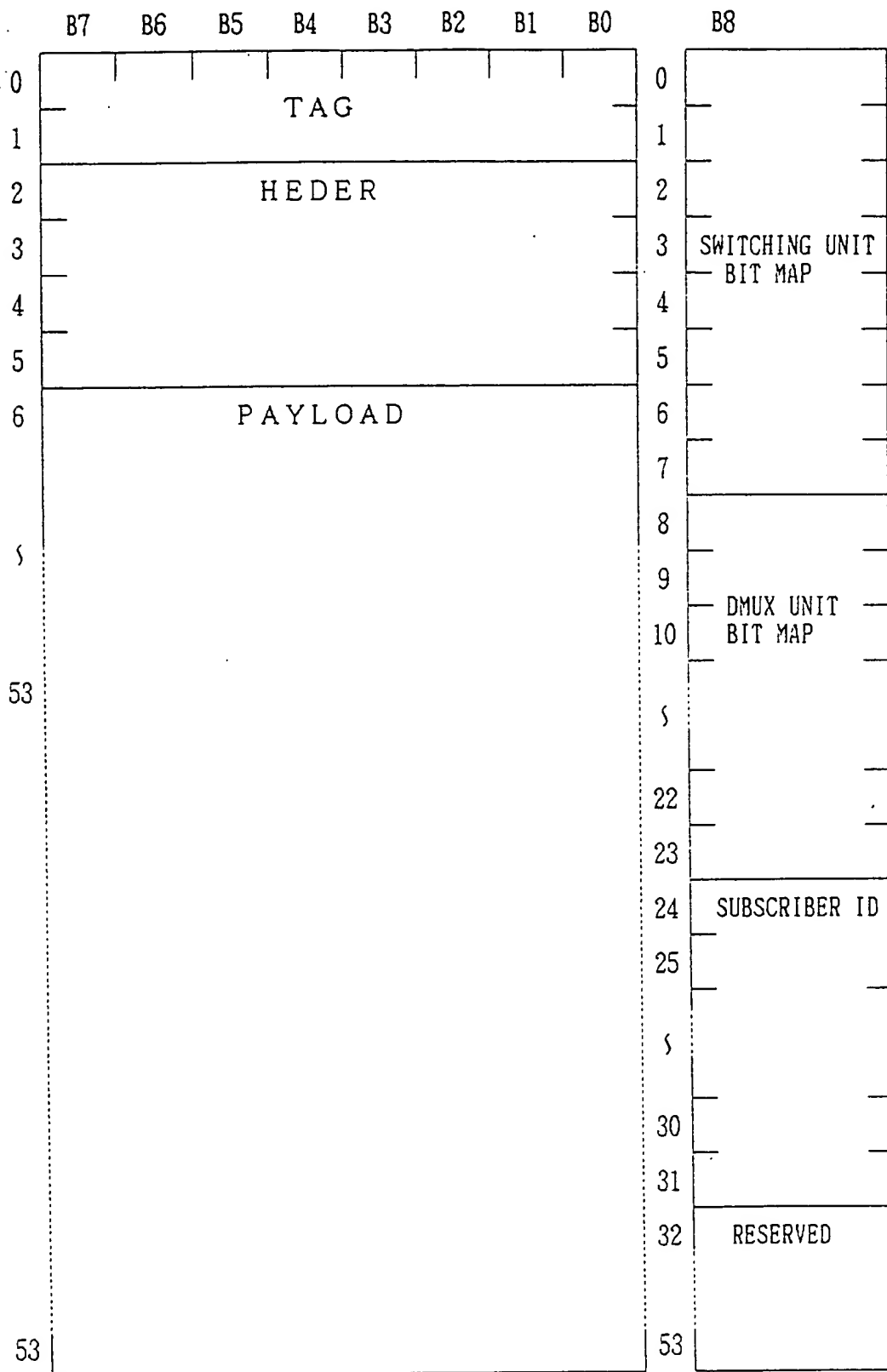


FIG. 846

669260-ET22260

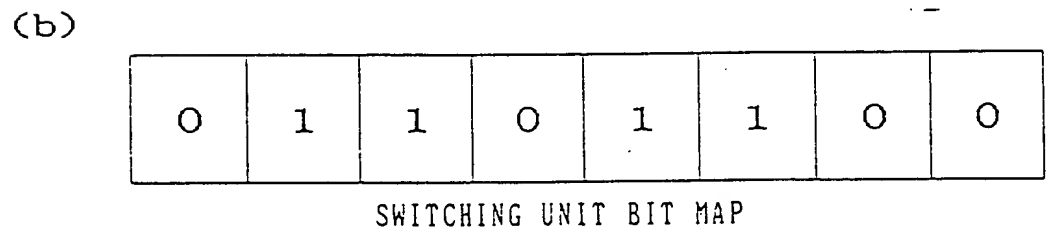
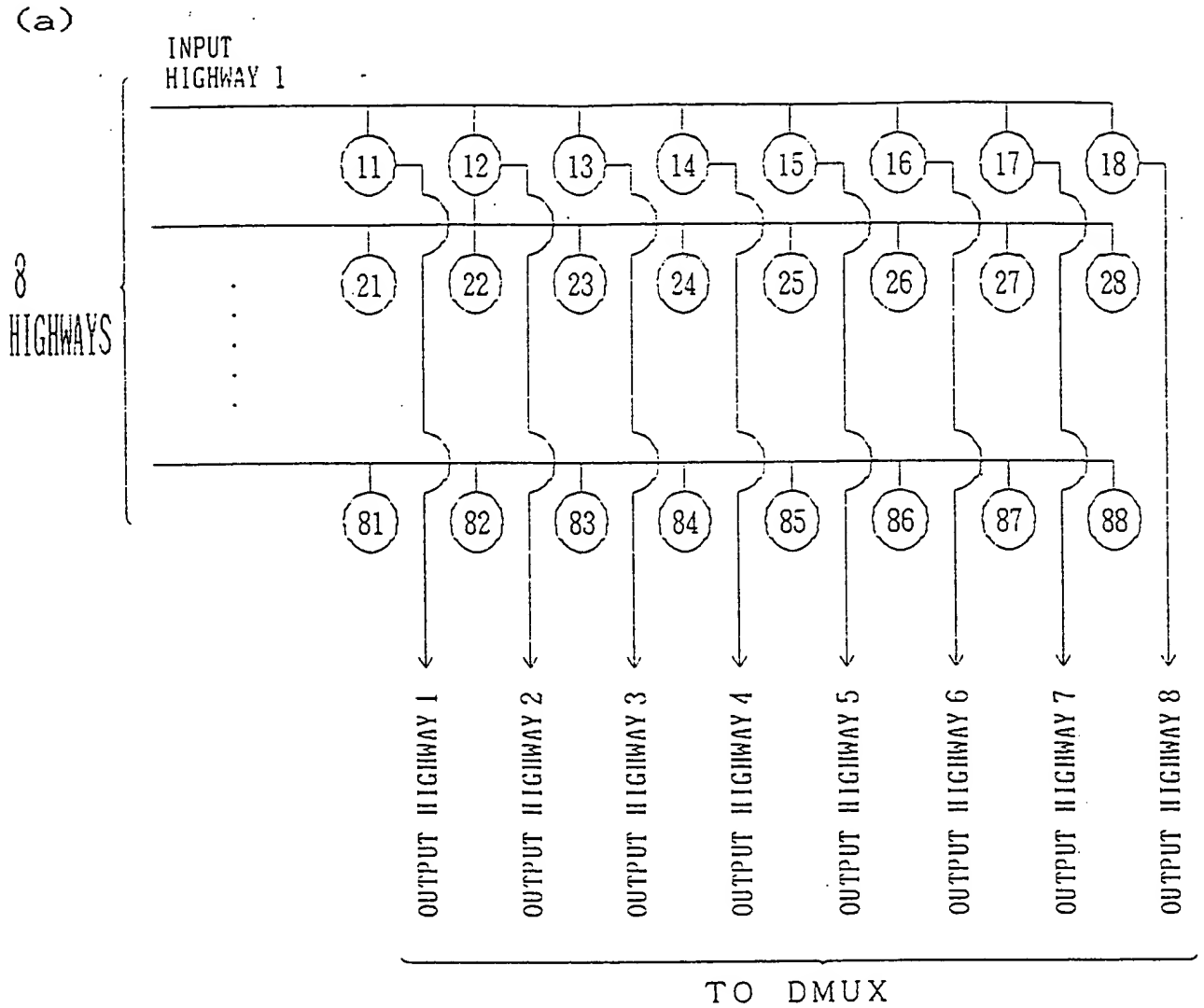


FIG. 847

669260 2122260

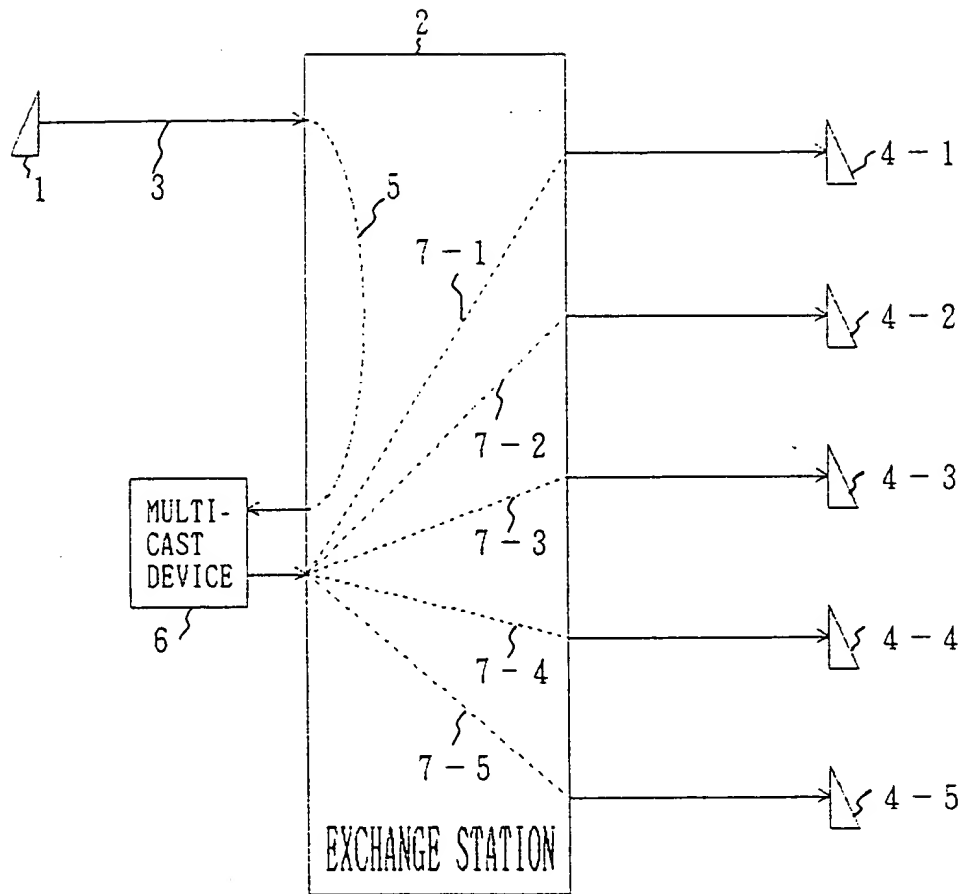


FIG. 848

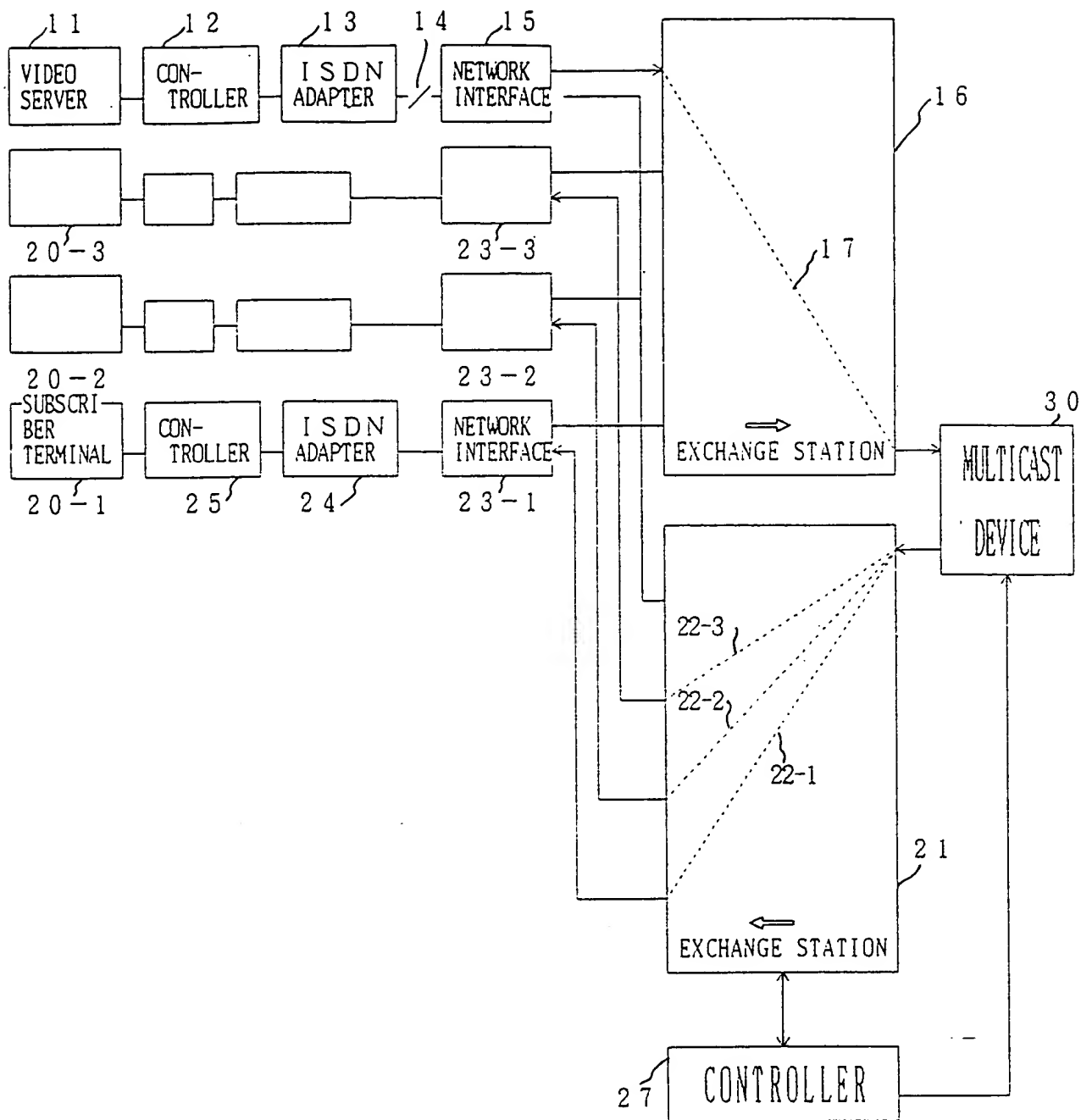


FIG. 849

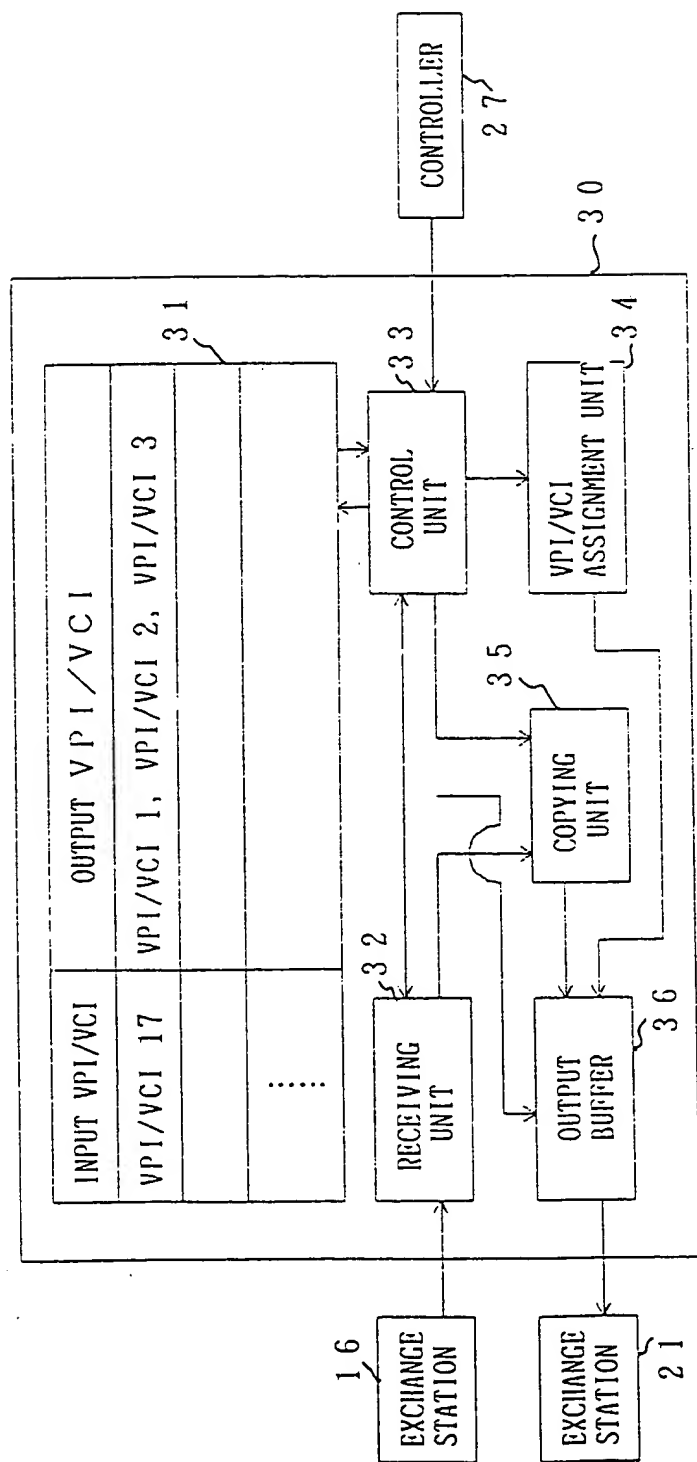
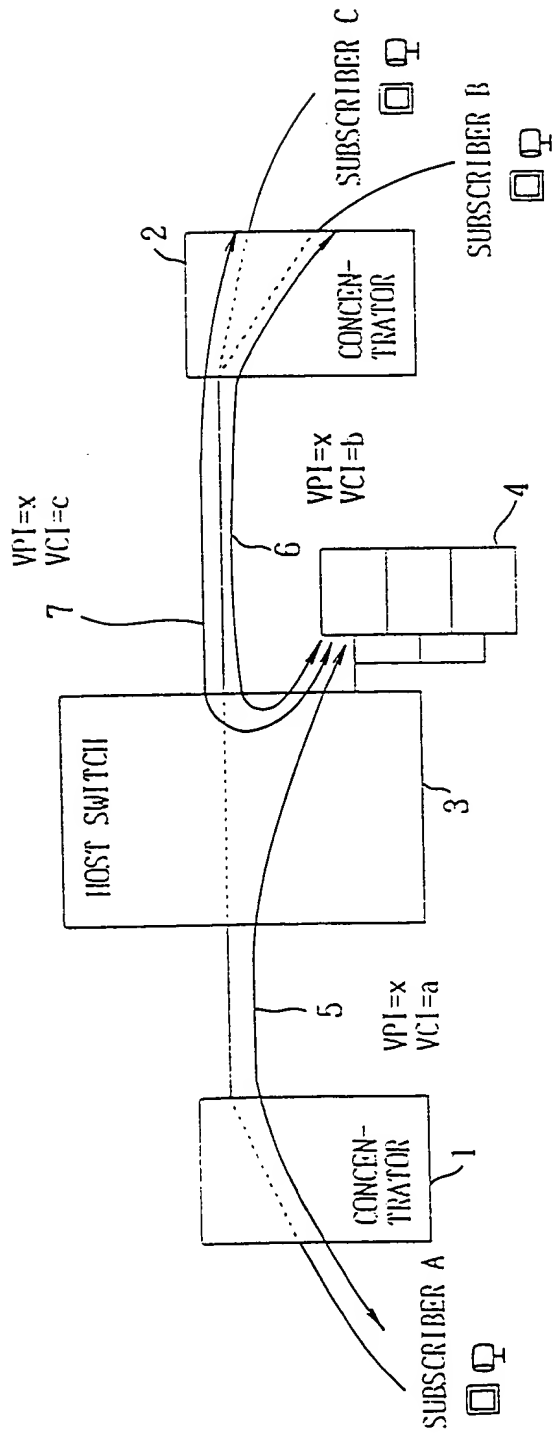


FIG. 850



MULTIPLE SUBSCRIBER COMMUNICATIONS TRUNK
(IMAGE, VOICE MIXER)

FIG. 851

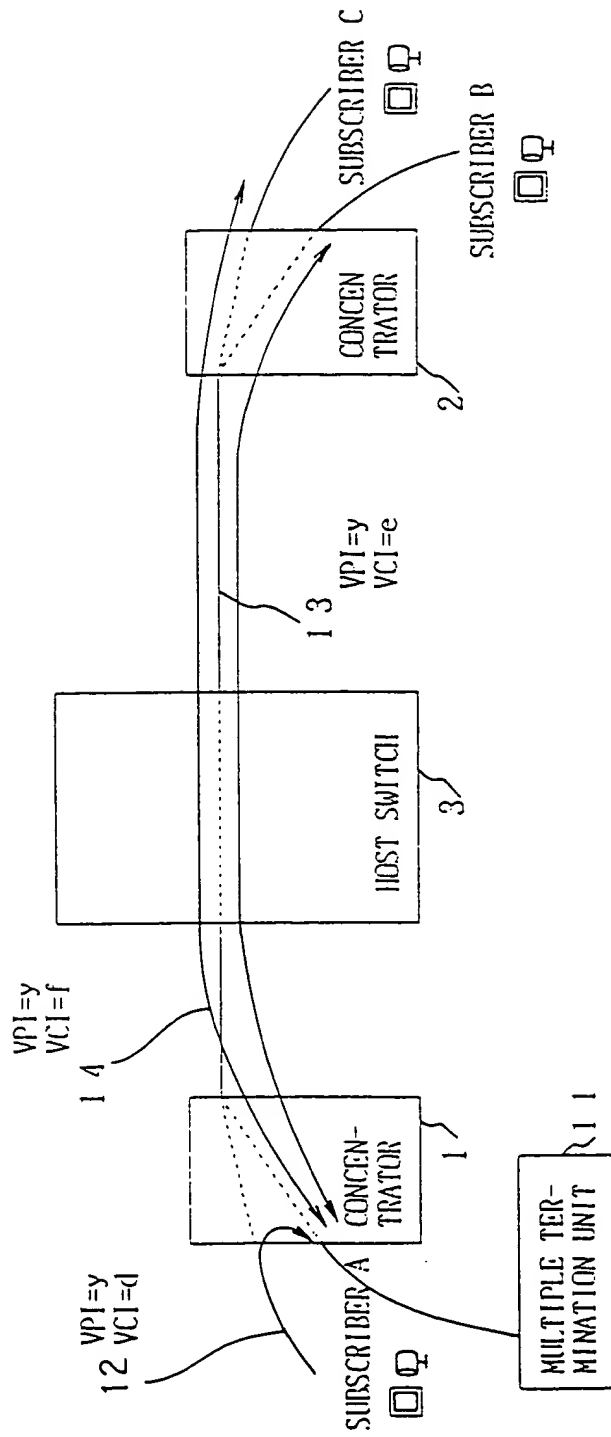


FIG. 852

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

RECEIVING THREE-
SUBSCRIBER
COMMUNICATIONS REQUEST

CALLING THIRD SUBSCRIBER

THIRD SUBSCRIBER BEING CALLED

RESPONSE

SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK

UPDATING NUMBER OF CONNECTED SUBSCRIBERS ☒ 50

TEMPORARILY DISCONNECTING PATH BETWEEN
TWO SUBSCRIBERS

CONNECTING THREE SUBSCRIBERS THROUGH
PREDETERMINED VPI/VCI

THREE-SUBSCRIBER COMMUNICATIONS IN PROCESS

FIG. 853

00000-00000

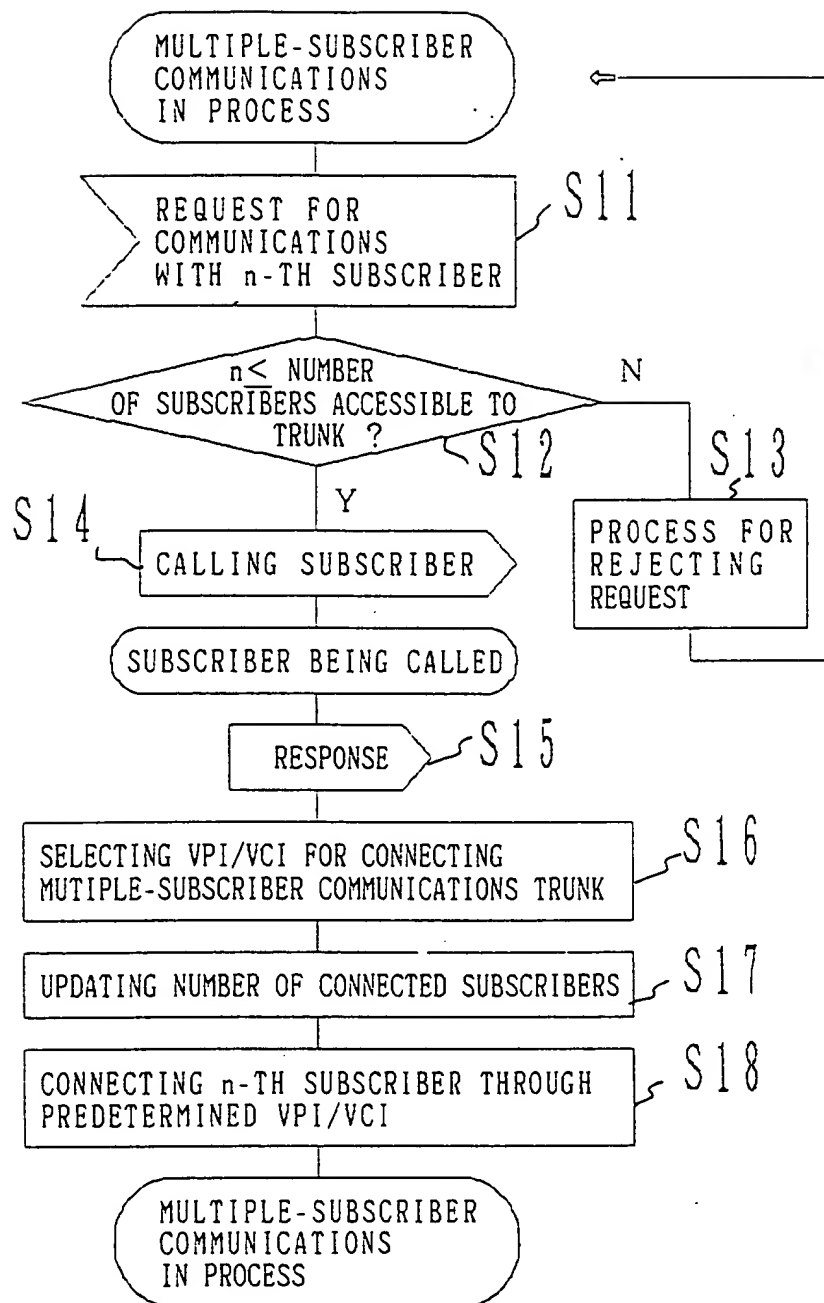


FIG. 854

```

graph TD
    A((A)) --> START([START])
    START --> S21[REQUEST FOR MULTIPLE-SUBSCRIBER COMMUNICATIONS + GROUP IDENTIFICATION NUMBER]
    S21 --> S22{IS TRUNK USED WITH GROUP IDENTIFICATION NUMBER ?}
    S22 -- N --> S25[HUNTING FOR MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S22 -- Y --> S23{NUMBER OF SUBSCRIBERS ACCESSIBLE TO TRUNK ?}
    S23 -- N --> S24[PROCESS OF REJECTING REQUEST]
    S23 -- Y --> S26[SELECTING VPI/ VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S24 --> A2((A))
    S25 --> S26
    S26 --> S27[UPDATING NUMBER OF CONNECTED SUBSCRIBERS]
    S27 --> S28[CONNECTING n-TH SUBSCRIBER THROUGH PREDETERMINED VPI/VCI]
    S28 --> END([MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS])
  
```

FIG. 855

```

graph TD
    A([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> B[RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST]
    B --> C[CALLING THIRD SUBSCRIBER]
    C --> D([THIRD SUBSCRIBER BEING CALLED])
    D --> E[RESPONSE]
    E --> F[SELECTING VPI/VCI FOR CONNECTING MULTIPLE-TERMINATION UNIT]
    F --> G[UPDATING NUMBER OF CONNECTED SUBSCRIBERS]
    G --> H[TEMPORARILY DISCONNECTING PATH BETWEEN TWO SUBSCRIBERS]
    H --> I[CONNECTING THREE SUBSCRIBERS THROUGH PREDETERMINED VPI/VCI]
    I --> J([THREE-SUBSCRIBER COMMUNICATIONS IN PROCESS])
  
```

FIG. 856

```

graph TD
    Start([MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> Request[/REQUEST FOR COMMUNICATIONS WITH n-TH SUBSCRIBER/]
    Request --> Decision{n ≤ NUMBER OF SUBSCRIBERS ACCESSIBLE TO TRUNK ?}
    Decision -- Y --> Calling[CALLING SUBSCRIBER]
    Calling --> Called([SUBSCRIBER BEING CALLED])
    Called --> Response[/RESPONSE/]
    Response --> Select[SELECTING VPI/VCI FOR CONNECTING MULTIPLE-TERMINATION UNIT]
    Select --> Update[UPDATING NUMBER OF CONNECTED SUBSCRIBERS]
    Update --> Connect[CONNECTING n-TH SUBSCRIBER THROUGH PREDETERMINED VPI/VCI]
    Connect --> End([MULTIPLE-SUBSCRIBER COMMUNICATIONS IN PROCESS])
    Decision -- N --> Reject[PROCESS FOR REJECTING REQUEST]
    Reject --> End
  
```

FIG. 857

```

graph TD
    S31([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> S31_1[RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST]
    S31_1 --> S32[SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S32 --> S33[CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI]
    S33 --> S34{COMMUNICATIONS TO BE CONTINUED?}
    S34 -- NO --> S42([DISCONNECTING COMMUNICATIONS])
    S34 -- YES --> S35[REQUEST FOR SWITCH]
    S35 --> S36[SWITCHING PATH THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S36 --> S37[RESPONSE FROM THIRD SUBSCRIBER]
    S37 --> S38[CONNECTING PATH TO THIRD SUBSCRIBER]
    S37 --> S43[RELEASING CONNECTION THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S38 --> S39([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])
    S39 --> S39_1[REQUEST TO TERMINATE COMMUNICATIONS WITH THIRD SUBSCRIBER]
    S39_1 --> S40[SWITCHING PATHS]
    S40 --> S41[RELEASING CONNECTION THROUGH MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    S41 --> S41_1([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])

```

FIG. 858

```

graph TD
    A([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> B[TRANSFER REQUEST S51]
    B --> C[DESTINATION INFORMATION S52]
    C --> D[SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK]
    D --> E[CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI]
    E --> F[CALLING THIRD SUBSCRIBER S55]
    F --> G[RESPONSE S56]
    G --> H([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])
  
```

FIG. 859

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

TRANSFER REQUEST

-S51

DESTINATION INFORMATION

-S 52

SELECTING VPI/VCI FOR CONNECTING MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK

S 53

CONNECTING TO MULTIPLE-SUBSCRIBER COMMUNICATIONS TRUNK THROUGH DETERMINED VPI/VCI

S 5 4

CALLING THIRD SUBSCRIBER

-S55

DISCONNECTION REQUEST
FROM TRANSFERRING
SUBSCRIBER

-S 6 1

SWITCHING PATHS

S 6 2

RELEASING CONNECTION

S 63

FIG. 860

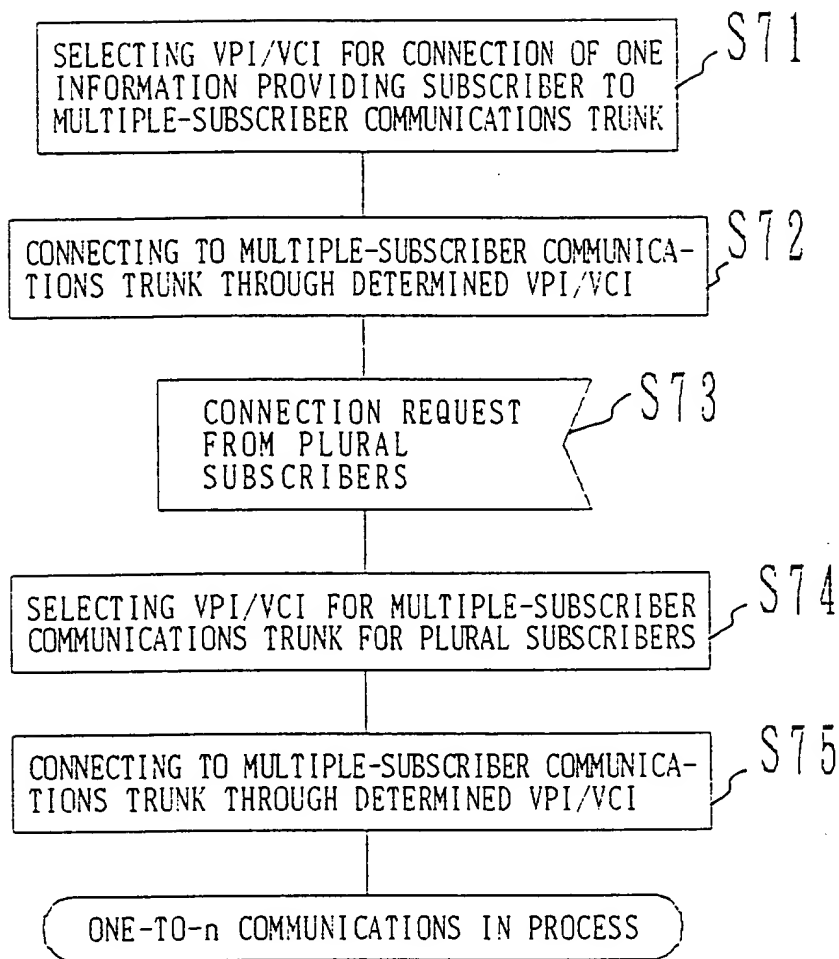


FIG. 861


```

graph TD
    Start([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> Step1[RECEIVING THREE-SUBSCRIBER COMMUNICATIONS REQUEST]
    Step1 --> Step2[SELECTING VPI/VCI FOR CONNECTING MULTIPLE TERMINATION UNIT]
    Step2 --> Step3[CONNECTING TO MULTIPLE TERMINATION UNIT THROUGH DETERMINED VPI/VCI]
    Step3 --> Decision{COMMUNICATIONS TO BE CONTINUED?}
    Decision -- YES --> Step4[REQUEST FOR SWITCH]
    Step4 --> Step5[SWITCHING PATHS BY MULTIPLE TERMINATION UNIT]
    Step5 --> Step6[RESPONSE FROM THIRD SUBSCRIBER]
    Step6 --> Step7[CONNECTING PATH TO THIRD SUBSCRIBER]
    Step7 --> Step8([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])
    Step6 --> Step9[RELEASING CONNECTION TO MULTIPLE TERMINATION UNIT]
    Step9 --> Step10[DISCONNECTING COMMUNICATIONS]
    Step10 --> Step11[NO]
    Step11 --> Step12[RELEASING CONNECTION TO MULTIPLE TERMINATION UNIT]
    Step12 --> Step13[REQUEST TO TERMINATE COMMUNICATIONS WITH THIRD SUBSCRIBER]
    Step13 --> Step14[SWITCHING PATHS]
    Step14 --> Step15[RELEASING CONNECTION TO MULTIPLE TERMINATION UNIT]
    Step15 --> Step16([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])

```

FIG. 862

```

graph TD
    A([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS]) --> B[TRANSFER REQUEST]
    B --> C[DESTINATION INFORMATION]
    C --> D[SELECTING VPI/VCI FOR CONNECTING  
MULTIPLE TERMINATION UNIT]
    D --> E[CONNECTING TO MULTIPLE TERMINATION  
UNIT THROUGH DETERMINED VPI/VCI]
    E --> F[CALLING THIRD SUBSCRIBER]
    F --> G[RESPONSE]
    G --> H([TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS])

```

FIG. 863

TWO-SUBSCRIBER COMMUNICATIONS IN PROCESS

TRANSFER REQUEST

DESTINATION INFORMATION

SELECTING VPI/VCI FOR CONNECTING MULTIPLE TERMINATION UNIT

CONNECTING TO MULTIPLE TERMINATION UNIT THROUGH DETERMINED VPI/VCI

CALLING THIRD SUBSCRIBER

DISCONNECTION REQUEST
FROM TRANSFERRING
SUBSCRIBER

SWITCHING PATHS

RELEASING CONNECTION

FIG. 864

SELECTING VPI/VCI FOR CONNECTION OF
ONE INFORMATION PROVIDING SUBSCRIBER
TO MULTIPLE TERMINATION UNIT

CONNECTING TO MULTIPLE TERMINATION
UNIT THROUGH DETERMINED VPI/VCI

CONNECTION REQUEST
FROM PLURAL
SUBSCRIBERS

SELECTING VPI/VCI FOR MULTIPLE-
TERMINATION UNIT FOR PLURAL SUBSCRIBERS

CONNECTING TO MULTIPLE TERMINATION
UNIT THROUGH DETERMINED VPI/VCI

ONE-TO-n COMMUNICATIONS IN PROCESS

FIG. 865

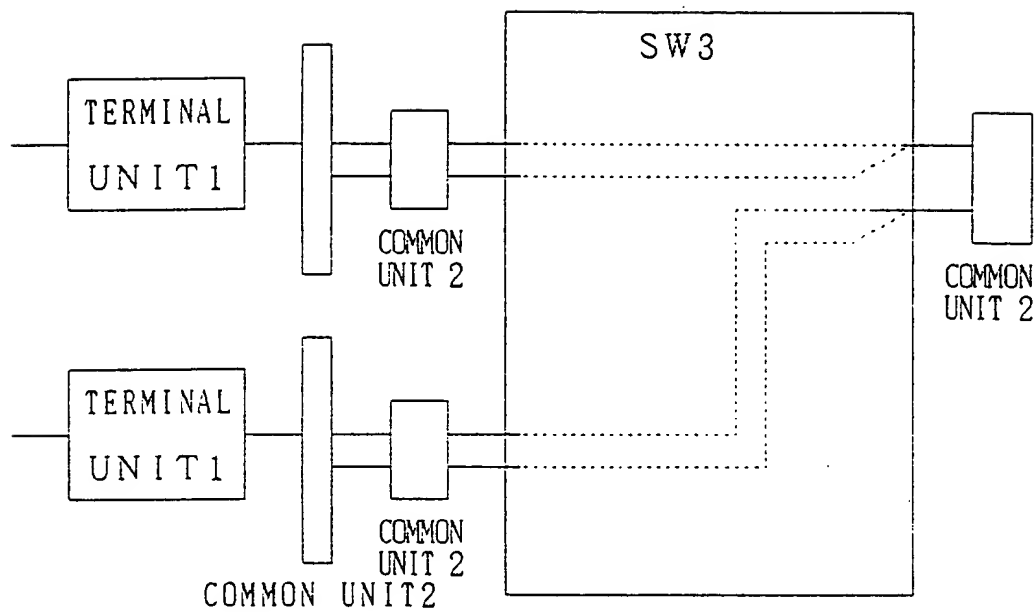


FIG. 866

669660-12260

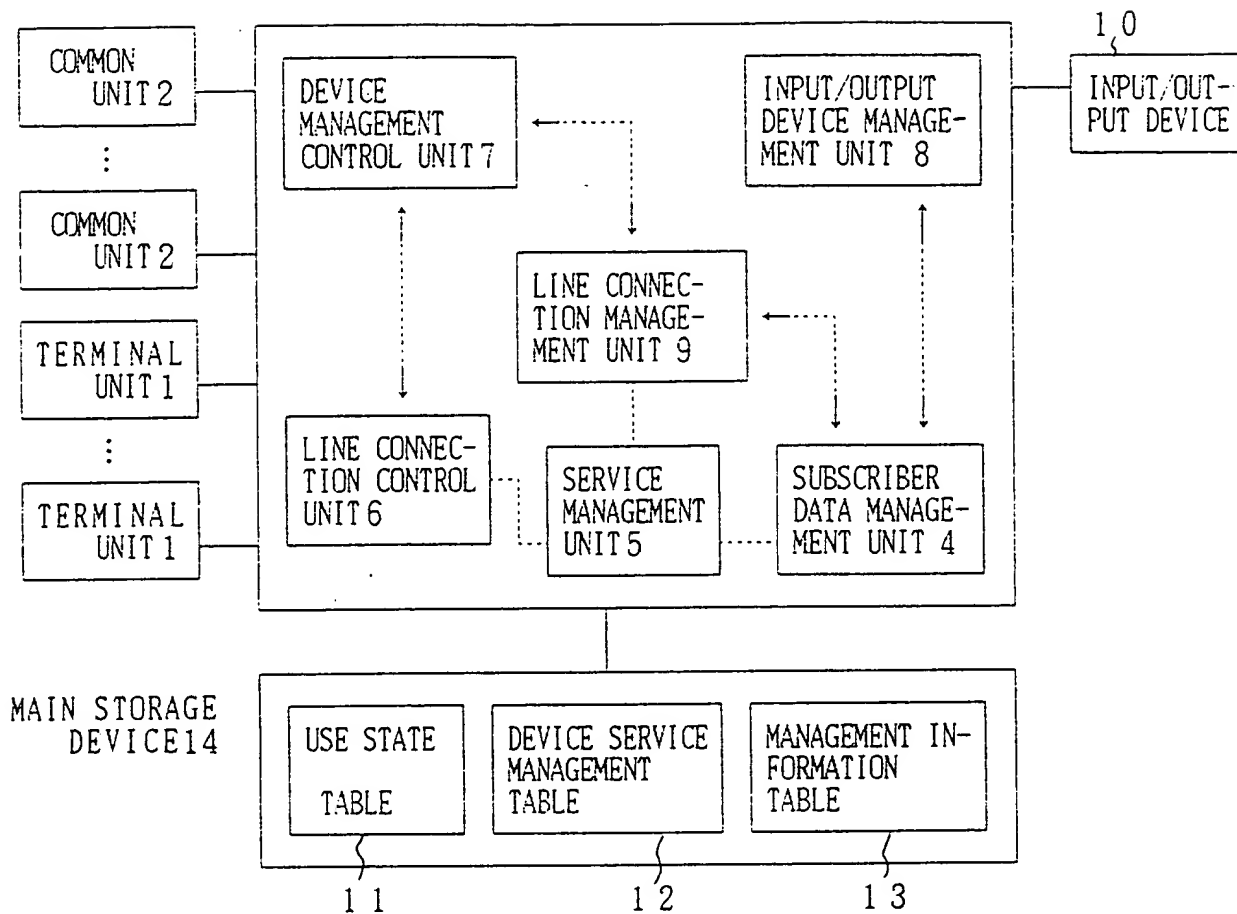


FIG. 867

00927241-03690

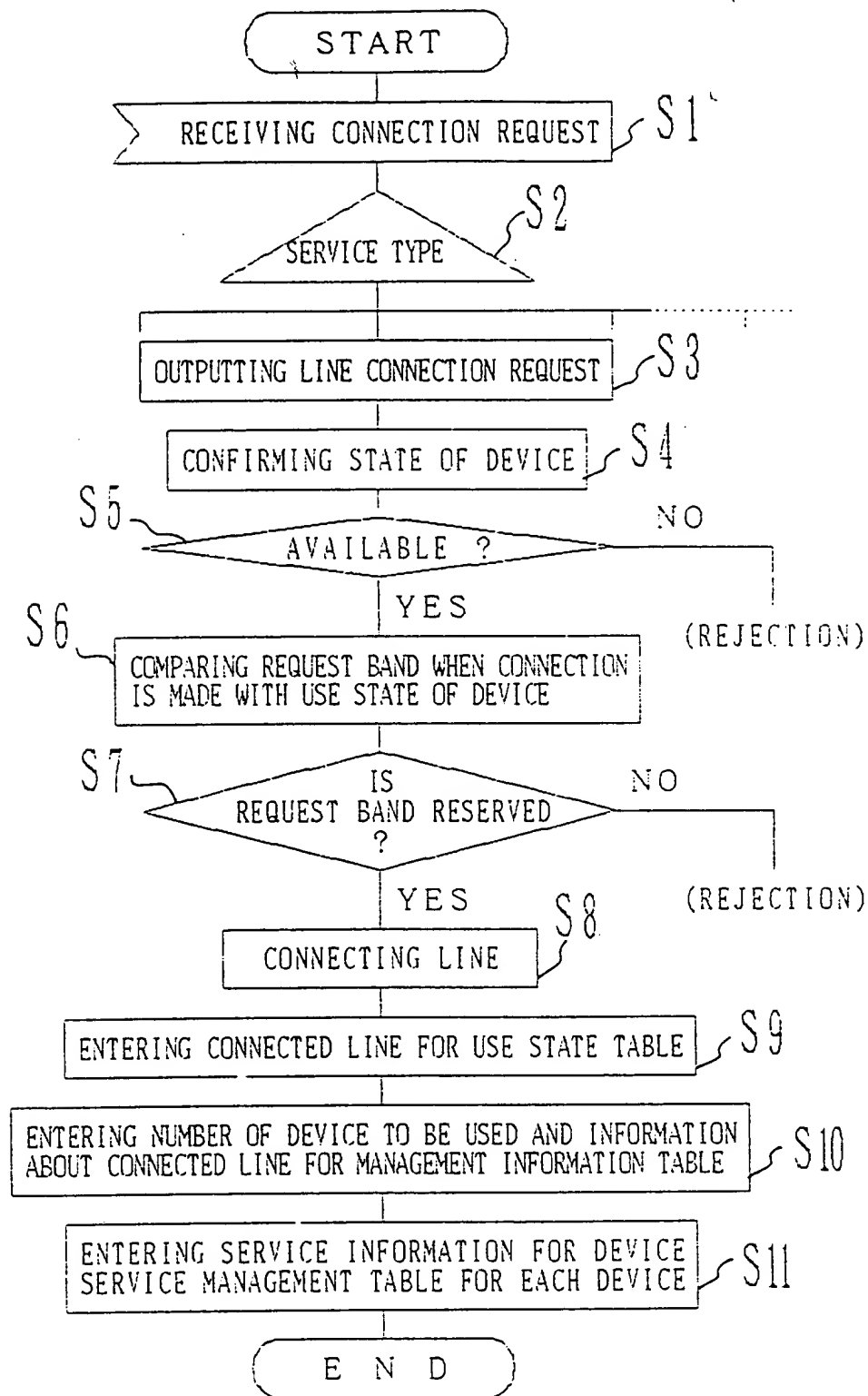


FIG. 868

START

DETECTING DEVICE FAULT

S 12

CONFIRMING DEVICE SERVICE MANAGEMENT TABLE

-S 13



SERVICE TYPE

-S 14

RETRIEVING LINE

S 15

EDITING AND OUTPUTTING CONNECTION
INFORMATION OF LINE

S 16

E N D

FIG. 869

[illegible]

0927243 032600

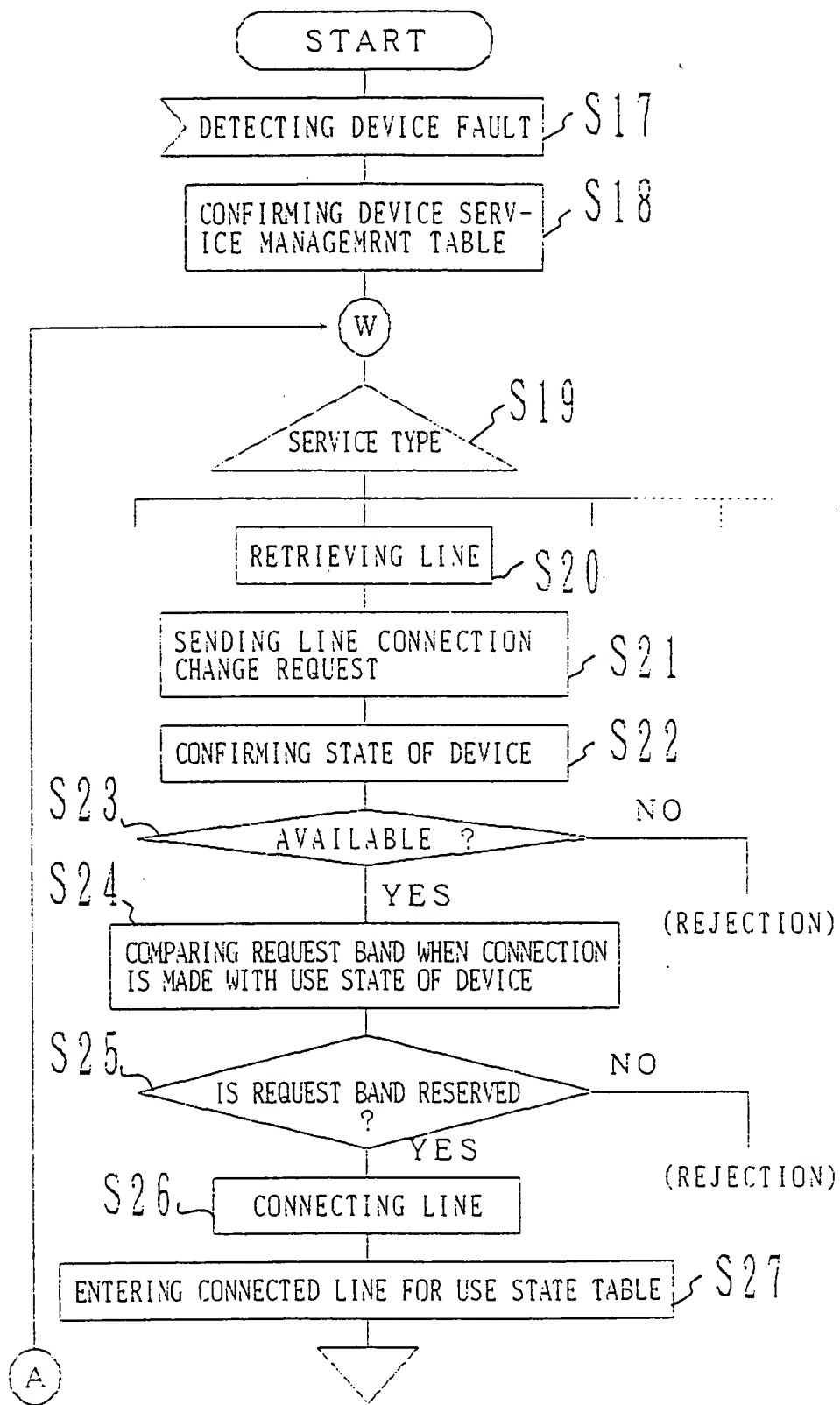


FIG. 870

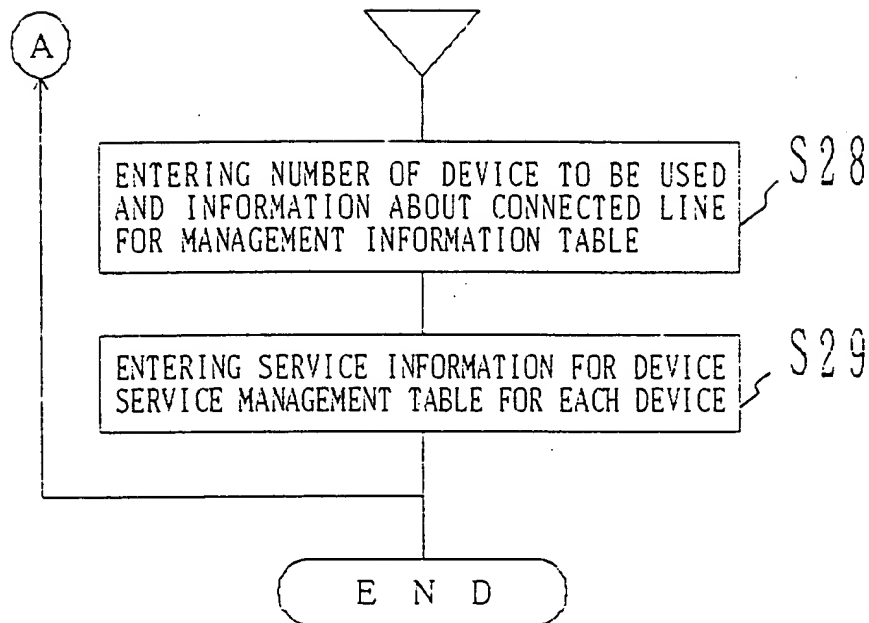
[illegible]

FIG. 871

Figure 1a is a block diagram illustrating a storage system architecture. The system is divided into four main sections: SHELF-B1, SHELF-A1, SW (Switch), and LLP-A. Two input lines, A and B, enter from the left. Line A passes through a block labeled T1, and line B passes through a block labeled T2. These lines then enter SHELF-B1 and SHELF-A1, which are represented by vertical rectangles. The outputs of SHELF-B1 and SHELF-A1 connect to the SW block. The SW block has two outputs that connect to LLP-A and LLP-B, represented by vertical rectangles. A dashed line indicates a connection between the outputs of SHELF-B1 and SHELF-A1 and the inputs of LLP-A and LLP-B. The entire system is labeled 1 a.

MANAGEMENT INFORMATION TABLE 13			USE STATE TABLE 11		
VPI/VCI OF A	LLP-A DEVICE SERVICE MANAGEMENT TABLE 12		A	AVAILABLE	3GM USED
POINT OF T1			B	AVAILABLE	UNUSED
POINT OF SHELF-B1	LLP-B DEVICE SERVICE MANAGEMENT TABLE 12		C	UNAVAILABLE	——
POINT OF SHELF-A1					.
POINT OF LLP-A					.
VPI/VCI OF B	SHELF-A1 DEVICE SERVICE MANAGEMENT TABLE 12				.
POINT OF T2					.
POINT OF SHELF-B2					.
POINT OF SHELF-A1					.
POINT OF LLP-B					.
PRIORITY/NON-PRIORITY					.

LINE TERMINATOR	ATM SWITCH VCC CONTROL DEVICE	REMOTE CONCENTRATOR VCC CONTROL DEVICE	LINE TERMINATOR
	<div style="border: 1px solid black; padding: 5px; text-align: center;"> LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEED ING LAYERS </div>		
CELL INFORMATION	CELL INFORMATION		S 1
	<div style="border: 1px solid black; padding: 5px; text-align: center;"> AIS F R E F PERFORMANCE MONITOR SIGNAL PERFORMANCE MONITOR RESULT </div>	※INVERSE PROCEDURE WHEN LINE FAULT OCCURS ON LAYER 2 AND SUCCEEDING LAYERS FROM REMOTE CONCENTRATOR	S 2
PERFORMING WHEN LINES ARE FAULTY IN LAYER 2 AND SUCCEEDING LAYERS			
DETECTING LINE FAULT FOR EACH LAYER		DETECTING LINE FAULT FOR EACH LAYER	S 3
	<div style="border: 1px solid black; padding: 5px;"> BAND REASSIGNMENT CONTROL/SAVE CONTROL FOR EACH CELL PRIORITY LEVEL </div>		
STOPPING FAULT MONITOR BAND REASSIGNMENT START NOTIFICATION		STOPPING FAULT MONITOR BAND REASSIGNMENT START NOTIFICATION	S 4
BAND REASSIGNMENT START RESPONSE		BAND REASSIGNMENT START RESPONSE	S 5
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL STARTING CELL-BUFFERING		CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL STARTING CELL-BUFFERING	S 6
FAULT/IDLE BAND CHECK		FAULT/IDLE BAND CHECK	S 7
PROCESSING FAULTY BAND IN ORDER FROM HIGHEST PRIORITY LEVEL	CANCELING FAULTY VPI/VCI REASSIGNING IDLE BAND VPI/VCI SWEEPING CELL BUFFERING INFORMATION DELETING CELL BUFFERING	CANCELING FAULTY VPI/VCI REASSIGNING IDLE BAND VPI/VCI SWEEPING CELL BUFFERING INFORMATION DELETING CELL BUFFERING	S 8
		PROCESSING FAULT BAND IN ORDER FROM HIGHEST PRIORITY LEVEL	S 9
			S 10
			S 11
RESUMING FAULT MONITOR		RESUMING FAULT MONITOR	S 12
BAND REASSIGNMENT TERMINATION NOTIFICATION		BAND REASSIGNMENT TERMINATION NOTIFICATION	S 13
BAND REASSIGNMENT TERMINATION RESPONSE		BAND REASSIGNMENT TERMINATION RESPONSE	

FIG. 874

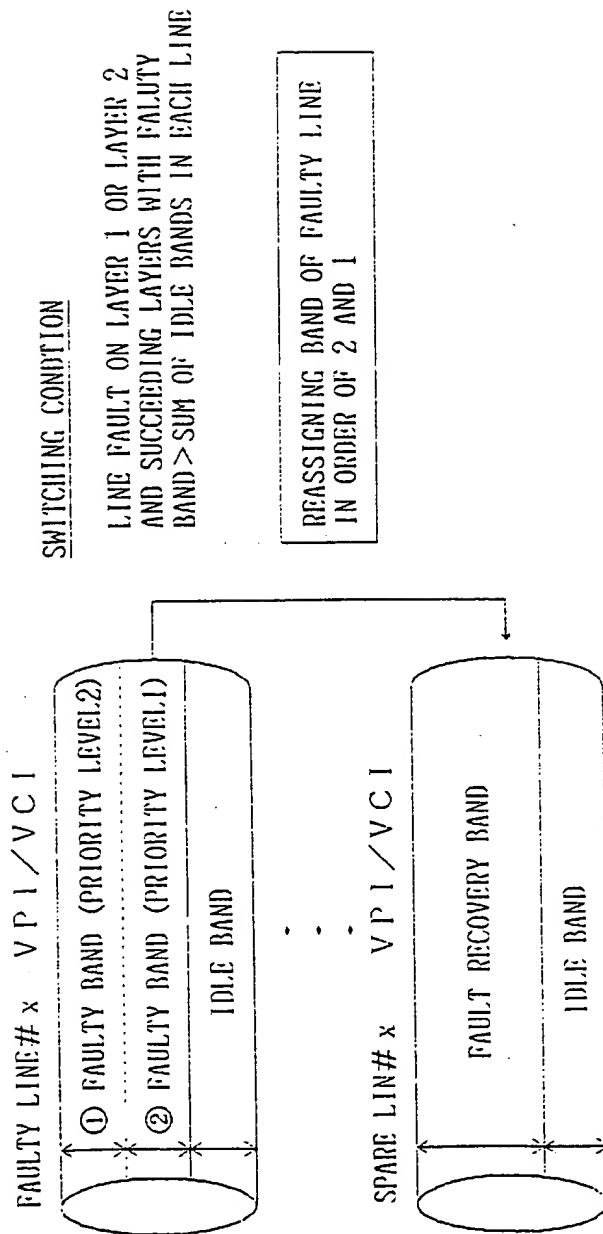


FIG. 875

LINE TERMINATOR	ATM SWITCH VCC CONTROL DEVICE	REMOTE CONCENTRATOR VCC CONTROL DEVICE	LINE TERMINATOR
	<div style="border: 1px solid black; padding: 5px; text-align: center;"> LINE FAULT ON LAYER 1 OR LAYER 2 AND SUCCEEDING LAYERS </div>		
CELL INFORMATION	CELL INFORMATION		S 1
	AIS		
PERFORMING WHEN LINES ARE FAULTY IN LAYER 2 AND SUCCEEDING LAYERS	FREF	※INVERSE PROCEDURE WHEN LINE FAULT OCCURS ON LAYER 2 AND SUCCEEDING LAYERS FROM REMOTE CONCENTRATOR	S 2
	PERFORMANCE MONITOR SIGNAL		
	PERFORMANCE MONITOR RESULT		
DETECTING LINE FAULT FOR EACH LAYER		DETECTING LINE FAULT FOR EACH LAYER	S 3
BAND REASSIGNMENT CONTROL/SAVE CONTROL FOR EACH CELL PRIORITY LEVEL			
BAND REASSIGNMENT START NOTIFICATION	STOPPING FAULT MONITOR	STOPPING FAULT MONITOR	S 4
BAND REASSIGNMENT START RESPONSE		BAND REASSIGNMENT START NOTIFICATION	S 5
CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL		CELL INFORMATION BUFFERING BASED ON PRIORITY LEVEL	
STARTING CELL-BUFFERING		STARTING CELL-BUFFERING	S 6
	FAULT/IDLE BAND CHECK	FAULT/IDLE BAND CHECK	S 7
PROCESSING FAULTY BAND IN ORDER FROM HIGHEST PRIORITY LEVEL	CANCELING FAULTY VPI/VCI	CANCELING FAULTY VPI/VCI	S 8
	REASSIGNING SPARE LINE VPI/VCI	REASSIGNING SPARE LINE VPI/VCI	S 9
	SWEEPING CELL BUFFERING INFORMATION	SWEEPING CELL BUFFERING INFORMATION	S 10
	DELETING CELL BUFFERING	DELETING CELL BUFFERING	S 11
RESUMING FAULT MONITOR		RESUMING FAULT MONITOR	S 12
SPARE LINE REASSIGNMENT TERMINATION NOTIFICATION		SPARE LINE REASSIGNMENT TERMINATION NOTIFICATION	
SPARE LINE REASSIGNMENT TERMINATION RESPONSE		SPARE LINE REASSIGNMENT TERMINATION RESPONSE	S 13

FIG. 876

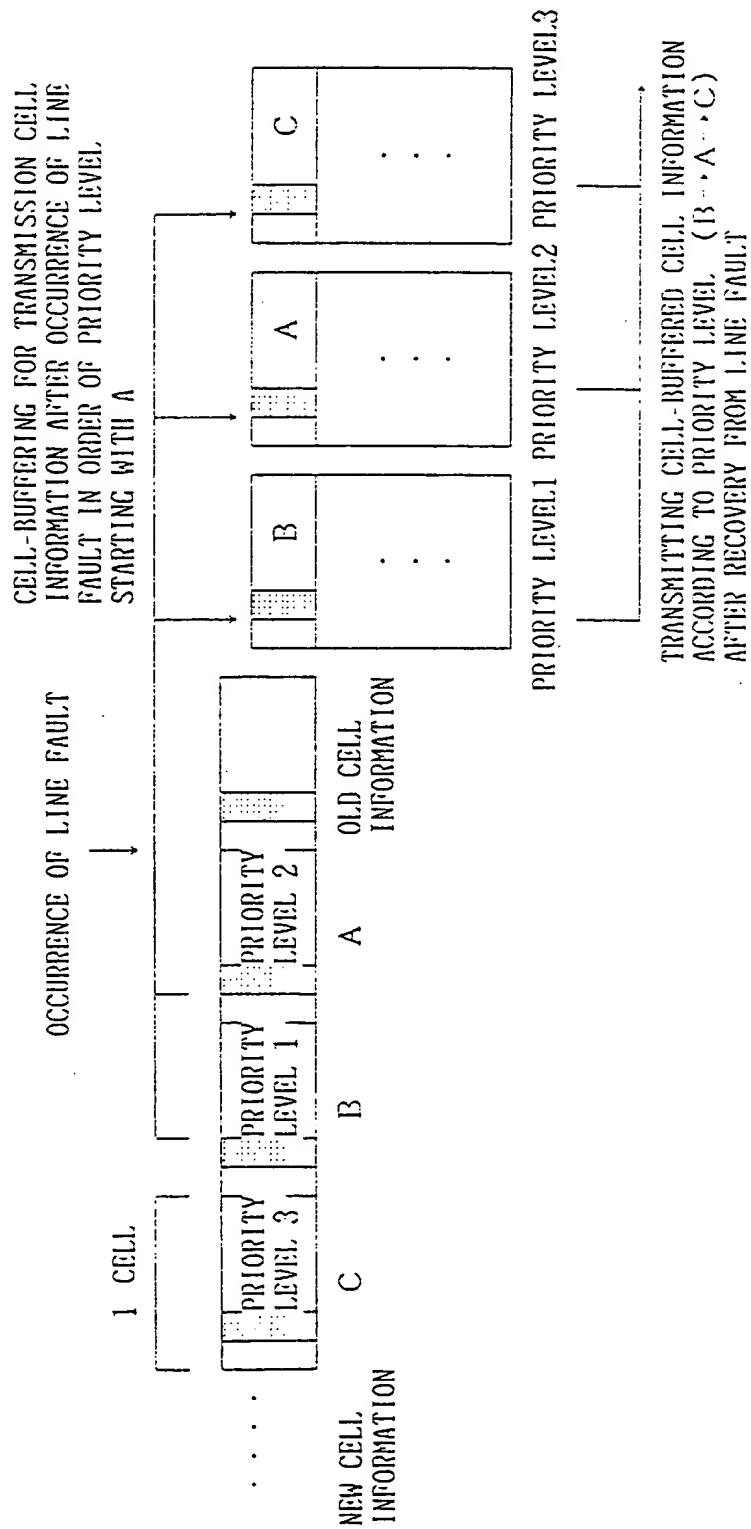


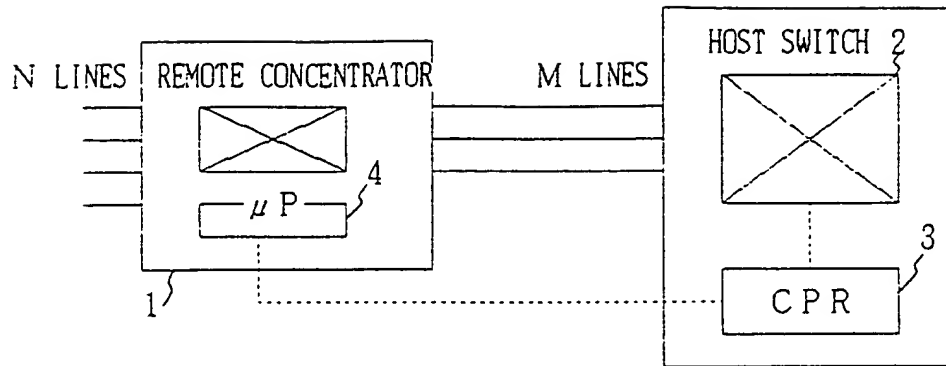
FIG. 877

- (I) CELL TYPE LEVEL OAM CELL, INTRA-STATION LAP CELL, COMMON CELL, TEST CELL, ETC.
 (II) SERVICE LEVEL F R, SMDS, C R, C E, ETC.
 (III) AVAILABLE BAND LEVEL... DEFINING PRIORITY OR NON-PRIORITY DEPENDING ON SIZE
 OF AVAILABLE BAND.
 (IV) LINE TYPE LEVEL O C 3; O C 1 2, ETC.

CELL TYPE	CELL SIGNAL NAME	PRIORITY LEVEL
OAM CELL	A I S (WARNING DISPLAY SIGNAL) F E R F (REMOTE TERMINAL RECEPTION FAULT) PERFORMANCE MONITOR SIGNAL e t c	1
INTRA-STATION LAP CELL	TRAFFIC INFORMATION BILLING INFORMATION PERFORMANCE INFORMATION e t c	2
COMMON CELL	PRIORITY BIT ON INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING SMALL AMOUNT OF INFORMA- TION OR SMALL NUMBER OF CELLS)	3
	PRIORITY BIT ON INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING LARGE AMOUNT OF INFORMA- TION OR LARGE NUMBER OF CELLS)	4
	PRIORITY BIT OFF INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING SMALL AMOUNT OF INFORMA- TION OR SMALL NUMBER OF CELLS)	5
	PRIORITY BIT OFF INFORMATION IN CELL FOR EACH SERVICE (WITH 1 PIECE OF INFORMATION FOR CELL CONTAINING LARGE AMOUNT OF INFORMA- TION OR LARGE NUMBER OF CELLS)	6
TEST CELL	CELL LOOPBACK TEST INFORMATION LOOPBACK TEST INFORMATION e t c	7

F I G. 8 7 8

669220-672220



WHERE $N > M$

FIG. 879

00920" 6722200

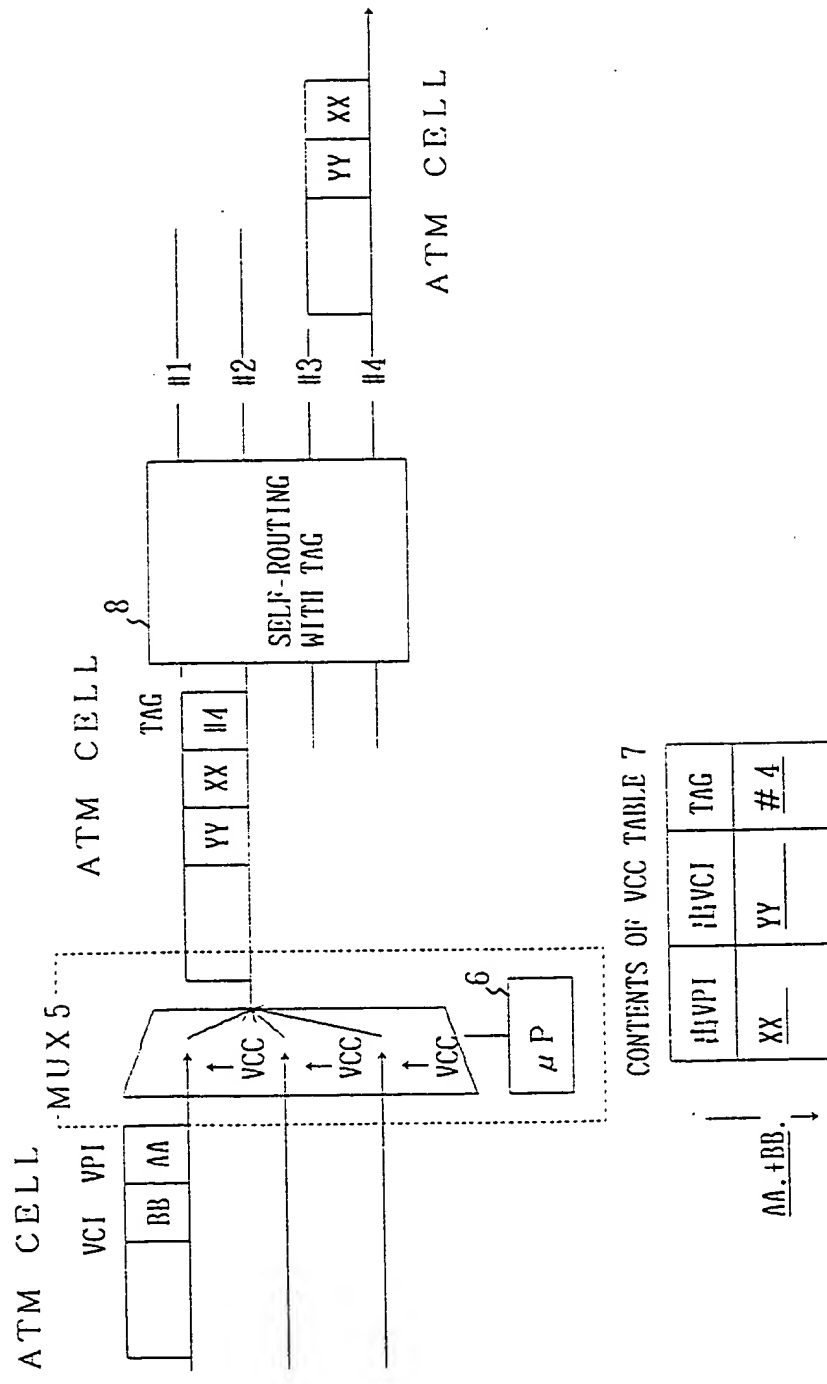


FIG. 880

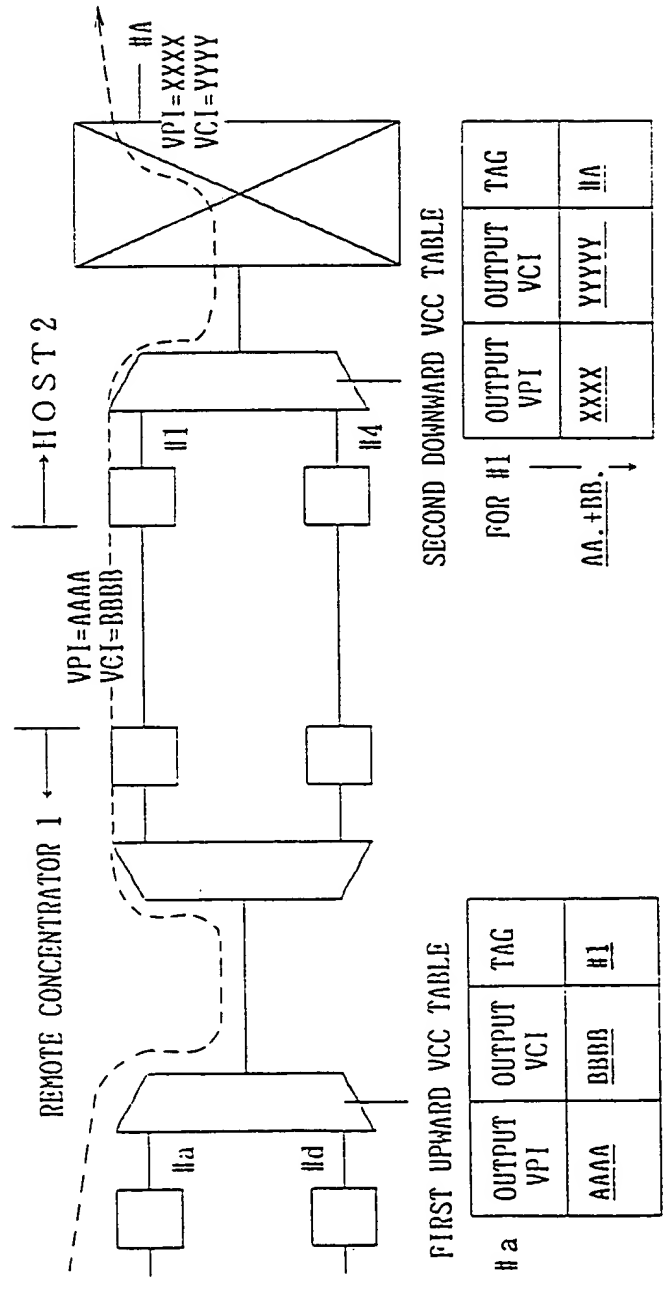


FIG. 881

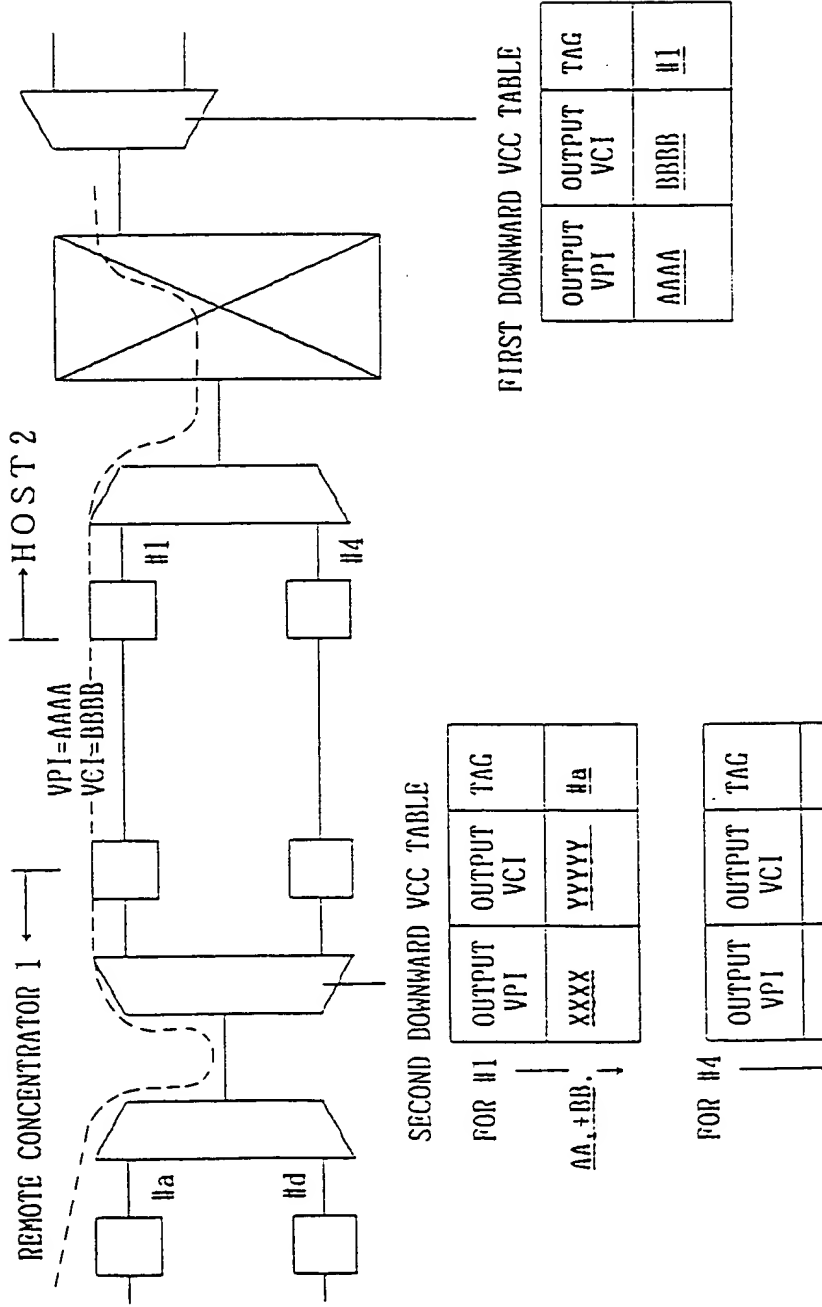


FIG. 882

CONNECTING PATH

S1

HAS PATH
CONNECTION REQUEST BEEN
ISSUED ?

NO

YES

S2

BANDS OF NORMAL ROUTE AND SPARE ROUTE AND VPI/VCI ARE
RESERVED WHEN PATH IS SET BETWEEN CONCENTRATOR AND HOST.

S3

VCC IS SET FOR NORMAL ROUTE ON FIRST UPWARD VCC TABLE AND
FIRST DOWNWARD VCC TABLE. NORMAL VCC DATA AND REASSIGNMENT
VCC DATA ARE SET ON SECOND UPWARD VCC TABLE AND SECOND
DOWNWARD VCC TABLE.

FIG. 883

NORMAL VCC DATA

REASSIGNMENT VCC DATA

OUTPUT VCC	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG
A A A A	B B B B	# 1	C C C C	D D D D D	# 4

FIG. 884

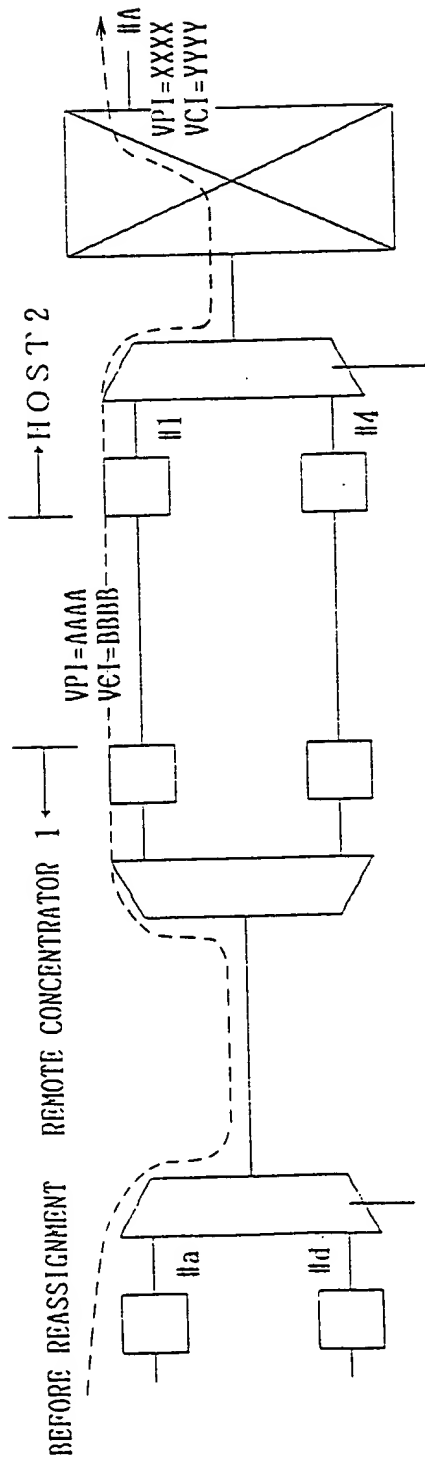
PATH REASSIGNING PROCESS

S4
SPECIFYING FAULTY TRANSMISSION LINE AND EXTRACTING PATH
WHICH USES FAULTY ROUTE.

S5
SETTING REASSIGNMENT VCC DATA ON EACH OF FIRST UPWARD
VCC TABLE AND FIRST DOWNWARD VCC TABLE.

END

FIG. 885



FIRST UPWARD VCC TABLE

REASSIGNMENT VCC DATA

NORMAL VCC DATA				REASSIGNMENT VCC DATA			
	OUTPUT VPI	OUTPUT VCI	TAG	OUTPUT VPI	OUTPUT VCI	TAG	
0	AAAA	BBBB	#1	CCCC	DDDD	#4	

↑
0 : NORMAL VCC TABLE 1 : REASSIGNMENT VCC TABLE

SECOND UPWARD VCC TABLE

FOR #1		FOR #4		
AA.+BB.	CC.+DD.	OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYY	XXXX	YYYY	#4

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYYY	#4

FIG. 886

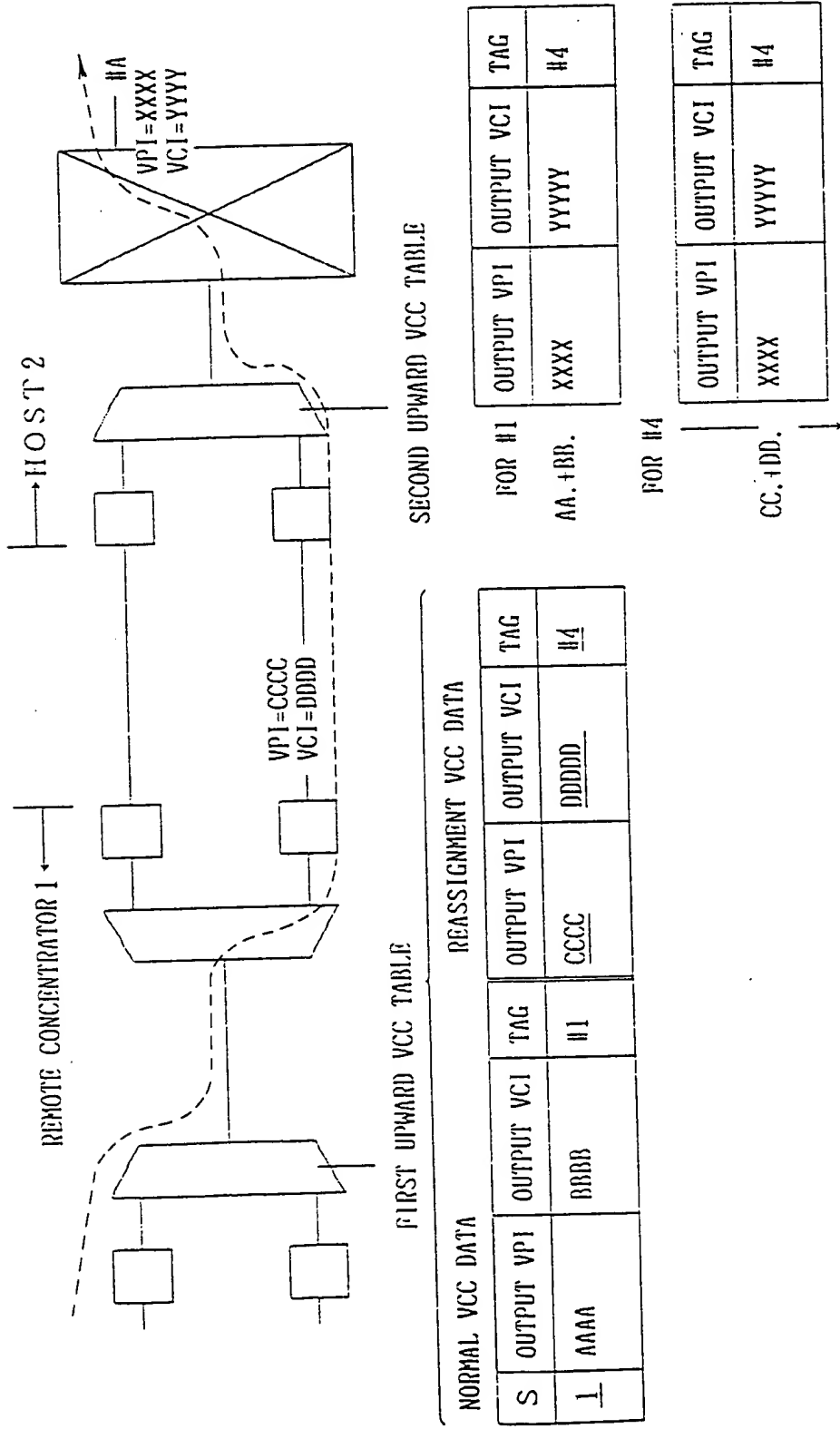


FIG. 887

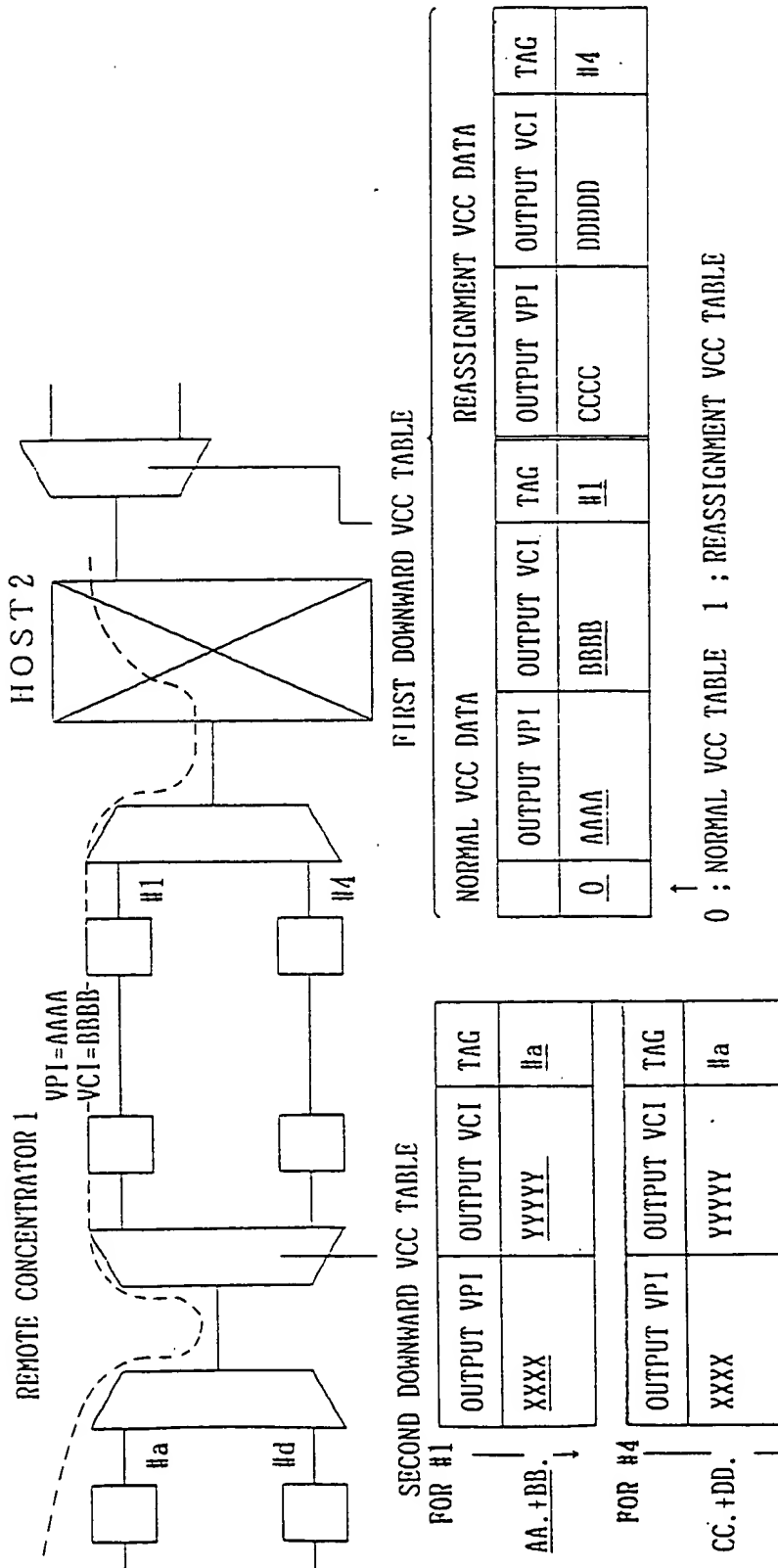


FIG. 888

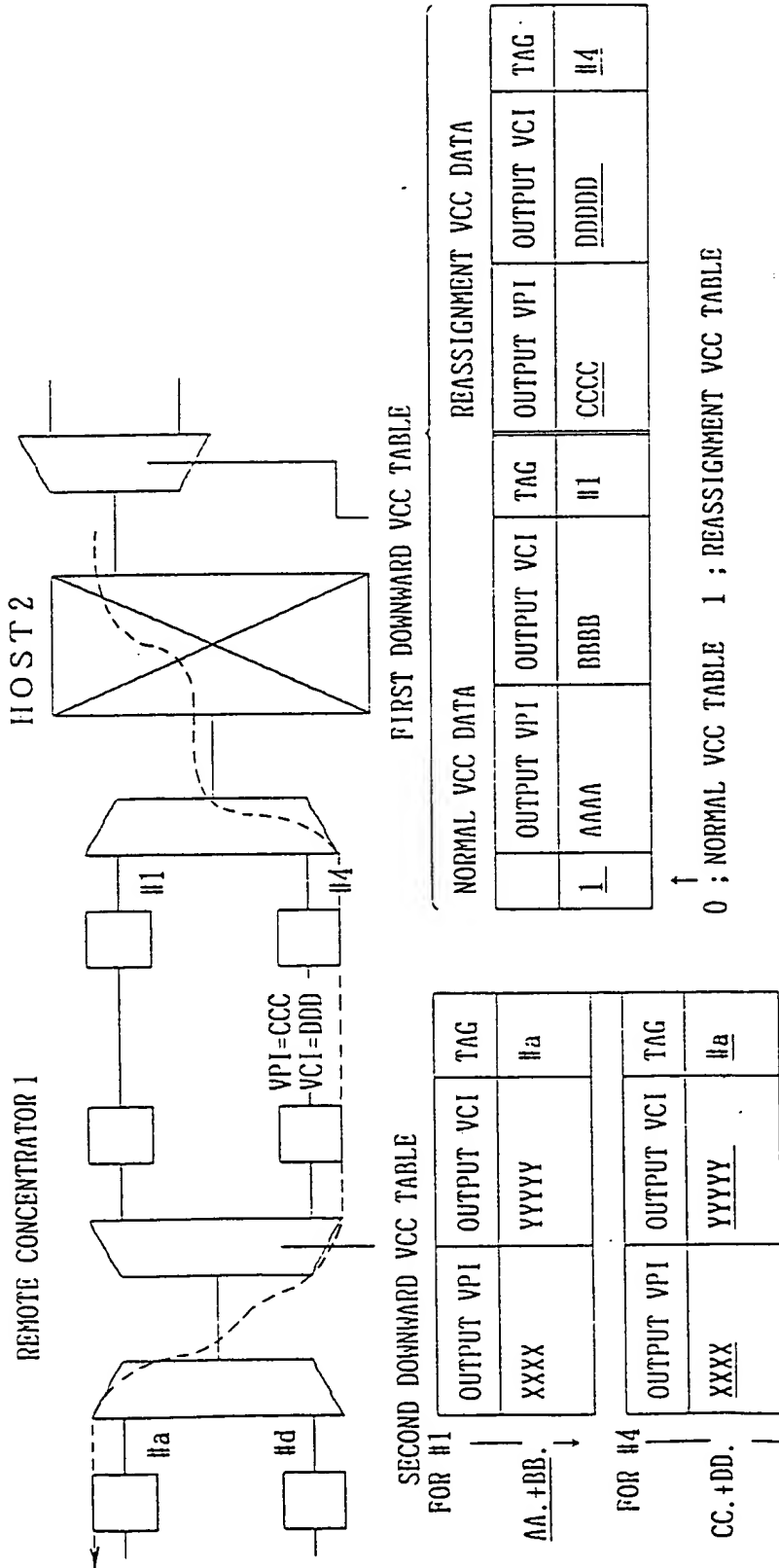
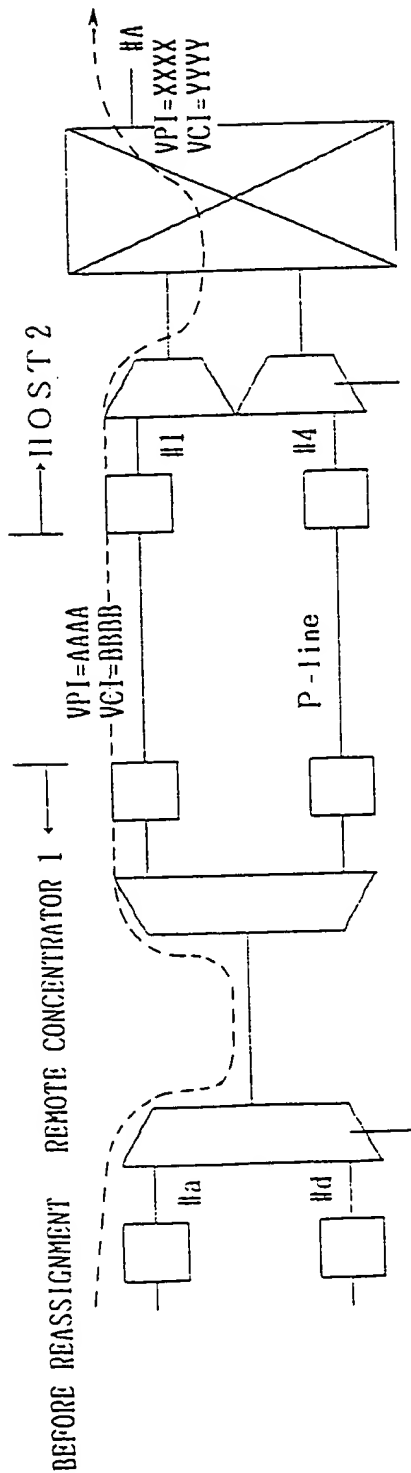


FIG. 889



FIRST UPWARD VCC TABLE

OUTPUT VPI	OUTPUT VCI	TAG
AAAA	BBBB	II1

#a

SECOND UPWARD VCC TABLE

OUTPUT VPI	OUTPUT VCI	TAG
XXXX	YYYY	II4

FOR II1

AA + BB

FOR II4

OUTPUT VPI	OUTPUT VCI	TAG
BLANK	BLANK	

FIG. 890

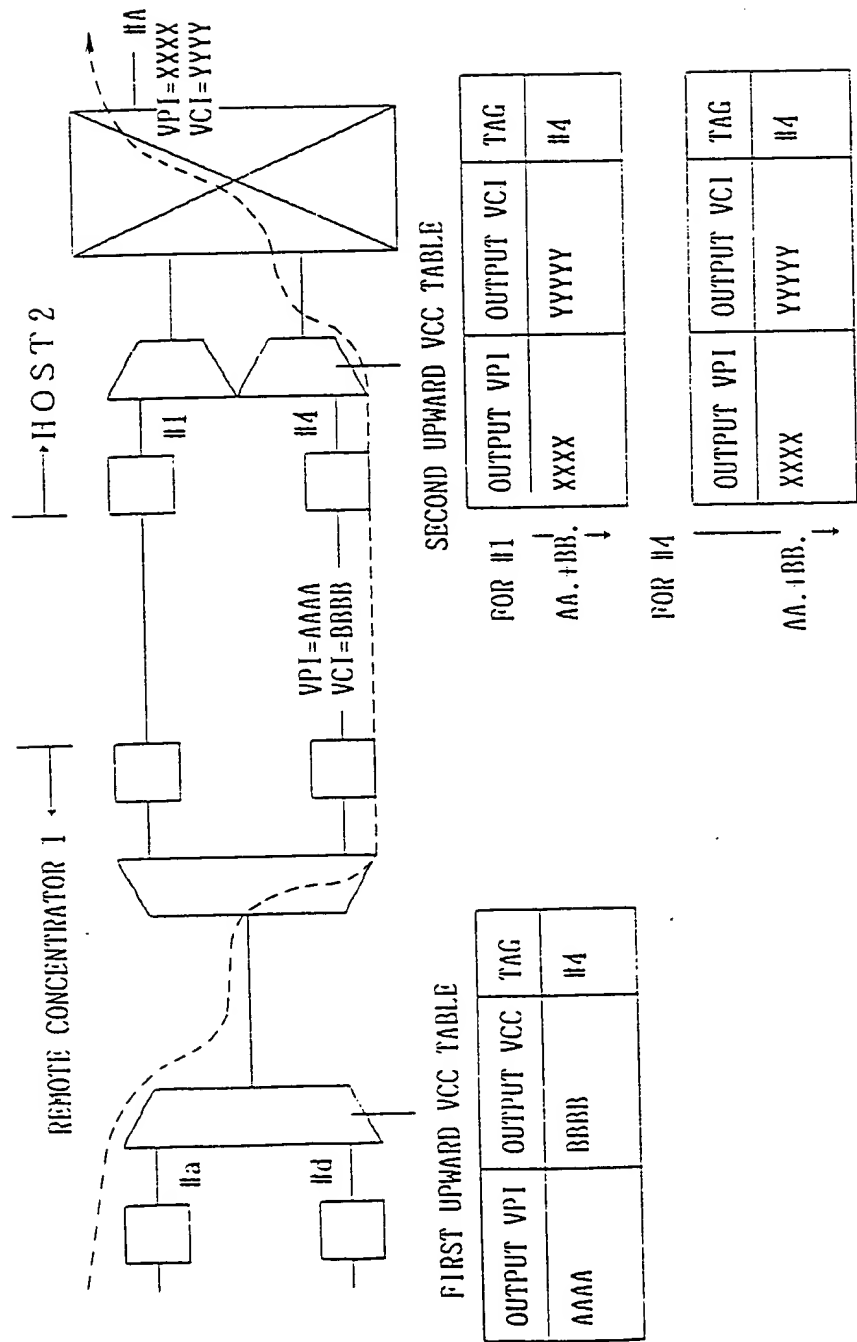
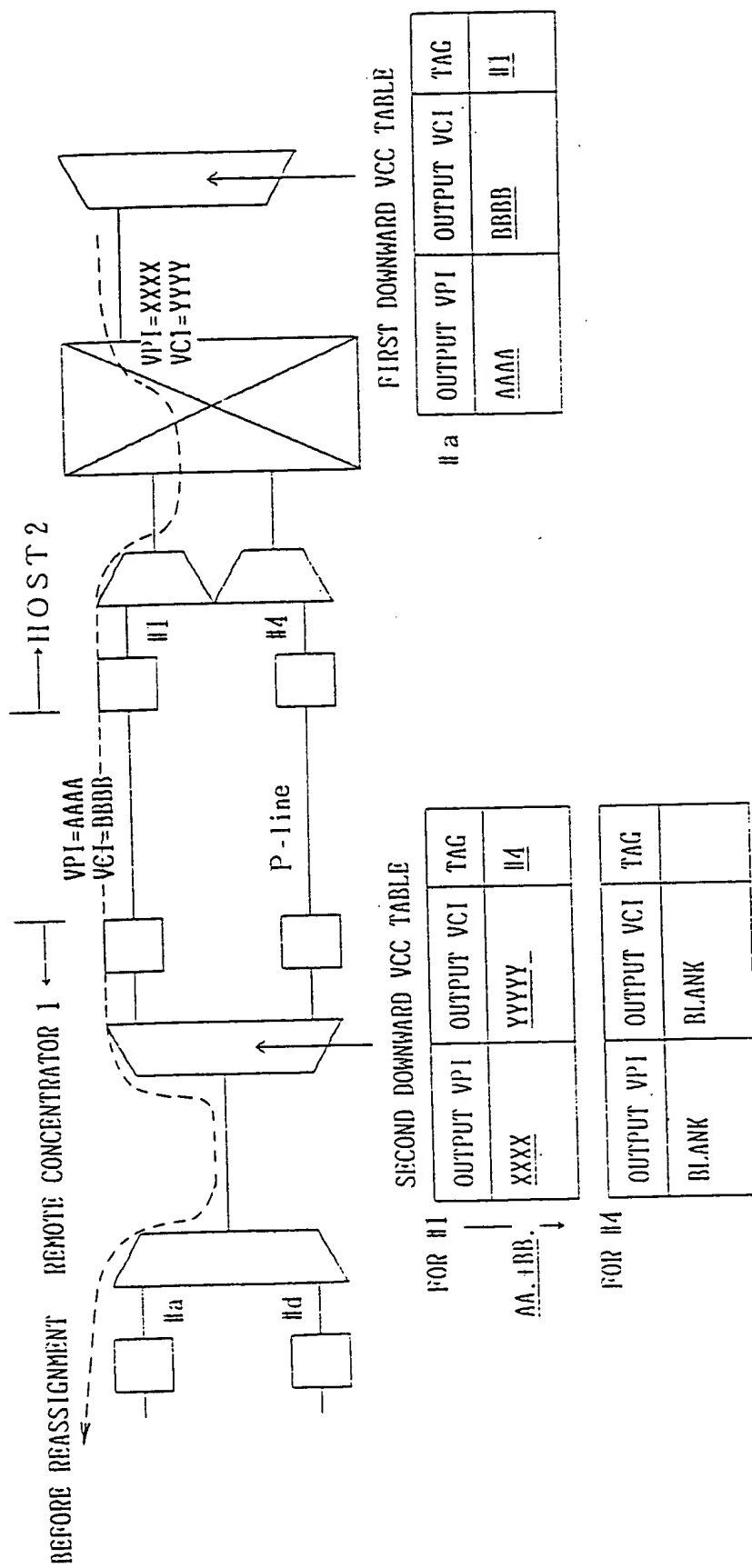


FIG. 891



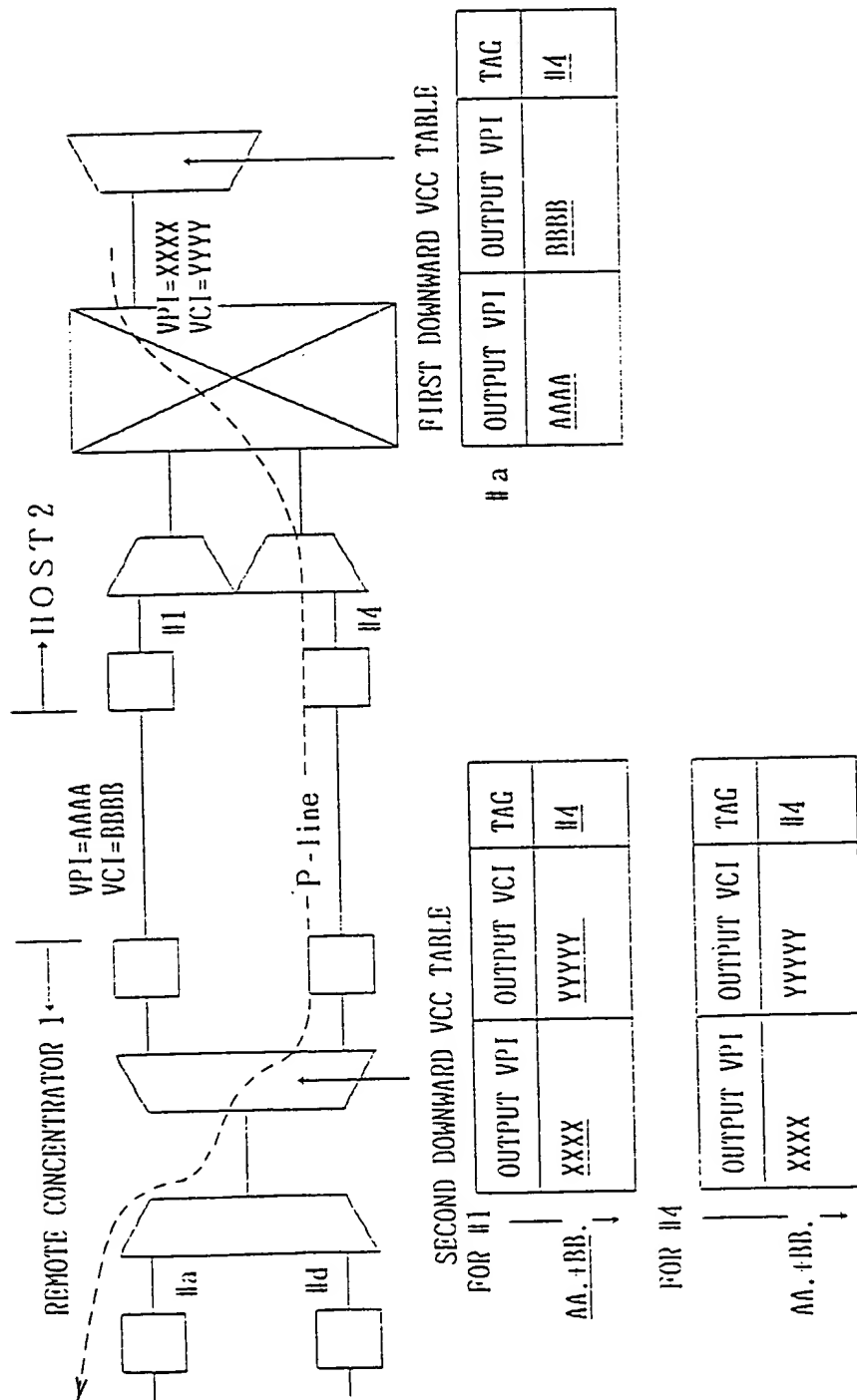


FIG. 893

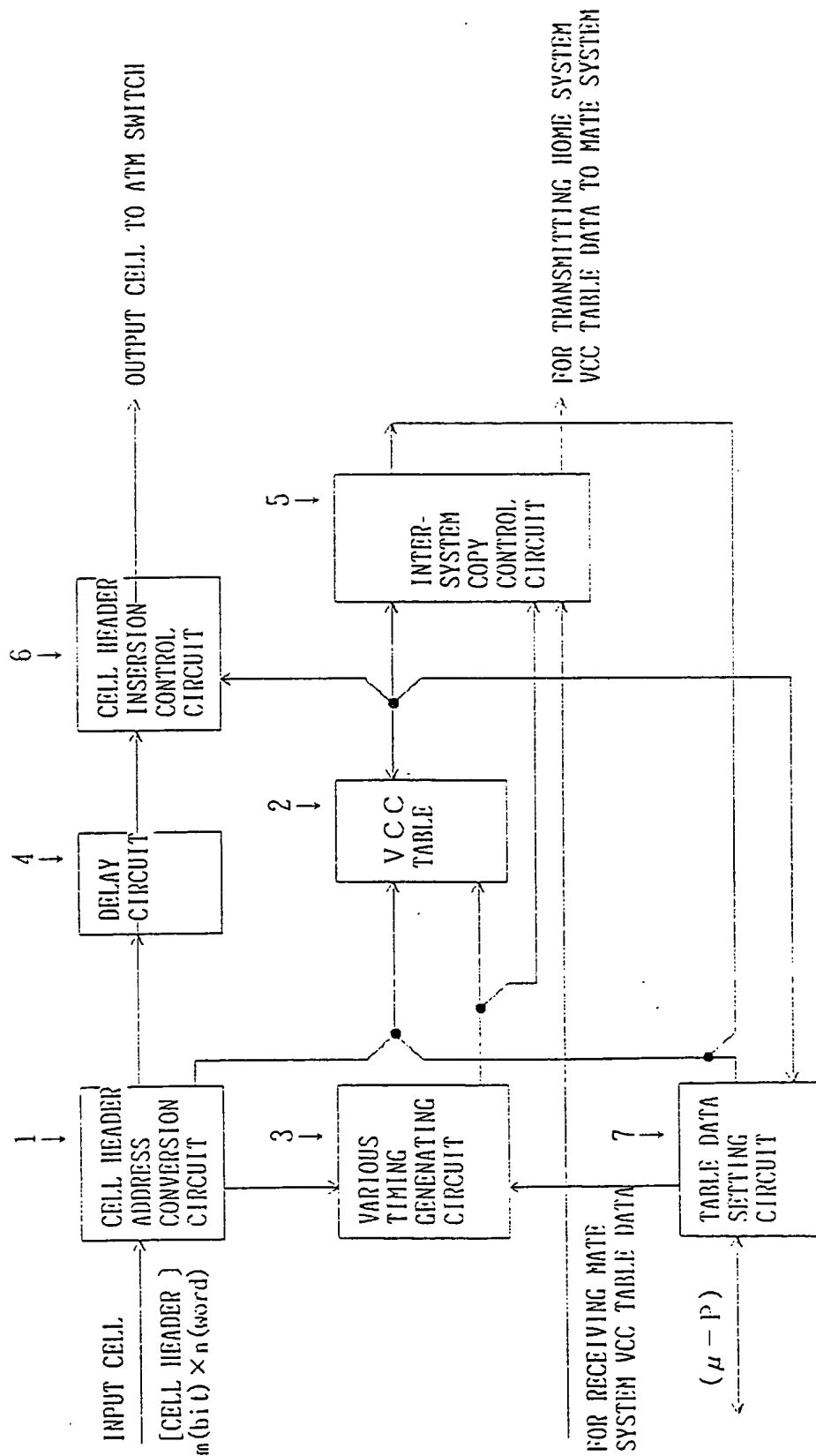


FIG. 894

[VCC TABLE ACCESS TIMING USING INPUT CELL]

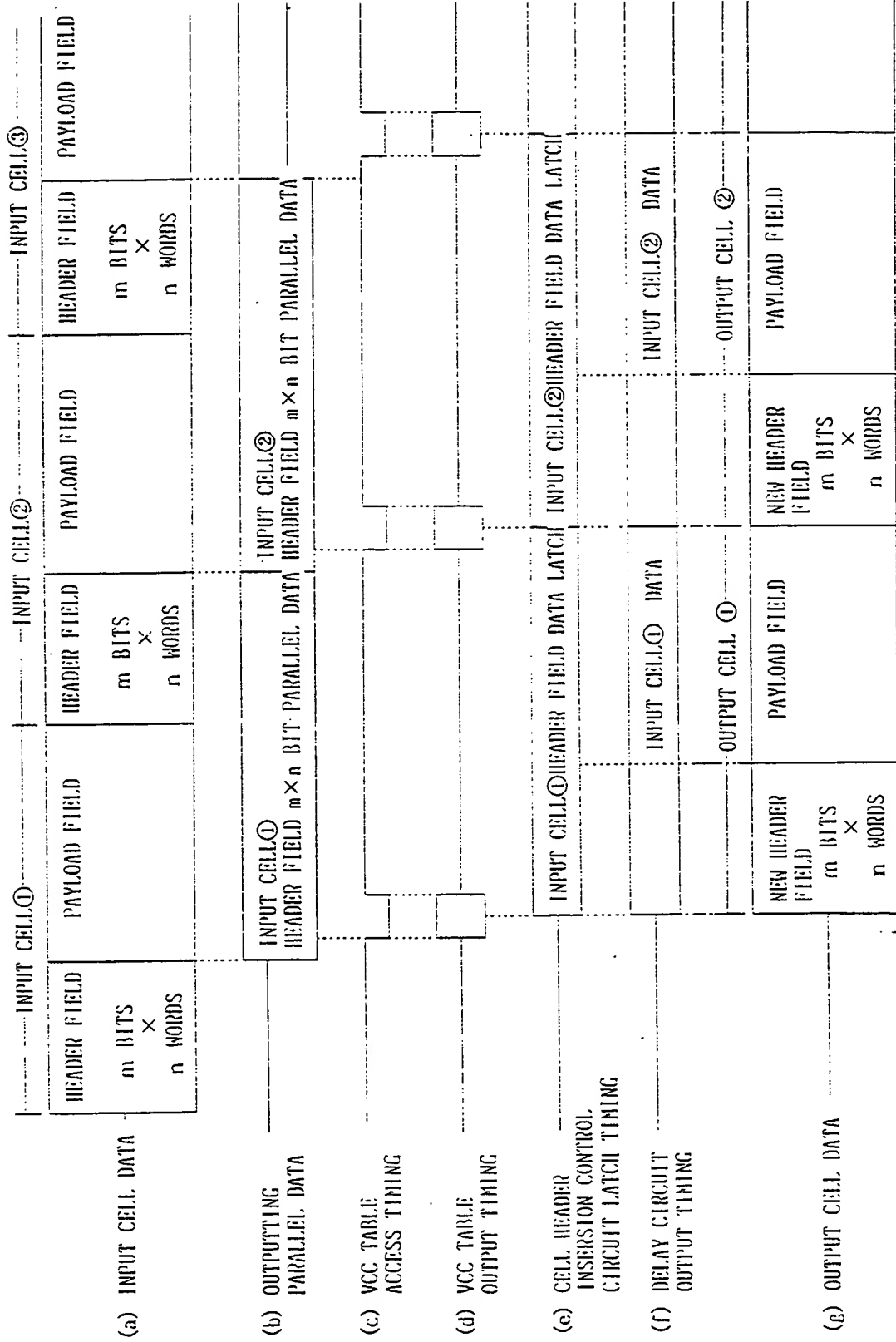


FIG. 895

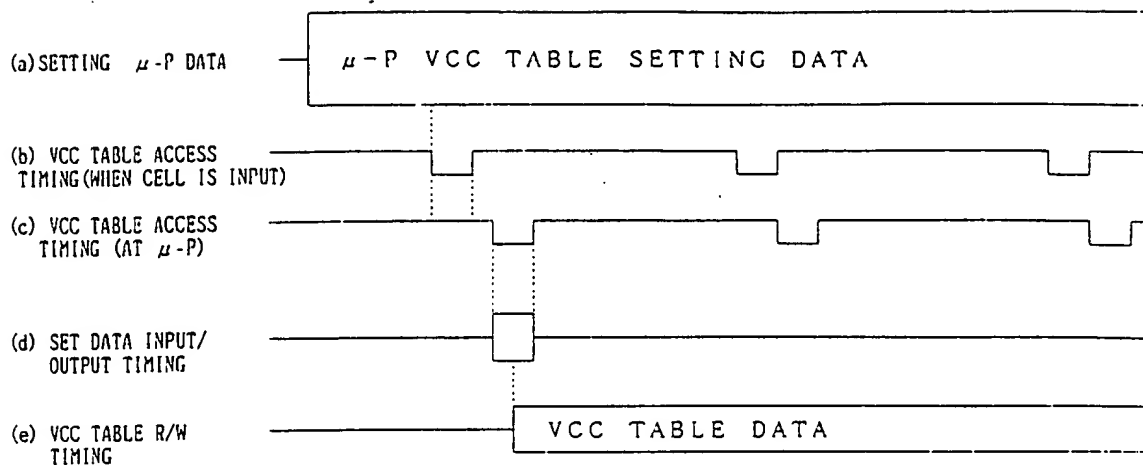


FIG. 896A

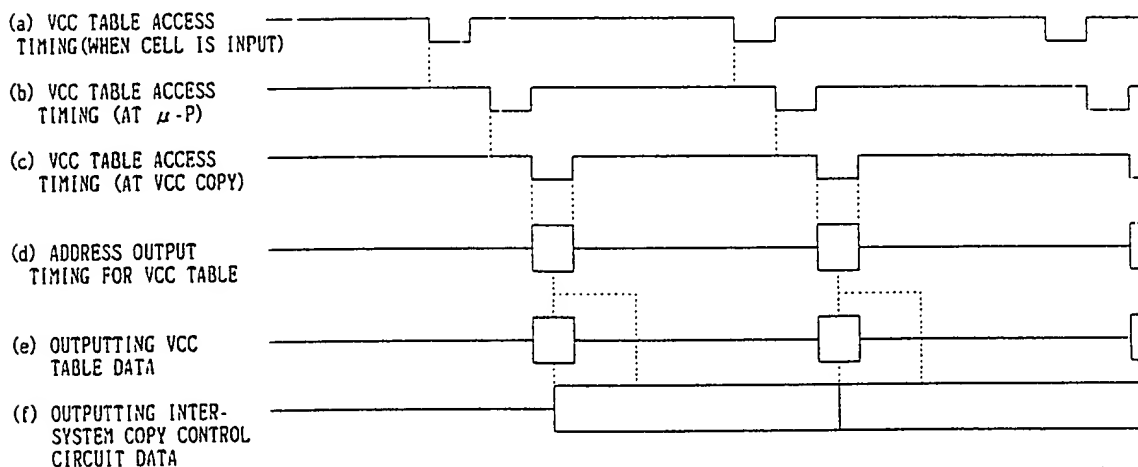


FIG. 896B

669260 612260

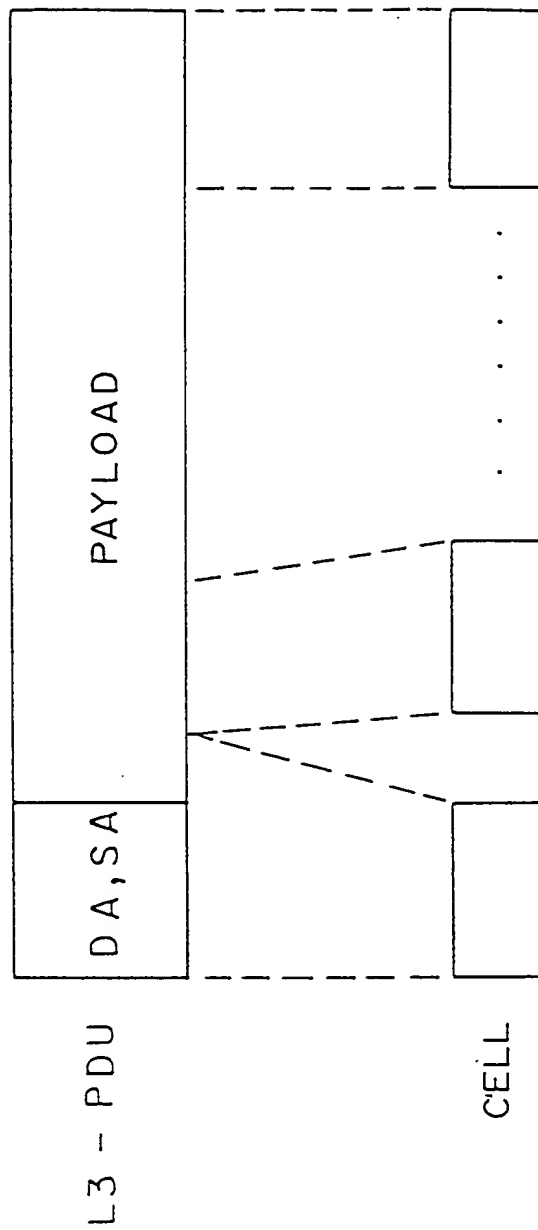


FIG. 897

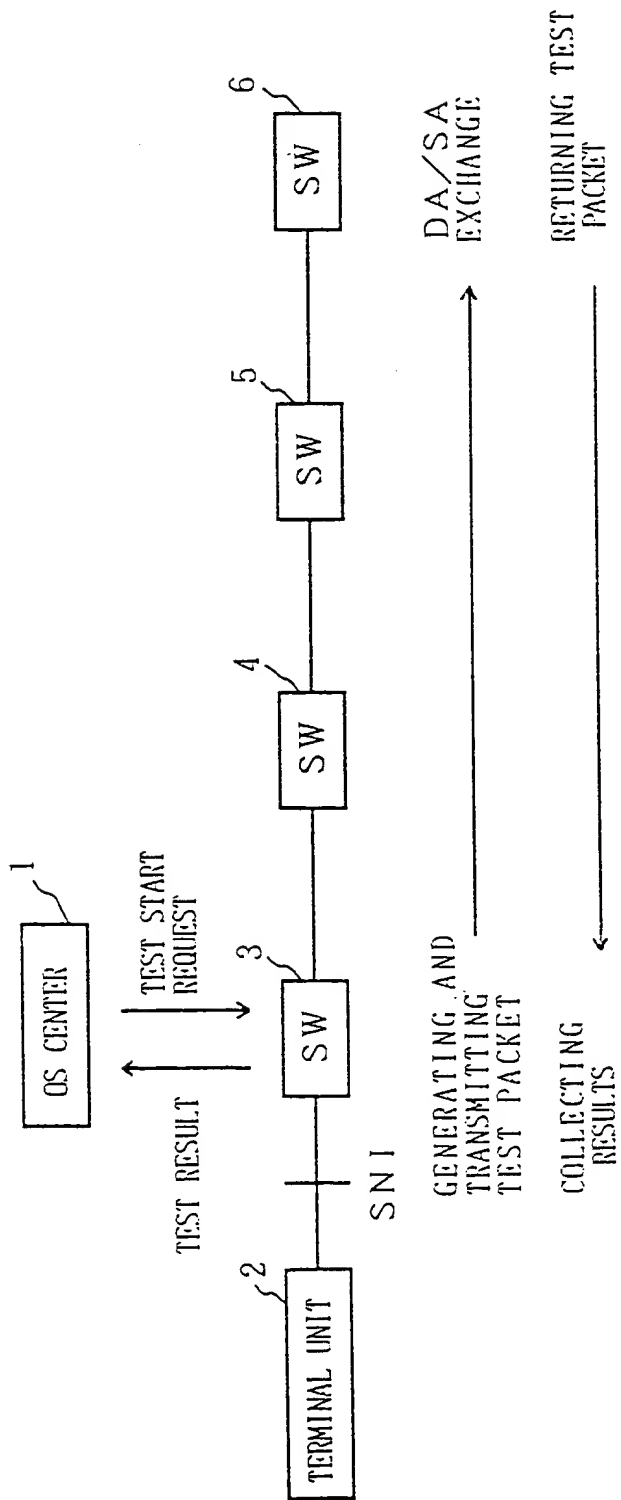


FIG. 898

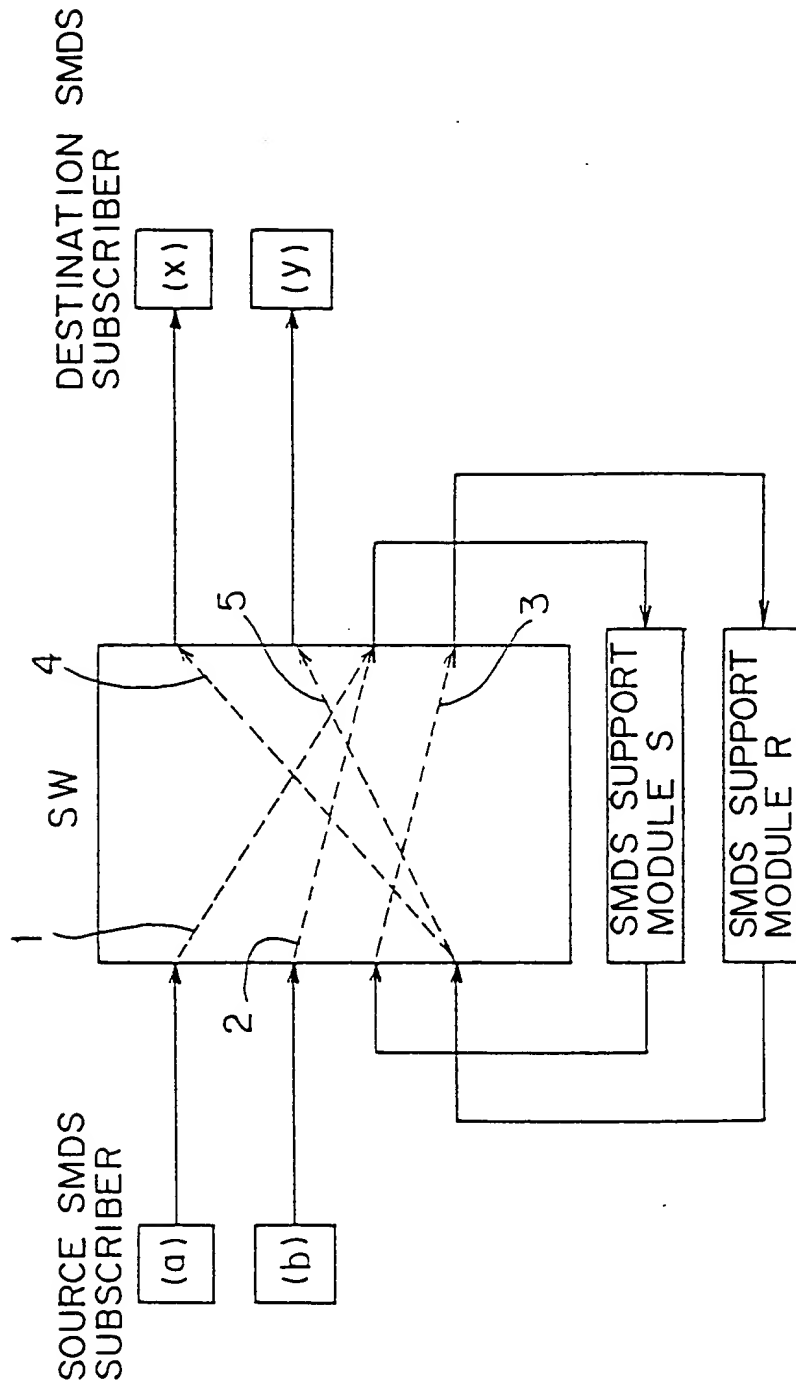


FIG. 899

66320-ET2200

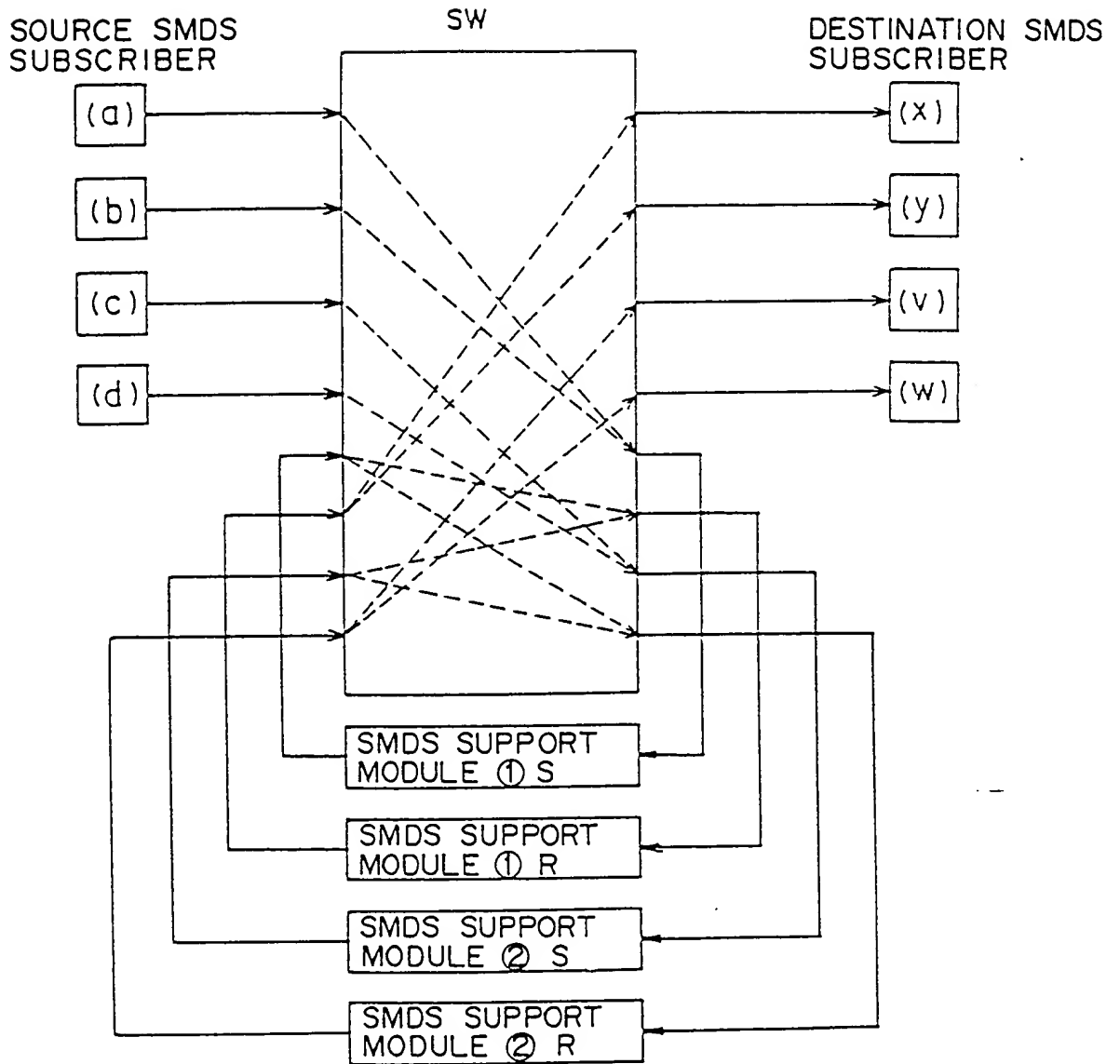


FIG. 900

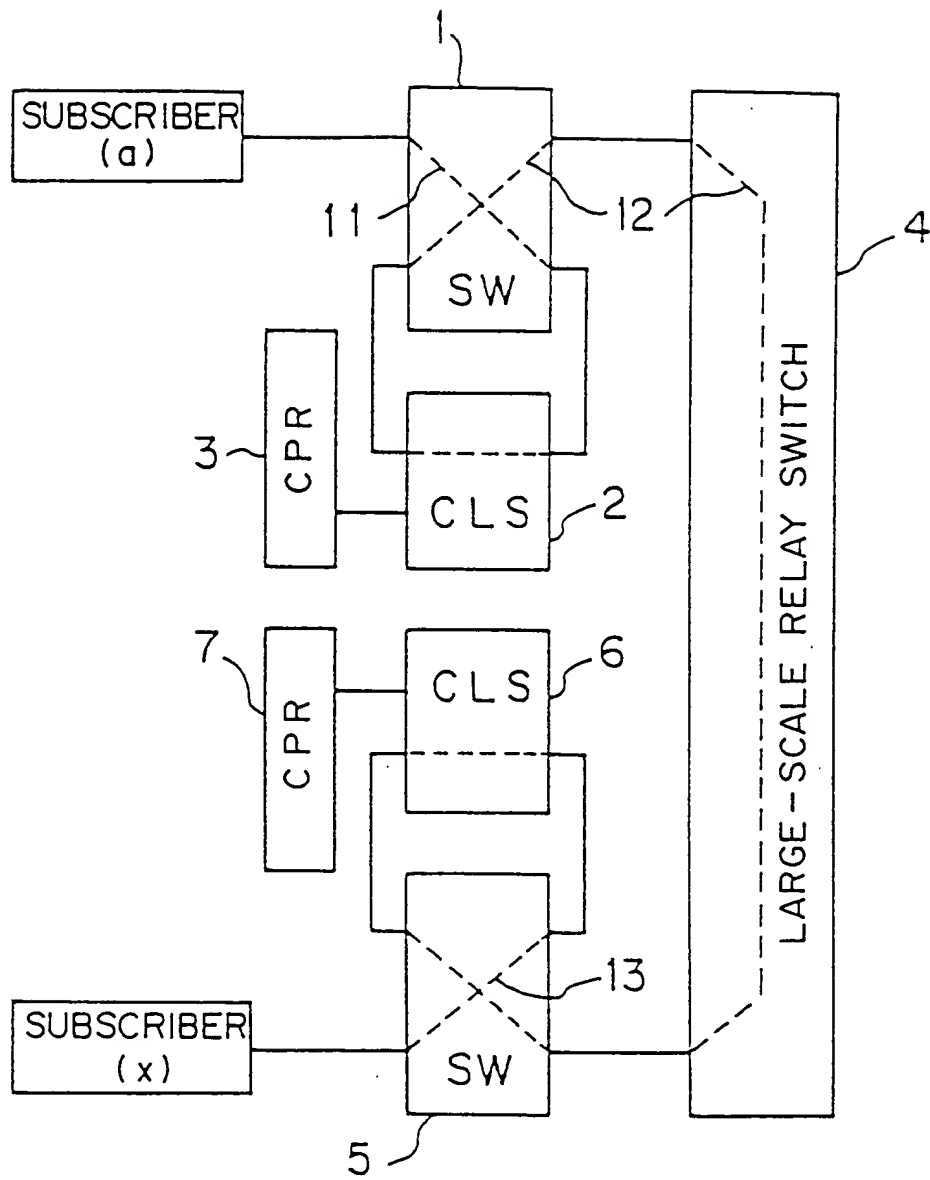


FIG. 901

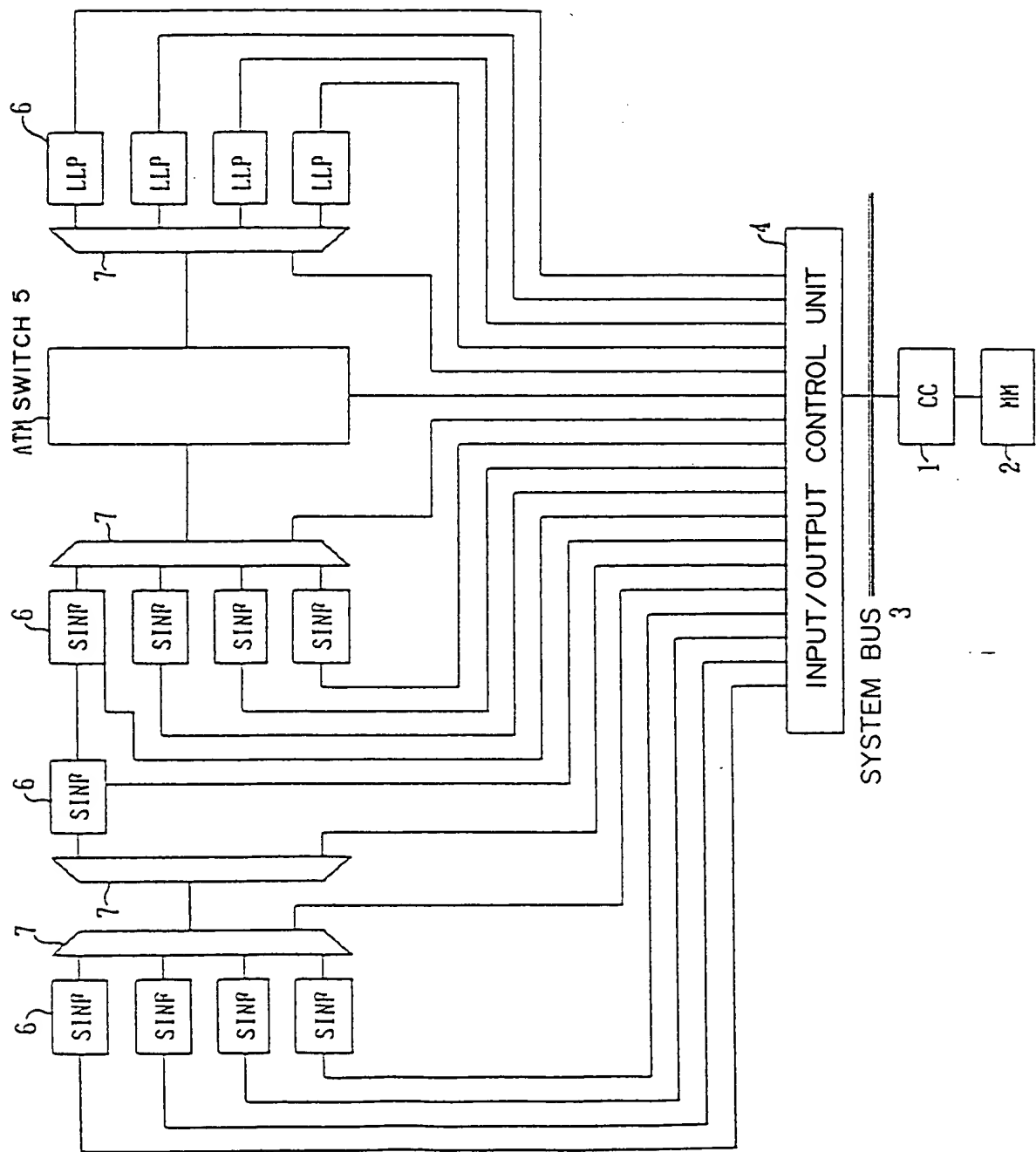


FIG. 902

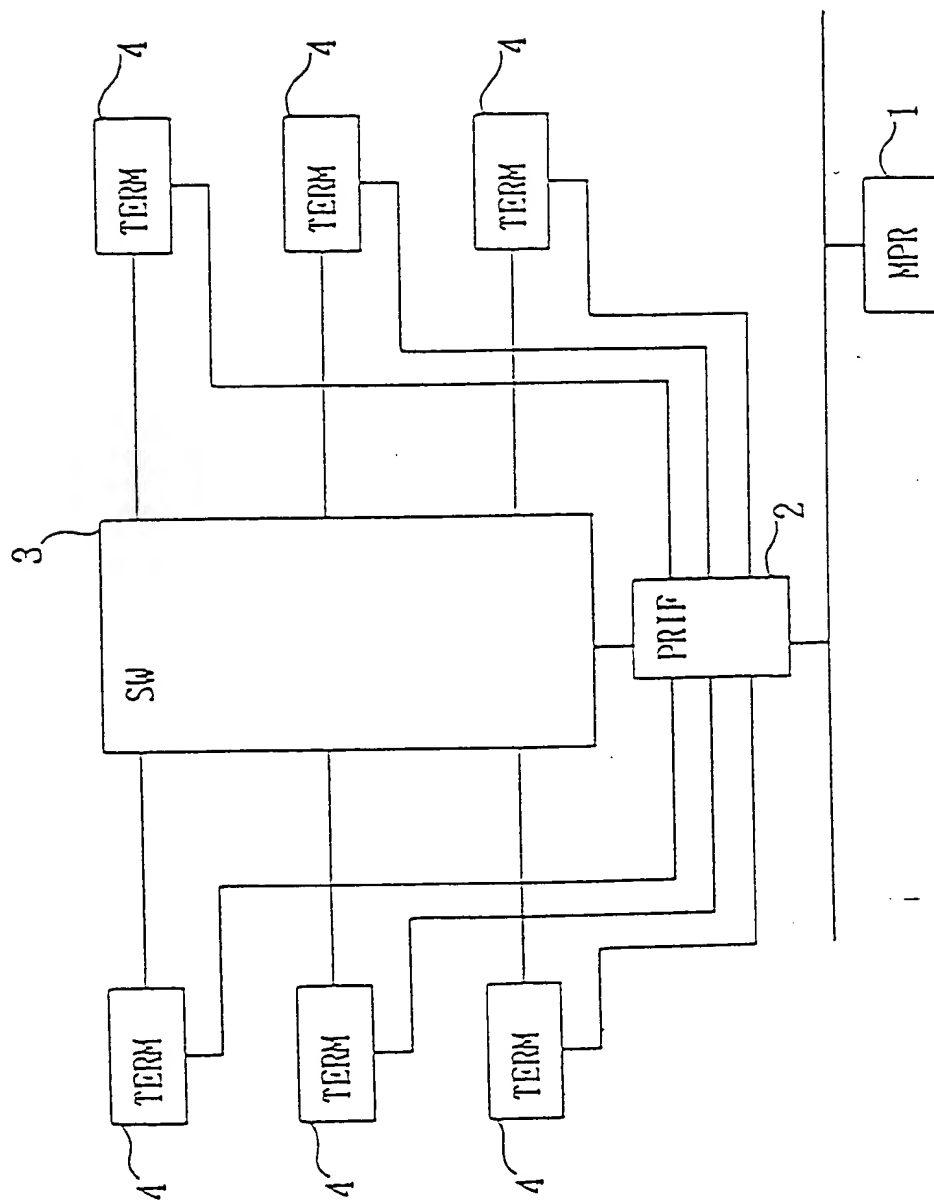


FIG. 903

66920-62220

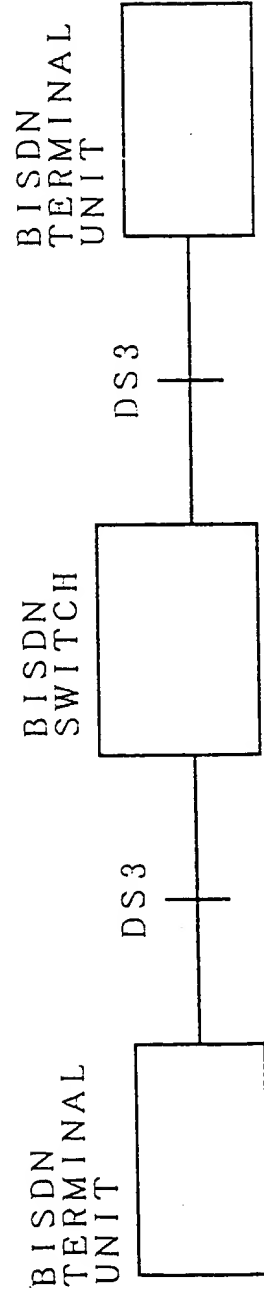


FIG. 904

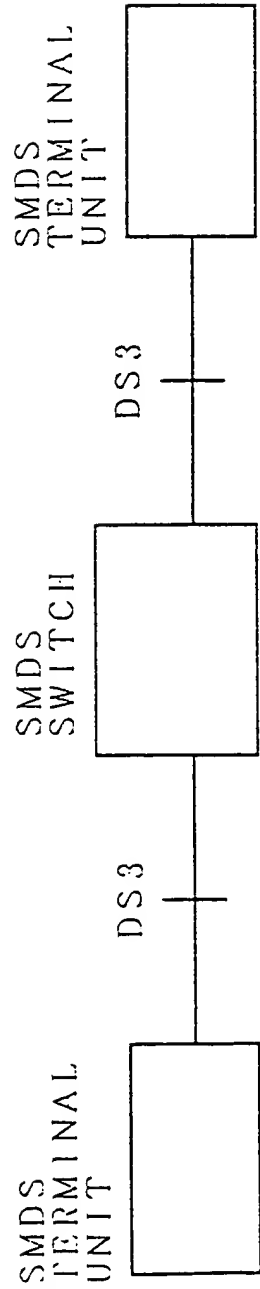
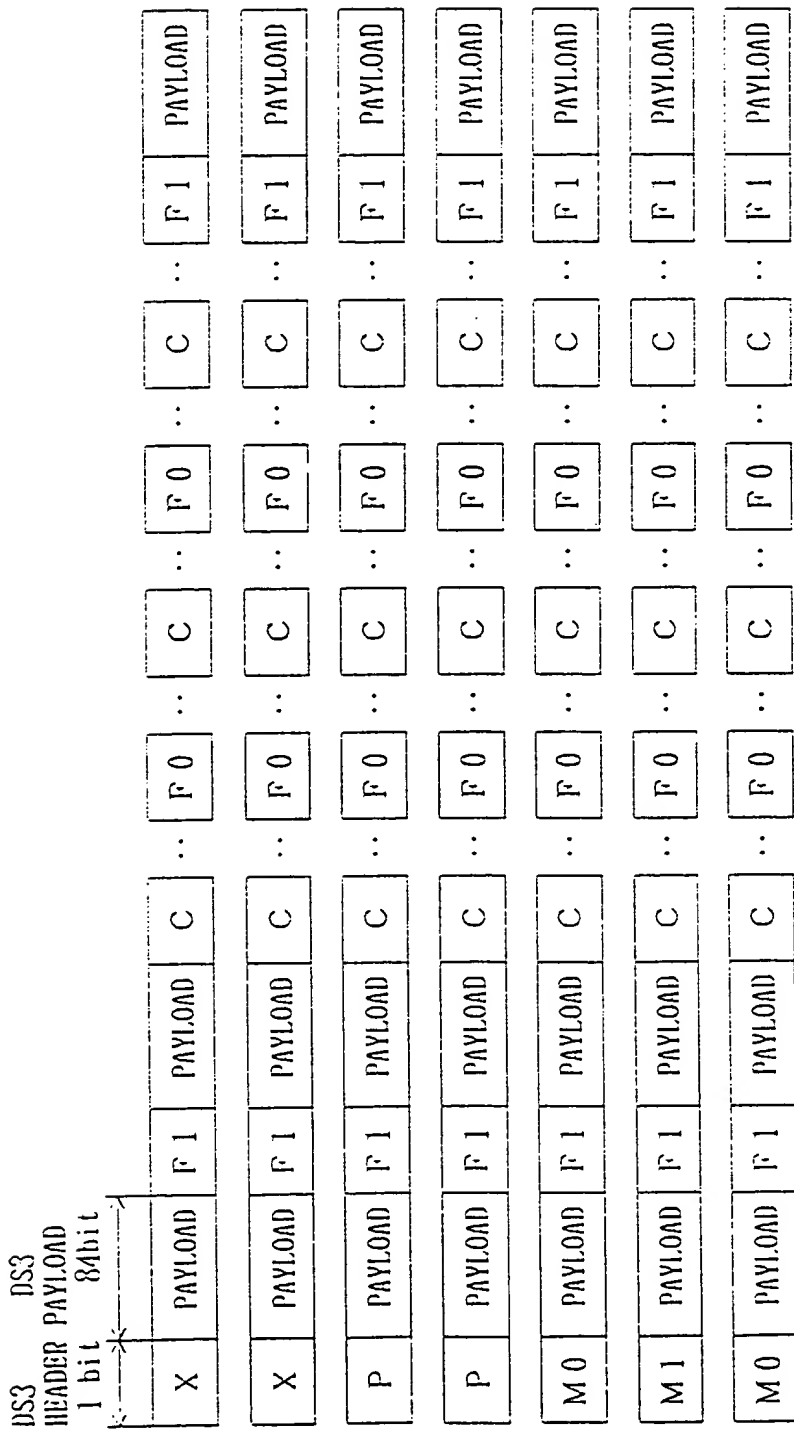


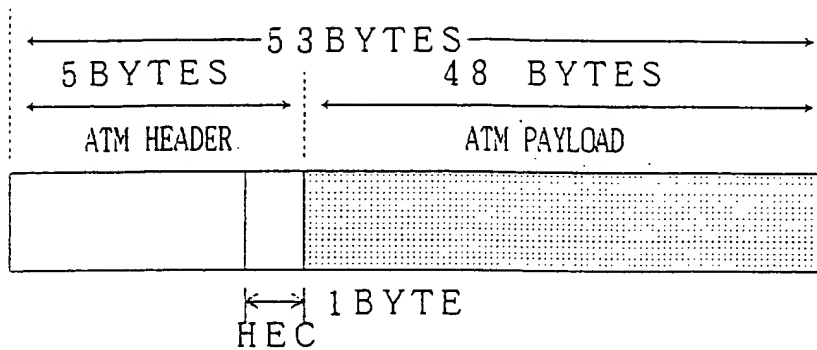
FIG. 905



DS 3 MULTIFRAME = 4760 BITS (85 BITS \times 8 \times 7)

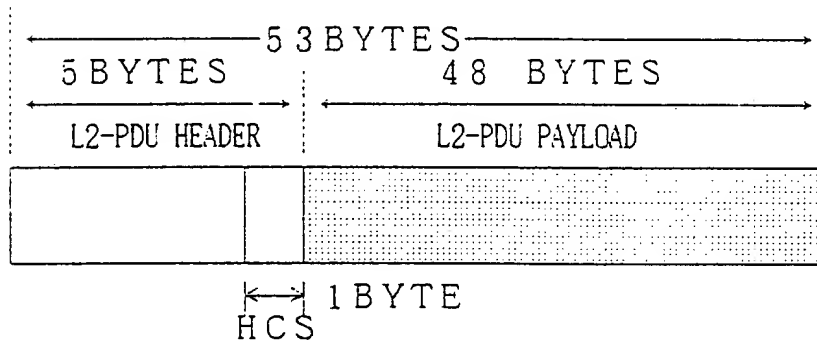
F 0, F 1 : SUBFRAME ALIGNMENT BIT
M 0, M 1 : MULTIFRAME ALIGNMENT BIT
P : PARITY INFORMATION BIT
X : ERROR STATE DESIGNATION BIT
C (RESERVED)

FIG. 906



HEC : HEADER ERROR CONTROL

(a) CONFIGURATION OF ATM CELL



HEC : HEADER CHECK SEQUENCE

(b) CONFIGURATION OF SMDS CELL

FIG. 907

000000-000000

PLCP HEADER				PLCP PAYLOAD	
2BYTES		1BYTE	1BYTE	53 (OCTET)	
A1	A2	POH1 P 11	POH Z 6	1st L2-PDU	
A1	A2	P 10	Z 5	L2-PDU	
A1	A2	P 9	Z 4	L2-PDU	
A1	A2	P 8	Z 3	L2-PDU	
A1	A2	P 7	Z 2	L2-PDU	
A1	A2	P 6	Z 1	L2-PDU	
A1	A2	P 5	F 1	L2-PDU	
A1	A2	P 4	B 1	L2-PDU	
A1	A2	P 3	G 1	L2-PDU	
A1	A2	P 2	M 2	L2-PDU	
A1	A2	P 1	M 1	L2-PDU	13/14 NIBBLES
A1	A2	P 0	C 1	12th L2-PDU	TRAILER

```

A1, A2 : FRAME ALIGNMENT
POHI (P11~P0) : PATH OVERHEAD IDENTIFIER OCTET
POH : PATH OVERHEAD OCTET
Z6~Z1 : GROSS OCTET
F1 : PLCP PATH USER CHANNEL
B1 : BIT INTERVAL PARITY 8
G1 : PLCP PATH STATUS
M2~M1 : SIP LEVEL 1 CONTROL INFORMATION
C1 : CYCLE STUFF COUNTER

```

FIG. 908

I T E M	C Y C L E S T U F F C O U N T E R	B I T P A T T E R N	R E M A R K S
C 1		<div> <div>11111111</div> <div>00000000</div> <div>01100110</div> <div>10011001</div> </div>	<p>TL IS REPRESENTED BY 4 TYPES OF C1 AS SHOWN BELOW BECAUSE TRAILER LENGTH TL PERIODICALLY CHANGES IN DS3 PLCP FRAME.</p> <p> ↗ FIRST TYPE (TL=13) ↗ SECOND TYPE (TL=14) ↗ THIRD TYPE (TL=13 : NO STUFF) ↗ THIRD TYPE (TL=14 : STUFF) </p>
T R A I L E R		1100	L E N G T H D E P E N D S O N C 1 B Y T E V A L U E .

FIG. 909

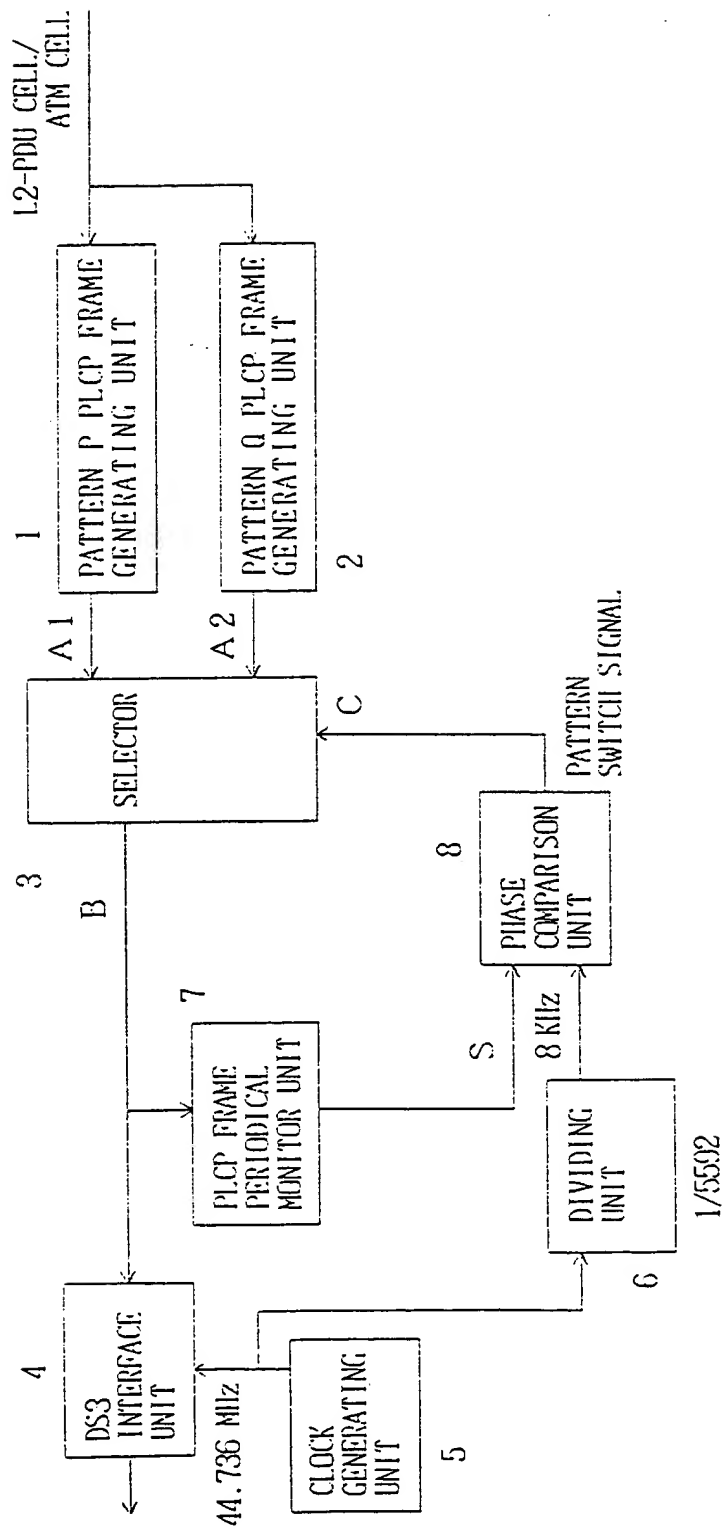


FIG. 910

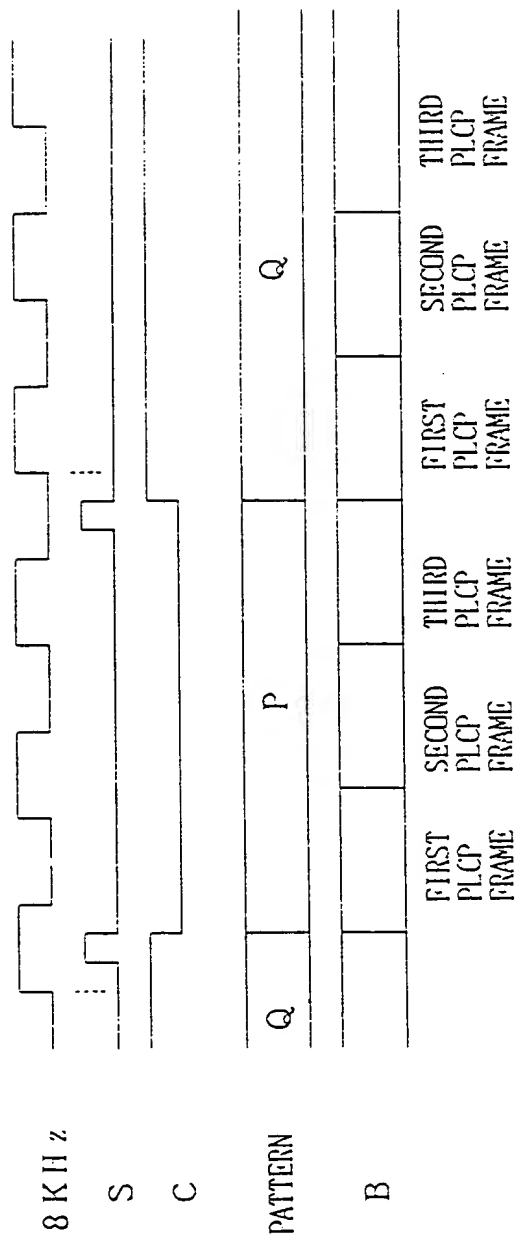
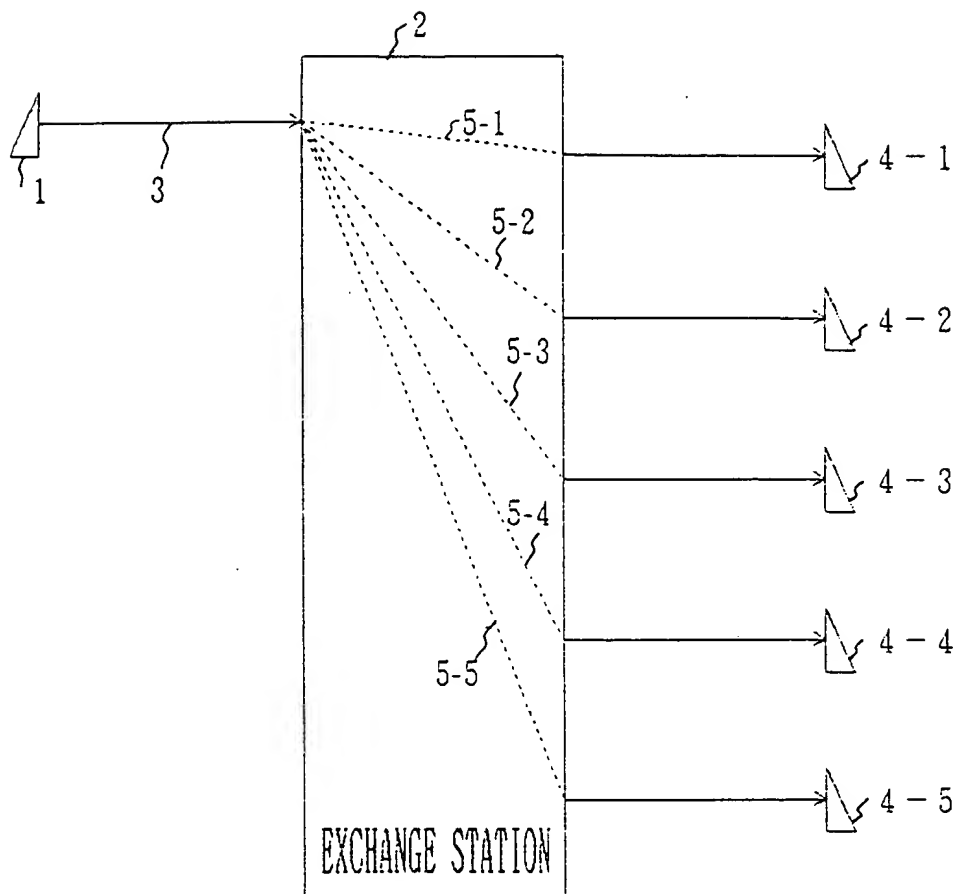
[illegible]

FIG. 16.

669360-ET2260



F I G. 9 1 2

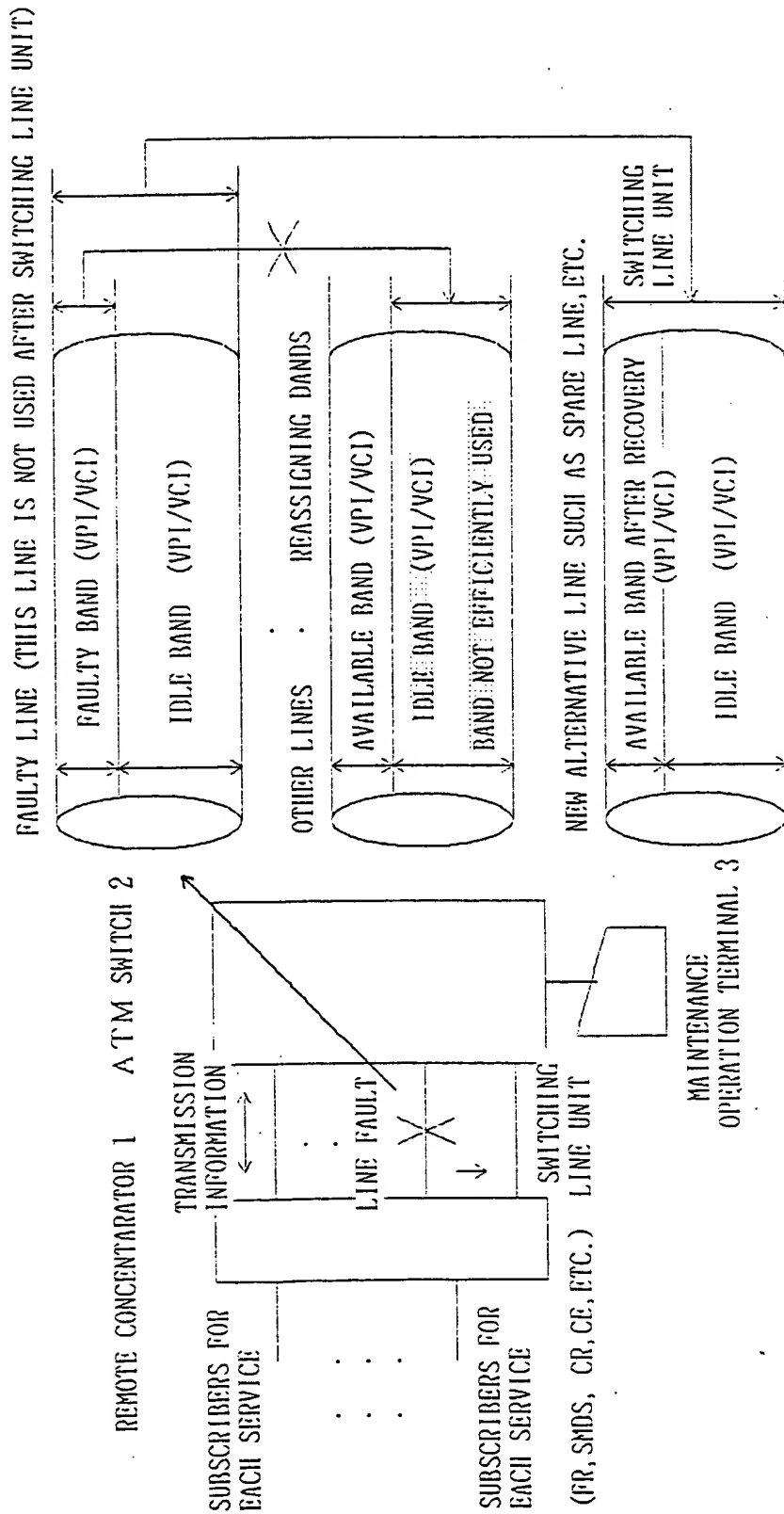


FIG. 913